

# Operational Amplifier Distortion

Samuel Groner, September 1, 2008

# Acknowledgements

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# Chapter 1

## Introduction

This paper provides the reader with a large amount of operational amplifier distortion measurement results. While DC precision and standard AC data such as open-loop gain and phase are readily available from the manufacturers datasheet, distortion within the audio frequency range is usually either totally absent from the specifications, listed with insufficient level of detail (as we will see later there are at least four largely independent distortion mechanisms which need separate specification) or at least derived with different setups amongst different manufacturers or even amongst different devices from the same manufacturer, making comparison difficult or even impossible.

Walt Jung presented a comparable measurement series in [1]. Unfortunately, many (if not most) modern low-distortion IC opamps are not included as the according work has been carried out before 1986. In this book Jung introduces the systematics to characterise operational amplifier distortion with three basic distortion mechanisms (transfer linearity, common-mode linearity and output linearity—see section 2.1 for more details); this method is used for the here presented work as well, although one important additional test (input impedance linearity) has been added and more detailed data (e.g. distortion at various levels) is shown. This greatly increases the significance of the measurements. Only voltage feedback amplifiers will be considered; current feedback amplifiers would need a different measurement setup because their bandwidth depends on the feedback resistor value used.

The author hopes that this measurement series helps to simplify and speed up the process of selecting an amplifier for a low distortion application by providing the so far lacking systematic data. Main application field for the presented results will be audio circuit design, but there might be other applications where low distortion within a similar frequency range is desirable as distortion is an error which is not easily reduced by system calibration as are gain and offset errors. As time permits, more opamps will

be measured and the results included in this document. An updated version will be available for download from (see section *IC OpAmps*):

[http://www.sg-acoustic.ch/analogue\\_audio/](http://www.sg-acoustic.ch/analogue_audio/)

This document is outlined as follows: chapter 2 presents how the opamp distortion is measured, how the measurement data is displayed and where the measurement limits are. In addition to this, a short text discusses some limitations of the measurement series and ideas for future work. The following chapter 3 presents the measurement data for all tested amplifiers. The appendix contains a personal conclusion, a short discussion on opamp topologies and a change log which records the changes applied to this document.

## Chapter 2

# Measurement Procedure

### 2.1 OpAmp Distortion Measurement

This measurement series characterises the distortion performance of operational amplifiers with four basic distortion mechanisms:

- *Transfer Linearity*: The distortion remaining after the three other distortion sources mentioned below have been eliminated. The amplifier operates in inverting configuration and with negligible output loading.
- *Common-Mode Linearity*: The distortion arising from operating the amplifier in a noninverting configuration; the input will see the full input signal as common-mode swing.
- *Output Linearity*: The distortion resulting from the amplifier having to provide a significant output current into a load.
- *Input Impedance Linearity*: The distortion resulting from the opamp being driven from a high impedance source when used as noninverting amplifier.

A fifth measure—called *high-frequency linearity*—is introduced to characterise transfer and common-mode linearity at high frequencies; as we will see in section 2.2, the standard measurement procedure for these two distortion mechanisms is limited to frequencies less than  $\frac{1}{2000}$  or  $\frac{1}{3000}$  of the amplifier gain bandwidth product. As this might be below 20 kHz for many amplifiers and because linearity above the audible range is of interest as well even for audio applications (e.g. to avoid intermodulation distortion with spurious HF interference), the additional figure is used.

One of the main problems when measuring opamp distortion is the fact that for essentially all devices the distortion of a typical amplifier configuration with low noise gain is well below the measurement limit of even the best currently available equipment for distortion measurement. This is

especially true at low and medium frequencies (say below 5 kHz) and for THD+N measurements, where noise of the oscillator source and the analyser often make up a significant contribution of the reading. But even with a THD measurement insensitive to noise (e.g. by means of spectral analysis) it is close to impossible to reach the distortion floor of less than  $-160$  dB achieved by the best opamps tested.

One convenient solution as suggested in [1] is to run the opamps at considerable noise gain but unity signal gain; this reduces loop gain and hence proportionally the linearity of the device under test while the oscillator and analyser operate at their optimum signal level. Figure 2.1 shows the three circuits used to test the amplifiers at about 60 dB noise gain. The first circuit is used to test transfer linearity. As the amplifier is operated in inverting configuration any common-mode swing is avoided; output loading is low as the feedback resistor and the input impedance of the analyser are chosen high (10 k $\Omega$  and 100 k $\Omega$  respectively). For many amplifiers the distortion measured up to a few kHz frequency is masked by the noise<sup>1</sup> of the amplifier, even up to levels of just a few dB below clipping. The distortion is usually dominated by the 2<sup>nd</sup> harmonic (rarely by the 3<sup>rd</sup> harmonic), with higher harmonics rapidly falling in level. Above a few kHz distortion rises as loop gain is falling and the linearity of the input differential pair decreases because it needs to provide higher output currents to charge/discharge the compensation capacitor [2].

The second circuit shown in figure 2.1 is used to measure common-mode linearity. The input stage is exposed to the full voltage swing; the presence of a common-mode voltage swing modulates bias parameters of the input transistors (e.g. as the impedance of the according tail current source is finite) which in turn generates a distorted output signal. This is once more amplified by the 60 dB noise gain. The observed distortion is usually rising with frequency and heavily dominated by the 2<sup>nd</sup> harmonic, with higher frequency even order distortion products being present as well. Some amplifiers show a frequency independent but lower level distortion mechanism which is dominant at low frequencies only. For most amplifiers common-mode linearity will be one or even two orders of magnitude worse than the basic transfer linearity. It is obvious that for lowest distortion careful consideration to this distortion mechanism must be given. Fortunately enough for many applications the common-mode swing will be lower because the feedback is set to provide signal gain above unity (i.e. the input signal is of considerably lower level than the output signal); this will reduce common-mode distortion accordingly.

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<sup>1</sup>The main contributor being voltage noise as the effective source resistance seen by the amplifier is below 10  $\Omega$ , rendering current noise contributions negligible.

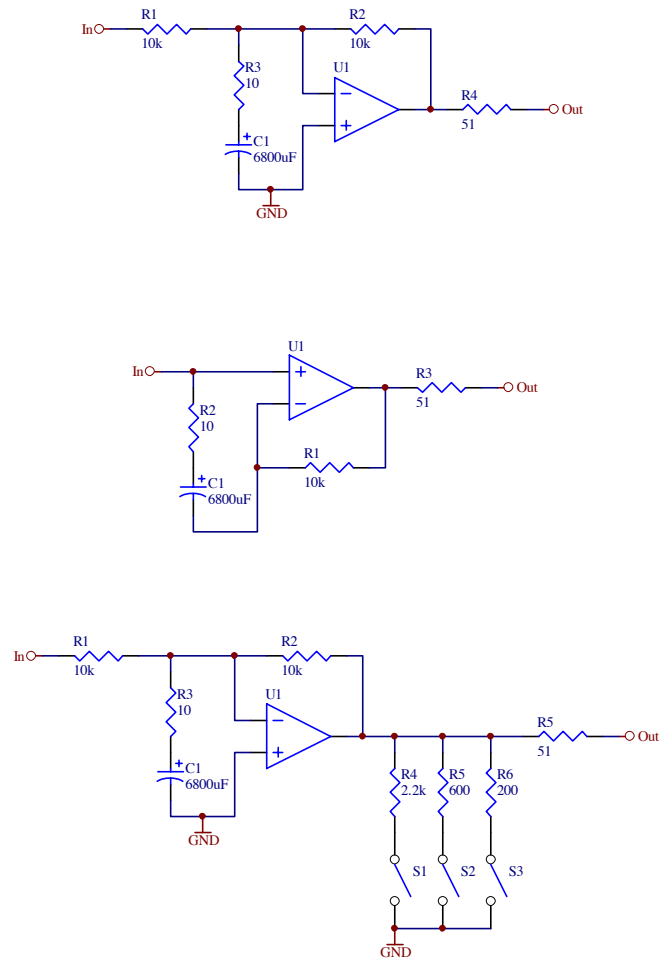


Figure 2.1: Measurement configuration for the transfer, common-mode and output linearity (top to bottom).

The last configuration in figure 2.1 tests the output linearity of the amplifier. The circuit is identical with the one used for the transfer linearity test (i.e. an inverting configuration with 60 dB noise gain and 0 dB signal gain), except that a grounded resistive output load is added. Two different values are used, 2.2 k $\Omega$  and 600  $\Omega$ . For the few amplifiers which can drive heavier loads without current limiting an additional test with a 200  $\Omega$  load is done. Some IC amplifiers have output stage quiescent currents of up to 2 mA; accordingly they will operate in low-distortion class A for the transfer linearity and common-mode linearity test. With the increased output loading the output stage is forced to enter class B (or AB), now contributing with crossover distortion as well. Additional increase in distortion may result from finite current gain of the output stage; the input impedance of the output stage becomes lower and more voltage-dependent with increased output loading. This in turn will load the preceding gain stage (which typically has a high impedance output node) and reduce both open-loop gain and open-loop linearity.

The distortion observed for the output linearity test is often two to three times worse than the basic transfer linearity at high levels (around +20 dBu); even more obvious is this distortion at medium levels (0 dBu), where it might worsen the amplifier performance by one or two orders of magnitude—making clear that there is little reason to neglect these effects if best performance is needed. The observed distortion is often dominated by odd-order harmonics, with many higher-order distortion products visible.

In addition to this, the output linearity test might highlight thermal effects which show up as a with increasing loading rising low-frequency distortion. This is due to thermal coupling of input and output circuit transistors. At low frequencies the voltage dependent power dissipation of the output stage is able to modulate the input pair offset voltage; this effect effectively provides non-linear low-frequency feedback (of basically unknown polarity, i.e. either positive or negative feedback), worsening the open-loop linearity of the amplifier [3]. The magnitude of this effect is mainly dependent on the chip layout, which should be arranged to cancel thermal gradients from the output stage at the input stage.

As the amplifier is run at 60 dB noise gain for all three so far presented tests, the small signal bandwidth of these measurement circuits is limited to about  $\frac{1}{1000}$  the frequency of the gain bandwidth product<sup>2</sup> of the amplifier under test. The resulting low-pass filter will significantly reduce the level of the harmonics above its  $-3$  dB frequency; depending on whether the 2<sup>nd</sup> or 3<sup>rd</sup> harmonic is the dominant contributor the THD+N figure will hence roll off at  $\frac{1}{2000}$  or  $\frac{1}{3000}$  the frequency of the gain bandwidth product. This limits

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<sup>2</sup>Note that the gain bandwidth might be higher than the unity-gain frequency as many amplifiers deviate from the textbook 6 dB/octave open-loop gain roll-off in order to improve slew-rate and loop gain at signal frequencies.

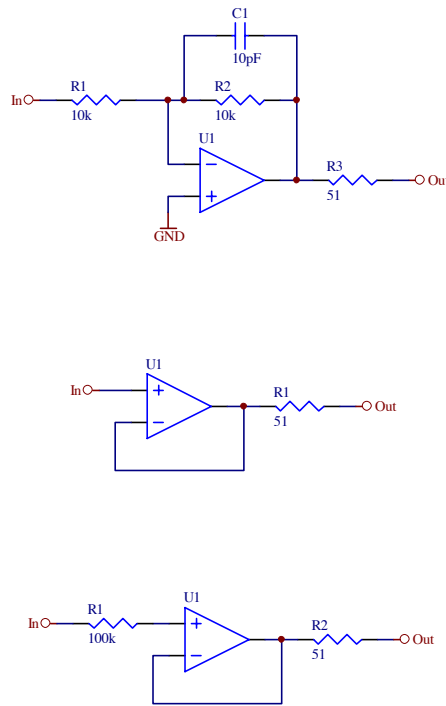


Figure 2.2: Measurement configuration for the inverting (top) and noninverting (middle) high-frequency linearity. The third circuit at the bottom shows the setup used to measure input impedance linearity.

the significance of the measurements at high frequencies. As mentioned before this is addressed by the additional high-frequency measurements.

Figure 2.2 shows the two setups to measure inverting and noninverting high-frequency linearity. The amplifier is operated at 6 dB (inverting) and 0 dB (noninverting) noise gain, and hence the bandwidth is very wide, allowing distortion measurements up to high frequencies without attenuating harmonics. The amount of distortion measured above the audio frequency range will often be inversely proportional to the slew-rate of the amplifier; because of this the term *slew-induced distortion* has sometimes been used to qualify high-frequency distortion. Note however that this relationship is only true for standard input stage topologies; there are amplifiers which dynamically increase the current available for charging the compensation capacitor. While these topologies increase the observed slew-rate they do not necessarily improve linearity within the here measured frequency range [4]. In addition to this it can be observed that amplifiers with JFET inputs typically have higher distortion than amplifiers with comparable slew-rate but using bipolar inputs. Last but not least it is possible that at higher frequencies additional gain stages which follow the input stage (see appendix B for an introduction on opamp topologies) may produce significant high-frequency

distortion, e.g. due to voltage dependent junction and substrate capacity. A slew-rate measurement will hence not replace a proper high-frequency distortion measurement.

The inverting configuration typically shows more distortion at very high frequencies (around 100 kHz) than the noninverting as the later configuration has less loop gain. However at somewhat lower frequencies (say 20 kHz) slew-induced distortion is greatly reduced and the noninverting configuration is often dominated by common-mode nonlinearity, making the total distortion figure inferior to that of the inverting high-frequency measurement. If slew-induced distortion is dominant, the observed distortion residual will mainly consist from 3<sup>rd</sup> harmonic; if the slew-rate of the amplifier is substantially asymmetric the 2<sup>nd</sup> harmonic will contribute as well.

The third setup shown in figure 2.2 is used to measure input impedance linearity. Due to the action of feedback, the input impedance of the shown follower configuration is raised towards the common-mode input impedance (and not towards infinity as often assumed). The common-mode input impedance however shows a dependence on common-mode voltage; this is mainly because of voltage-dependent junction capacity of the input transistors and equally voltage-dependent input capacity due to substrate diode connections from the input transistor's base or gate [5][6][7]. Secondary effects may result from  $h_{FE}$  dependence on collector voltage (once more of course of the input transistors), input bias cancellation circuits or ESD protection.

Now if a noninverting opamp configuration is driven from a non-zero source impedance the resulting input impedance modulation—remember that for a noninverting configuration the input signal appears as common-mode swing—will distort the signal as the source impedance and the input impedance form a voltage divider. At first one might expect these effects to be benign as the common-mode input impedance is often in the order of some hundred M $\Omega$  in parallel with just a few pF. However, the observed distortion with the used 100 k $\Omega$  source impedance (R1 in the third configuration shown in figure 2.2) is for almost all devices gross and will entirely dominate any other distortion source. Of course lowering the source impedance will proportionally reduce these effects, as will reducing the input level (as e.g. the case for noninverting configurations with signal gain above unity).

The observed distortion consists usually mainly of 2<sup>nd</sup> harmonic, though some 3<sup>rd</sup> and higher harmonics are visible as well. It is an unhappy coincidence that opamps with JFET inputs—which are usually used for high source impedances due to their low current noise—typically have much higher input capacity than bipolar amplifiers which causes considerably higher input impedance nonlinearity at high frequencies.

Figure 2.3 shows the test jig used for the distortion measurements. For easy compatibility with different IC pinouts and discrete opamps sockets



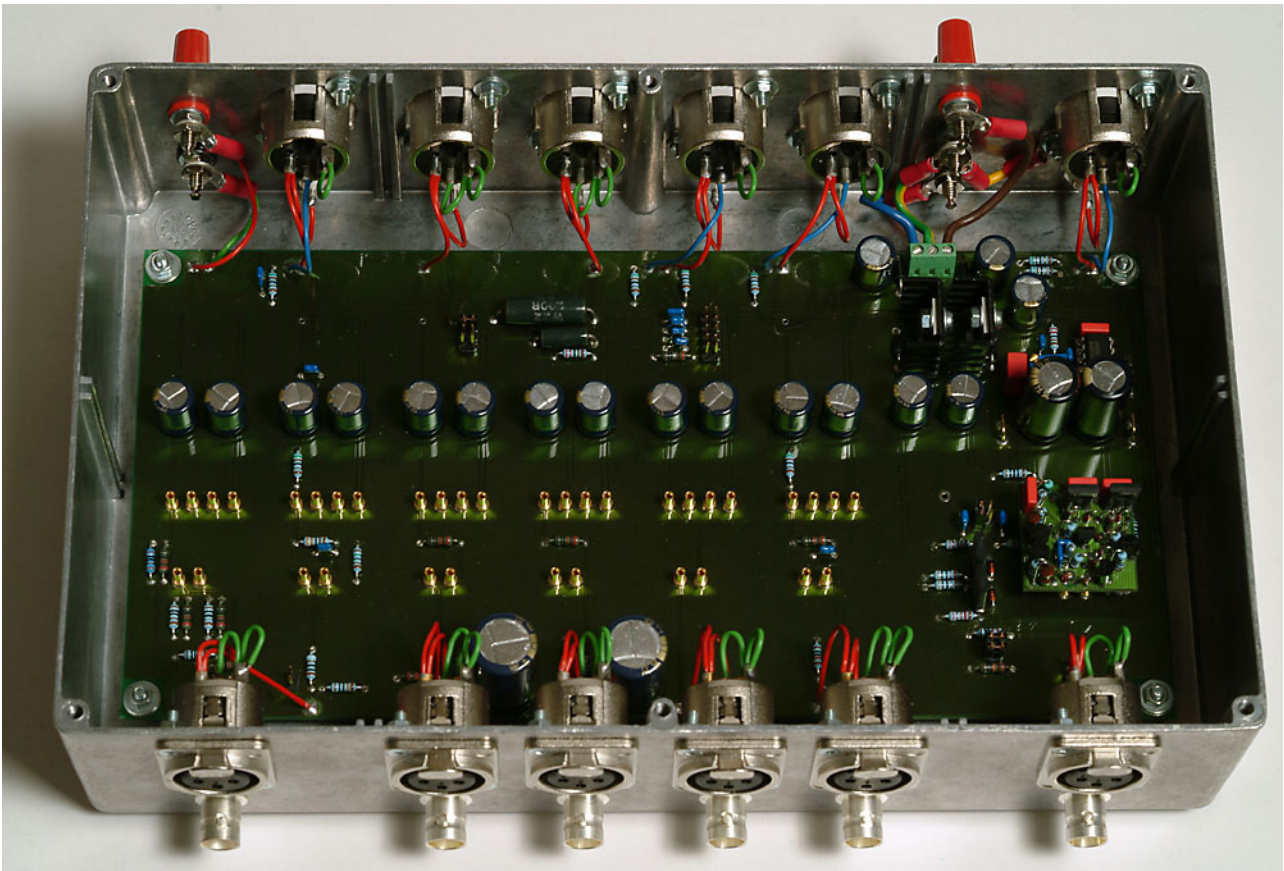


Figure 2.3: The test jig used to gather the distortion measurements. Additional parameters such as noise and offset can be measured as well.

are used to accommodate daughterboards. A 100 nF capacitor from each supply rail to ground is placed on each daughterboard in close proximity to the amplifier to guarantee stability; a pair of 220  $\mu$ F capacitors on the motherboard for each test circuit and the use of a linear laboratory power supply provide a low impedance supply within the audio frequency range. The amplifiers are tested at a nominal supply voltage of  $\pm 15$  V; devices which have a maximum supply voltage above 36 V are additionally tested at two volts below the maximum supply voltage, e.g. at  $\pm 21$  V for a 44 V rated opamp.

## 2.2 Data Acquisition And Display

This measurement series uses four different ways of presenting the distortion measurements:

- THD+N vs. frequency plot

- THD+N vs. amplitude plot
- Time-domain analysis of the distortion residual
- Spectral analysis of the distortion residual

In the following we will discuss the exact parameters set for the oscillator source and analyser and the additional processing steps carried out to arrive at the graphs presented in chapter 3.

For the THD+N vs. frequency plots the oscillator source was set to provide a fixed +20 dBu output level; the frequency was swept in 100 steps from 10 Hz to 200 kHz (corresponding to the maximum frequency range of the used Audio Precision System One measurement system). No filter in the analyser was used<sup>3</sup> in order to accommodate as many high-frequency harmonics as possible—mostly an issue for the high-frequency measurement where the amplifier is operated at low closed-loop gain and hence has itself high bandwidth as discussed in more detail above. As at lower frequencies it is difficult to estimate from the THD+N plot whether the shown number is actual distortion or just the noise floor<sup>4</sup> a sweep is run at -20 dBu; by dividing these numbers by hundred the noise floor is derived as now the residual is almost pure noise.

Subsequently the measurement data is imported into MATLAB to generate the graphs. For easy reading the various THD+N vs. frequency measurements are displayed in three different plots. The first shows transfer and common-mode linearity as well as the noise floor; to help interpretation of the data the small-signal bandwidth of the amplifier configuration (given as  $\frac{1}{1000}$  of the opamp gain bandwidth product) is shown.

The second graph is used to display the output linearity measurements. As before, the small-signal bandwidth is indicated; in addition to this, the transfer linearity plot is repeated to aid comparison with the distortion performance without significant output loading. The last graph shows the two high-frequency linearity measurements and the input impedance linearity measurement. As now the small-signal bandwidth is very high its display is omitted and the large-signal bandwidth shown instead. This shall back-up the often observed correlation between high-frequency distortion and large-signal bandwidth. For faster amplifiers the large-signal bandwidth is in excess of 200 kHz and hence does not show up in the graph. As at least at lower frequencies this measurement is for almost all tested devices dominated by source/analyser residual and not actual opamp performance the measurement limit is shown.

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<sup>3</sup>The bandwidth of the analyser is stated as at least 10 Hz–500 kHz without filters.

<sup>4</sup>Note that the observed noise floor is not only dependent on the amplifier's voltage noise but as well on its gain bandwidth product as there are no filters used to explicitly define the measurement bandwidth.

The THD+N vs. amplitude measurements are run at three discrete frequencies (100 Hz, 1 kHz and 10 kHz); the level is swept in 100 steps from  $-20$  dBu to either  $+30$  dBu or the level with peak-to-peak amplitude corresponding to the used power supply voltage, whichever is smaller. Limiting the input voltage will prevent damage of the amplifier for the common-mode linearity test. As now the measurement frequencies are fixed, bandpass filters can be used in the analyser to improve the resolution. The filters are set as follows: 100 Hz–22 kHz for the 100 Hz fundamental, 400 Hz–22 kHz for 1 kHz and 400 Hz–80 kHz for the 10 kHz measurement. The various measurements are finally displayed in three plots, one for each measurement frequency. For simplicity only a sweep with  $600\ \Omega$  loading is done for the output linearity test.

The time-domain and spectrum analysis are considerably more elaborate and incorporate additional processing steps. They are used to gather more information about the spectral distribution of the distortion, the residual waveform and distortion at low levels (where the amplifier noise might dominate a THD+N reading). The measurement is carried out at a fixed frequency of 1 kHz and three levels ( $+20$  dBu, 0 dBu and  $-20$  dBu) by recording 10 seconds of the oscillator monitor output and the reading output (i.e. the residual after the analyser notch filter) simultaneously with a standard audio recorder set to 96 kHz sampling frequency and 16 bit resolution. An analyser bandpass filter of 400 Hz–30 kHz has been set in order to avoid aliasing in the AD converter and to remove hum and low-frequency noise. As for the THD+N plots only a  $600\ \Omega$  output loading test is done.

For further signal processing this data is imported into MATLAB. By scaling the amplitude of the two signals according to the THD+N reading which was noted during the recording of the signals the original amplitude relation between fundamental and distortion residual is restored, although the gain which has been applied to the residual by the analyser is not known directly. To further reduce remaining fundamental, low-frequency noise and hum in the residual signal a steep linear phase digital high-pass filter at about 1.8 kHz is applied.

For the time-domain display of the residual waveform the signals are now averaged 3000 times to reduce noise in the residual signal. This corresponds to a noise reduction of about 34.7 dB. For the spectrum analysis a FFT with the following parameters is used:

- size: 65 536 samples
- window: Kaiser,  $\beta = 50$
- averages: 110

Table 2.1 summarises the important settings of the different measurements as discussed above. The following list shows several hardware settings

Measurement	Amplitude	Frequency	Filter
THD+N vs. frequency	+20 dBu (distortion) −20 dBu (noise floor)	10 Hz–200 kHz	–
THD+N vs. amplitude	−20 dBu to +30 dBu or the amplitude with corresponding peak-to-peak voltage equal to the power supply voltage, whatever is smaller	100 Hz 1 kHz 10 kHz	100 Hz–22 kHz 400 Hz–22 kHz 400 Hz–80 kHz
Spectral and time-domain analysis of residual	+20 dBu, 0 dBu and −20 dBu	1 kHz	400 Hz–30 kHz, additional digital high-pass filter at 1.8 kHz

Table 2.1: Table summarising the different parameters which were set to acquire the measurement data.

of the Audio Precision System One which were used for all measurements and might be of interest:

- Oscillator: source impedance  $50 \Omega$ , floating balanced
- Analyser: input impedance  $100 \text{ k}\Omega$
- Detector: RMS, 4 readings/s

## 2.3 Measurement Limit

It is always a good idea to check what the measurement limit of a given setup is. For this measurement series an Audio Precision System One has been used as signal source and analyser. Figure 2.3 shows the measurement limit as THD+N vs. frequency and THD+N vs. level (for 100 Hz, 1 kHz and 10 kHz frequency, filters set as shown in table 2.1) plots as well as FFT and time-domain residual analysis. Note that for most graphs the Y axis scaling has been changed compared to the opamp measurements to accommodate the lower readings observed.

At that point it is important to remind the reader about the interaction of two consecutive distortion sources. Depending on the actual phase relation between the two distortion sources at a given harmonic the distortion contribution can either add arithmetically for in phase relation (i.e. a 6 dB increase for equal distortive sources), subtract for out of phase relation (i.e. cancel for equal distortive sources) or add geometrically for a  $90^\circ$  relation (i.e. a 3 dB increase for equal distortive sources). In-between phase relationships are possible as well, resulting in partial cancellation, addition or no change at all [8]. This means that it is impossible to meaningfully measure THD+N close to the measurement limit of the used source/analyser combination as the three contributions are not distinguishable.

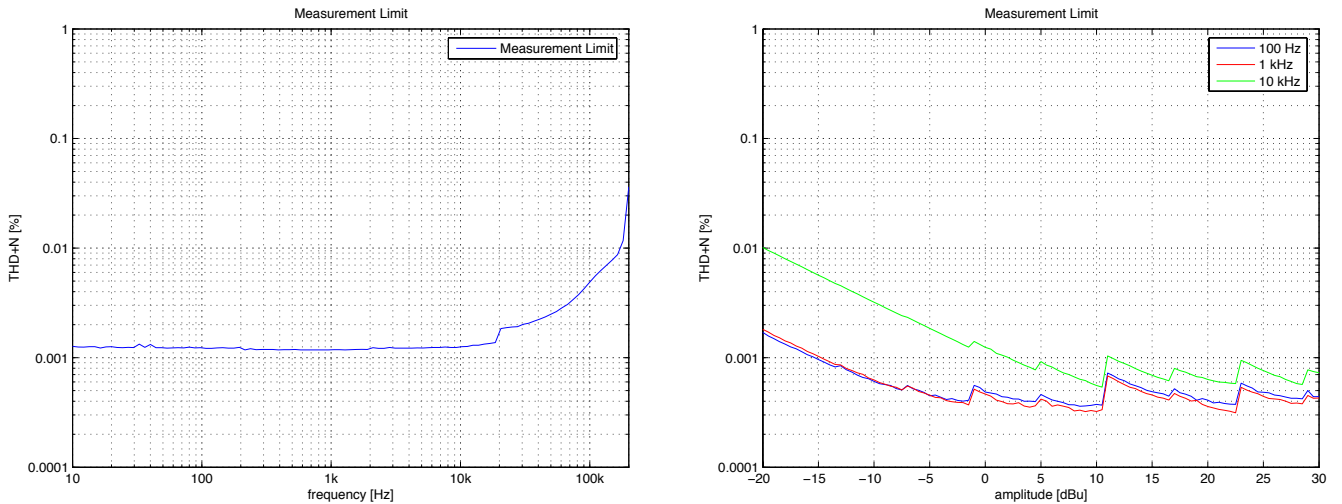


Figure 2.4: Measurement limit THD+N vs. frequency (left) and THD+N vs. level (right). Filters, frequencies and levels set according to table 2.1.

Typically it is found that for dependable results the device under test should show at least three times higher distortion than the source and analyser. Upon comparing the measurement limits with the measurement results it is found that this figure is easily met for most amplifiers and tested configurations except for the high-frequency measurements. High-speed amplifiers will reach (or probably even surpass) the distortion level of the source/analyser combination; it is thus advisable to consider these measurements with a grain of salt if the graph doesn't show distortion significantly above the measurement limit. In fact, cancellation of source, device under test and analyser distortion can be observed for some amplifiers, resulting in readings *below* the measurement limit.

While running this measurement series it was found that the measurement limit of the Audio Precision System One shows some fluctuation at the highest and lowest frequencies. In addition to this, some low-level interference of unknown origin at about 1.8 kHz and above has been observed; while of low enough level to not significantly affect the THD+N readings this does show up for some of the FFT plots, especially for the common-mode test.

## 2.4 Do These Measurements Tell It All?

Although the author hopes that this paper is a considerable advance over previously available data, it is not possible to present measurement data for all distortion mechanisms in exhaustive detail here. In the following paragraphs we will look at some limitations of the presented research and how one could gather further information for the missing gaps.

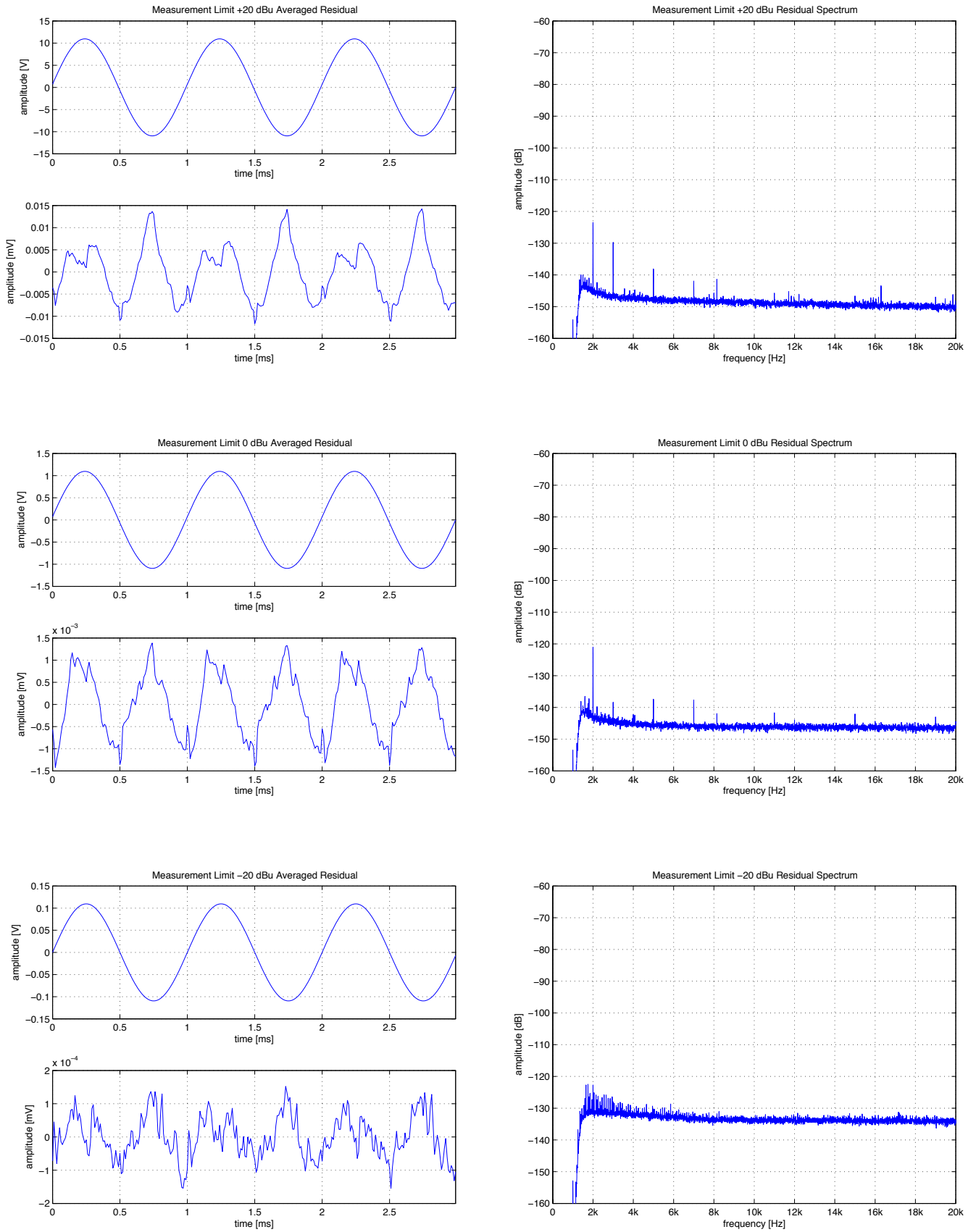


Figure 2.5: Measurement limit as FFT and time-domain residual analysis. Frequencies and levels set according to table 2.1.

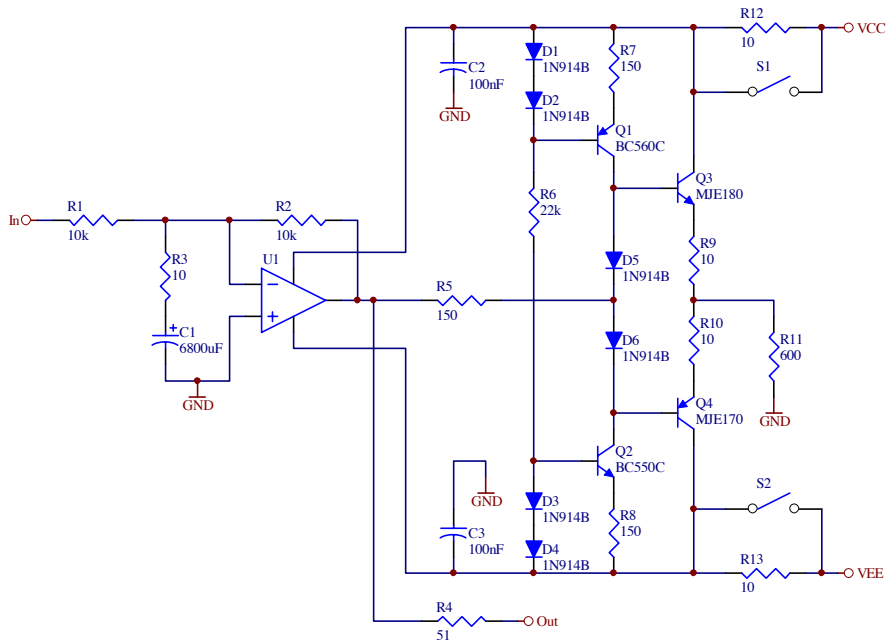


Figure 2.6: Suggested circuit to measure distortion from finite PSRR. Close switch S2 for a positive PSRR measurement and S1 for the negative PSRR. Omit C2 and C3 for opamps with on-board decoupling capacitors such as modular amplifiers.

One distortion source which is not detected at sufficient level in this measurement series is distortion injected through the supply rails. If an amplifier has to drive a heavy load which makes the output stage of the amplifier enter class B (or whatever switching class it is), half-wave rectified and hence heavily distorted currents are drawn from the power supply. By the action of finite supply impedance these currents are converted to an according supply ripple. A portion of this ripple will enter the amplifier circuitry by means of finite PSRR, appear as an output voltage and worsen the distortion performance of the amplifier.

Fortunately enough this distortion is usually easily reduced to negligible levels by keeping the supply impedance low by means of (as necessary local) voltage regulators and/or decoupling. If a more detailed insight is needed nonetheless calculation based on the PSRR of the amplifier (for which typical data is usually available from the datasheet), the output current and the power supply impedance might be helpful. Alternatively a setup as shown in figure 2.6 will provide measurement data [9].

Input impedance modulation has been introduced in section 2.1; it has not been mentioned though that this distortion mechanism can be partially canceled by matching the impedances seen at both input terminals—which

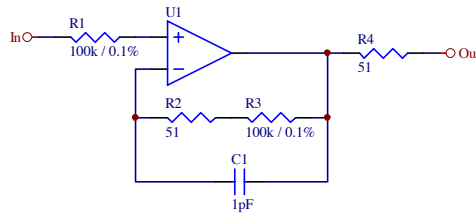


Figure 2.7: Circuit which can be used to test for input impedance modulation with matched impedances. Set R2 to the value equal to the oscillator source impedance.

of course assumes that the source impedance seen at the noninverting terminal is known. The matched impedances will duplicate the error at both inputs and suppress it by the CMRR of the amplifier. In practice the cancellation seems to be difficult to achieve with good accuracy<sup>5</sup> though and reducing the impedance level to start with is usually more effective. In any case it would be interesting to have a figure showing how good the cancellation is achieved for the various devices. The setup shown in figure 2.7 will achieve this. C1 is needed for stability (for many amplifiers a higher value will be needed) and R2 should be chosen to be equal to the oscillator source impedance (which will effectively add up with R1).

Another now rather subtle effect is distortion caused by nonlinear AC input bias currents as pointed out in [11]. As  $h_{FE}$  of a BJT transistor is a function of collector current and because finite open-loop linearity and global feedback constraint the input pair collector current to be nonlinear in order to keep the amplifier output linear it can be seen that the input bias currents of the amplifier must be nonlinear. The presence of a finite source and/or feedback impedance will result in an error which cannot be reduced by global feedback—in a similar way as input bias currents introduce DC errors. Amplifiers with low initial (i.e. before input bias current cancellation is applied) input bias currents, good open-loop linearity and/or a input bias current cancellation scheme tracking AC currents will be at an advantage here. Note that FET input amplifiers might not be entirely immune to this phenomena though; while DC input currents are usually very low, the often rather large input capacity might result in a significant AC input current.

The author suspects that these effects will usually be negligible in magnitude if feedback and source impedances are reasonably low. For verification the transfer linearity measurement setup could be altered by inserting a large resistor (typically 10 k $\Omega$  might be suitable) in series with the noninverting

<sup>5</sup>One possible explanation for this effect is that the input transistor pair collector/drain load shows an impedance mismatch for some topologies which in turn mismatches the capacity modulation for inverting and noninverting input [10].



input. The resulting distortion will be amplified by the 60 dB noise gain of the configuration.

In addition to the discussion above it must be appreciated that the measurement data presented here is for almost all devices derived by measurement of a single specimen; no claim can be made that this data is representative, and for sure no worst-case values can be given. It would be most interesting and convenient to have statistical data about the production variation of distortion—unfortunately no manufacturer seems to provide this information.

Finally it will be obvious for the alerted reader that the distortion observed in a final design will depend on the implementation (and not on the amplifier alone) and that distortion is never the only important design criteria. Parameters such as noise and frequency response (and much more—see e.g. [12] for a detailed list relevant for audio circuits) as well as anticipated cost and complexity might dictate a compromise; currently this writing cannot provide any further guidance to the (often difficult) problem of deriving an optimum implementation compromise for a given application, the author hopes though to include some information on this topic in a later revision.

## Chapter 3

# Measurement Results

The following pages present the measurement results of the various operational amplifiers tested, sorted in alphabetical order. For each amplifier a condensed specification table is given; the data is derived from the manufacturer's datasheet and the lowest-grade part has been chosen for devices where selected parts are available.<sup>1</sup> The price per unit—shown for the cheapest package and lowest grade—is based on data from the manufacturer's webpage and might not be up to date. In the following, a short text gives information about the amplifier topology (as far as this is known), its noise performance and additional external components such as compensation capacitors. Furthermore the most important results from the distortion measurements are highlighted, summarised and set in relation to the cost of the amplifier.

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<sup>1</sup>Usually devices are selected for DC precision (offset voltage, input bias current and input offset current); the often considerable additional expense for the graded version is not usually justified at least for audio applications.

### 3.1 Analog Devices AD797

<b>Number of Channels</b>	1
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	4.27 US\$ at 1k units (July 2008)

Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		25	80	$\mu\text{V}$
Input Bias Current		0.25	1.5	$\mu\text{A}$
Input Offset Current		100	400	nA
Gain Bandwidth Product		110		MHz
Slew-Rate	12.5	20		$\text{V}/\mu\text{S}$
Input Voltage Noise ( $f = 1 \text{ kHz}$ )		0.9	1.2	$\text{nV}/\sqrt{\text{Hz}}$
Input Current Noise ( $f = 1 \text{ kHz}$ )		2		$\text{pA}/\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 11$	$\pm 12$		V
Output Voltage Swing ( $R_L = 2 \text{ k}\Omega$ )	$\pm 12$	$\pm 13$		V
Output Voltage Swing ( $R_L = 600 \Omega$ )	$\pm 11$	$\pm 13$		V
Output Current	$\pm 30$	$\pm 50$		mA
Power Supply Voltage	$\pm 5$		$\pm 18$	V
Quiescent Current per Amplifier		8.2	10.5	mA

Table 3.1: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 15 \text{ V}$ .

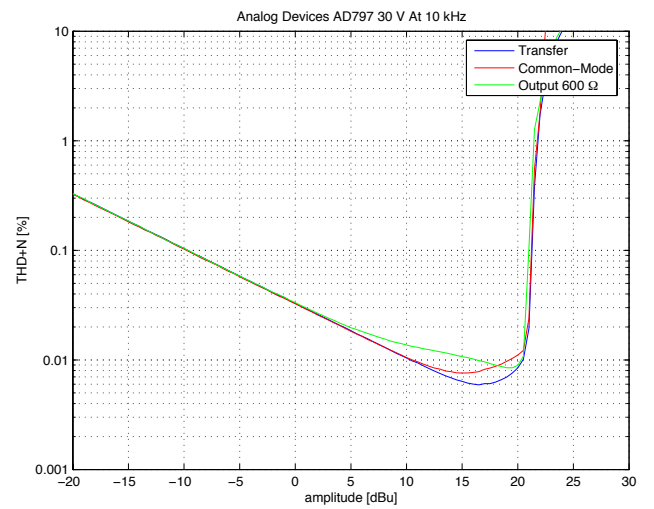
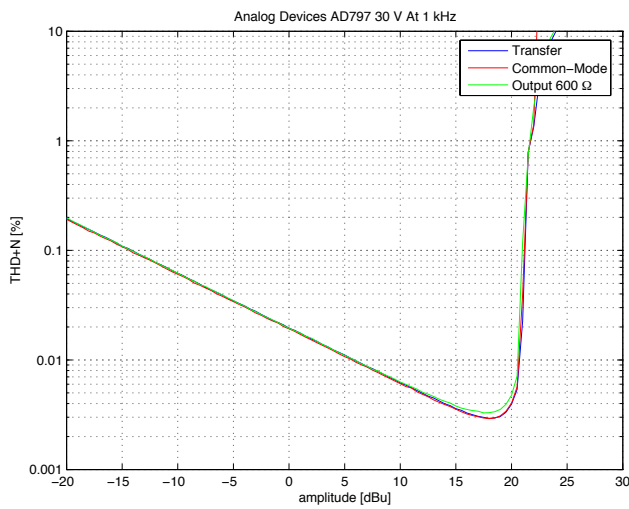
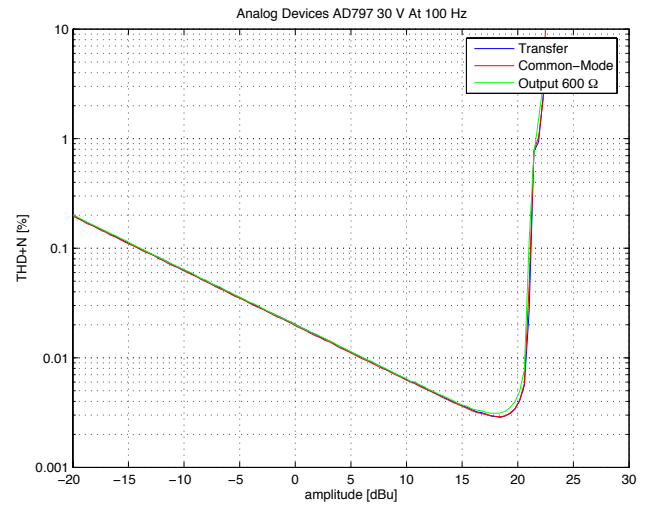
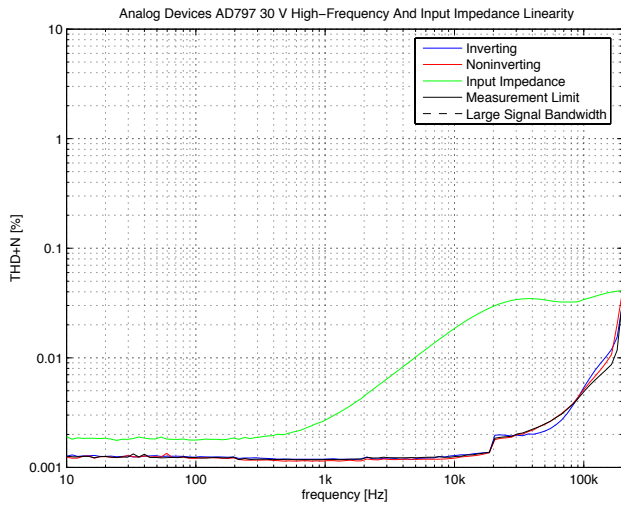
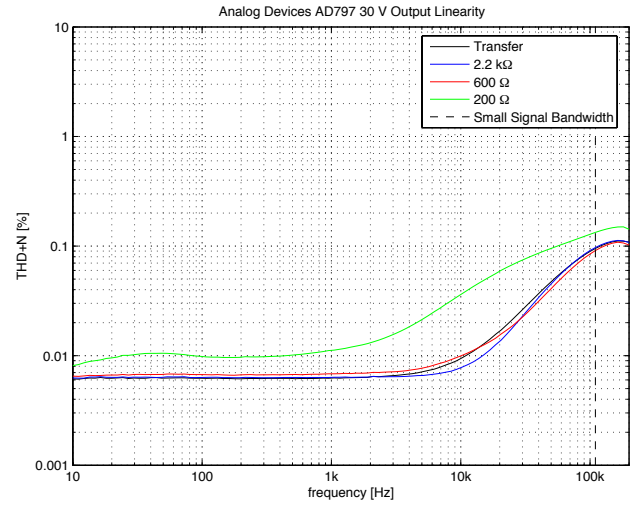
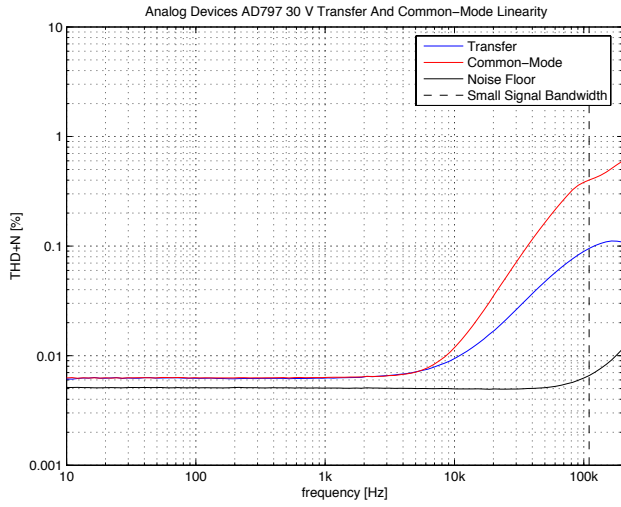
A single opamp with BJT input, based on a single-stage folded cascode topology with bootstrapped current mirror [13]. An external capacitor can be connected to cancel output stage distortion; for these measurements a 47 pF value has been used which is 3 pF lower than the value recommended in the datasheet.<sup>2</sup> In addition to this decompensation for higher noise gain configurations is possible as well. Stability is not easy to achieve—for voltage follower connections and capacitive feedback (e.g. integrators) a small resistor must be placed in series with the inverting input or the feedback capacitor as noted in the datasheet. 100  $\Omega$  has been used here for the non-inverting high-frequency linearity measurement. This amplifier offers very low voltage noise at the cost of higher than typical current noise and input bias currents.

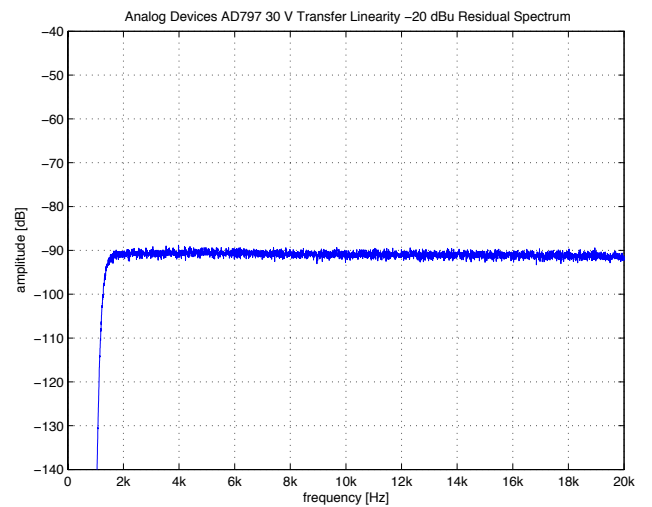
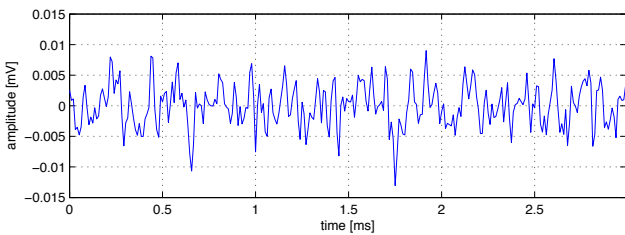
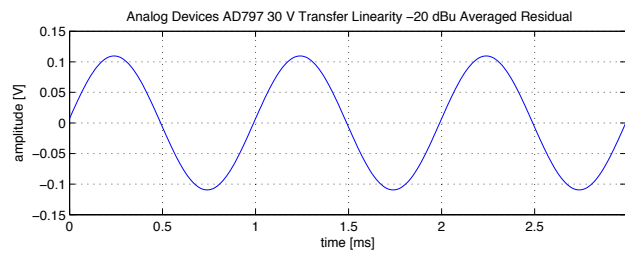
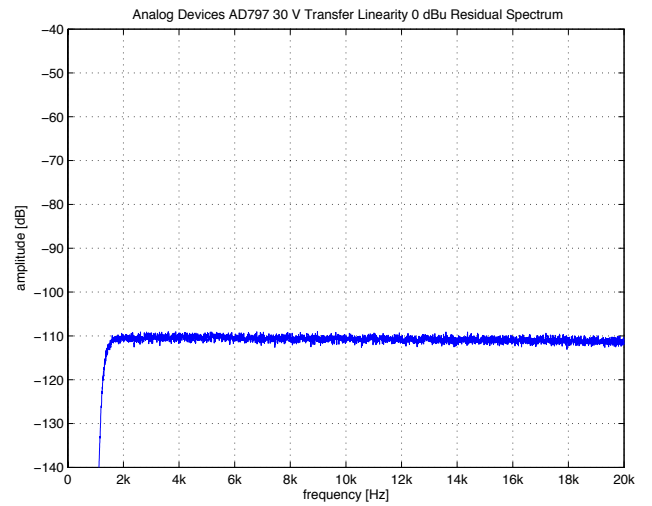
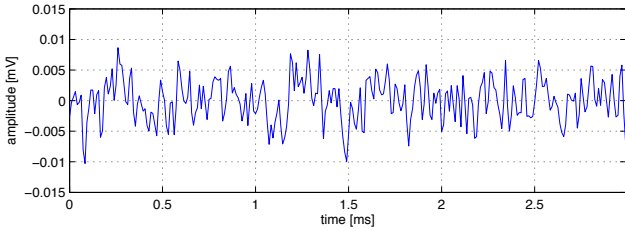
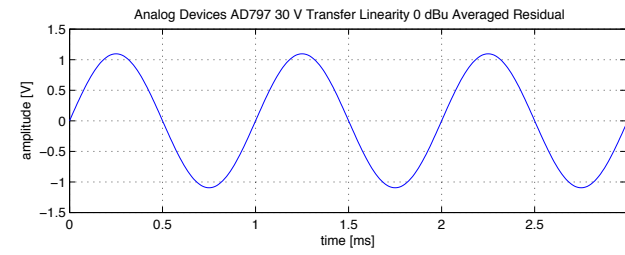
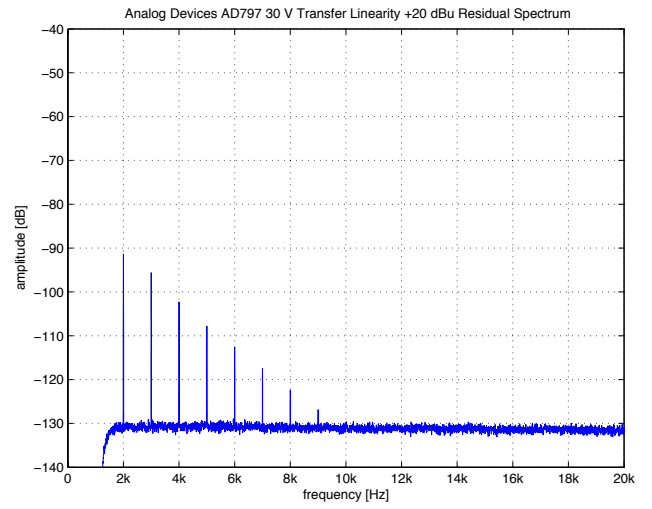
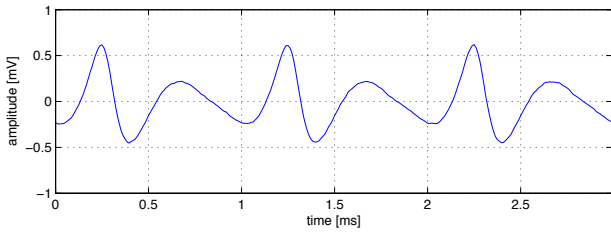
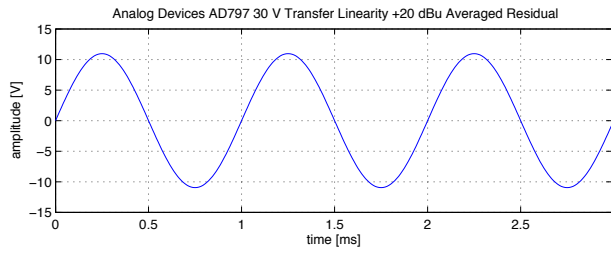
There are amplifiers which offer even better transfer linearity, but the AD797 is outstanding because all other distortion sources (with the exception of input impedance linearity) are carefully addressed such that they do not much degrade the transfer linearity. Output loading distortion is very well controlled and only significantly affects total harmonic distortion for a 200  $\Omega$  load; common-mode distortion becomes significant at the upper cor-

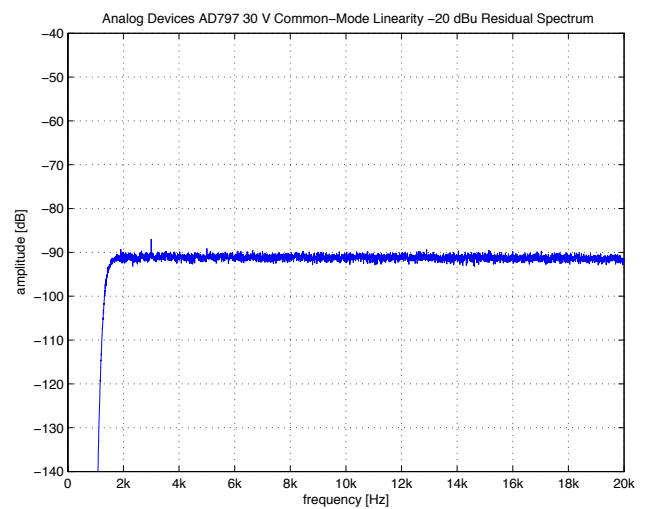
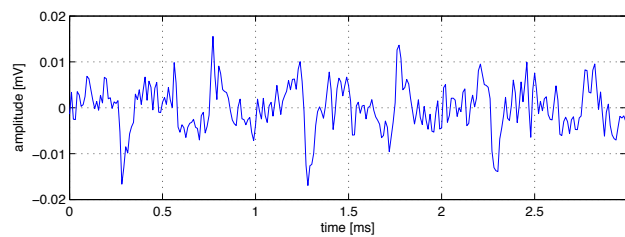
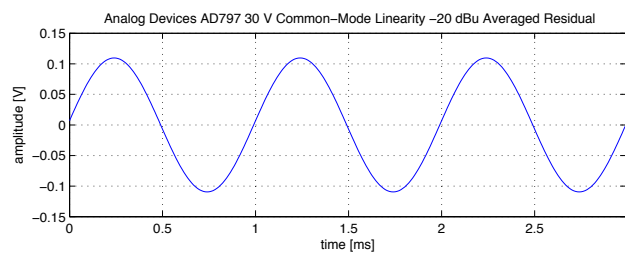
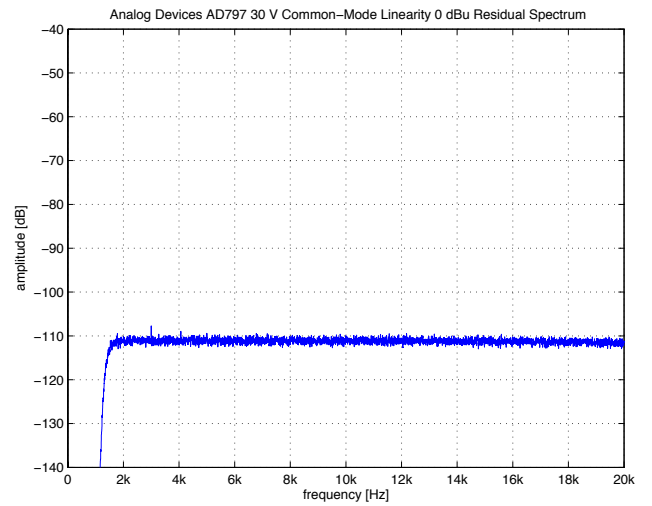
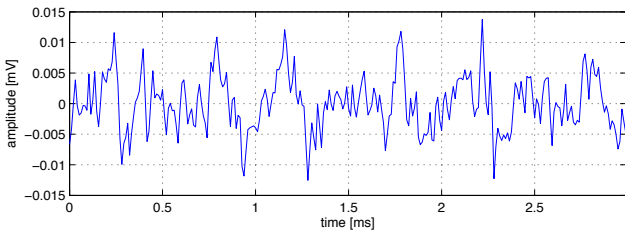
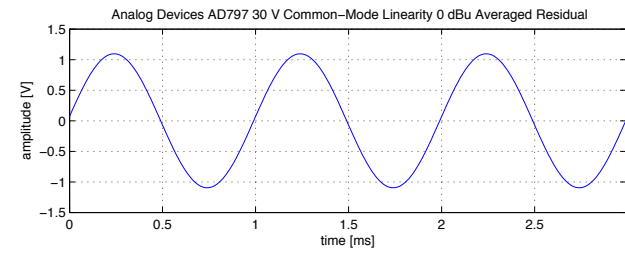
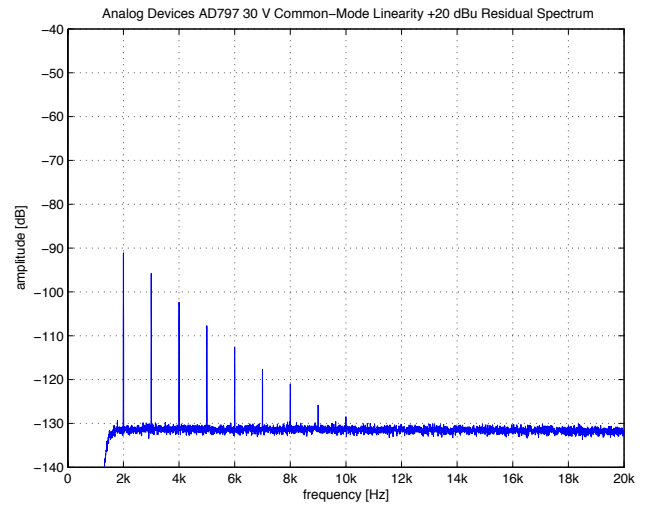
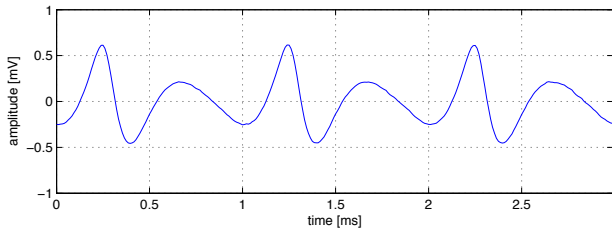
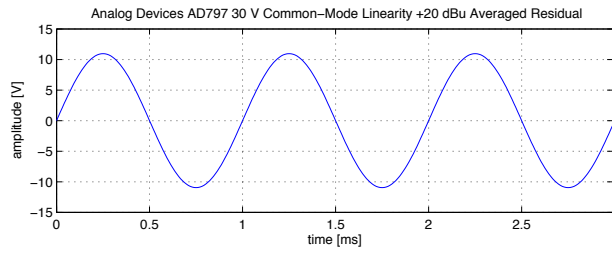
<sup>2</sup>It has not yet been verified whether this causes a measurable increase in distortion.

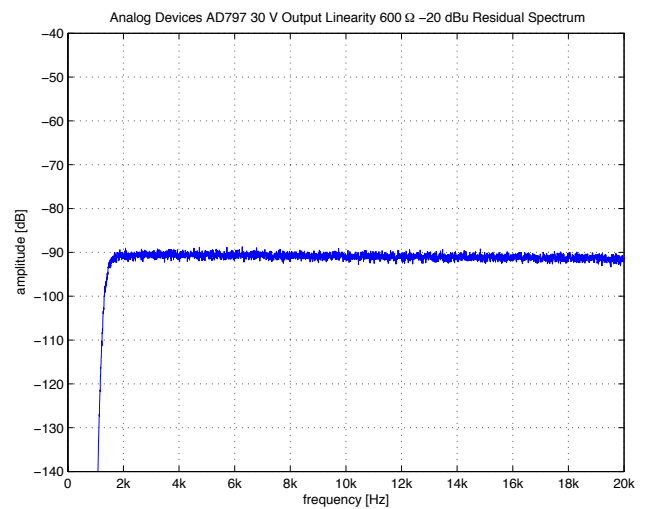
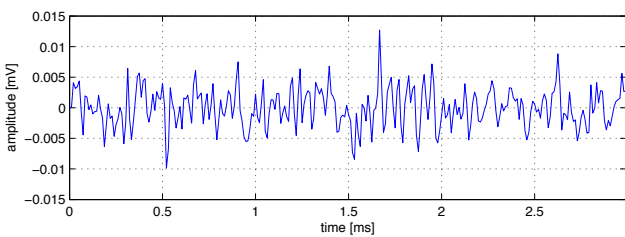
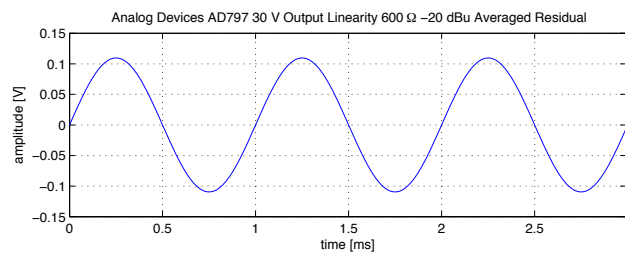
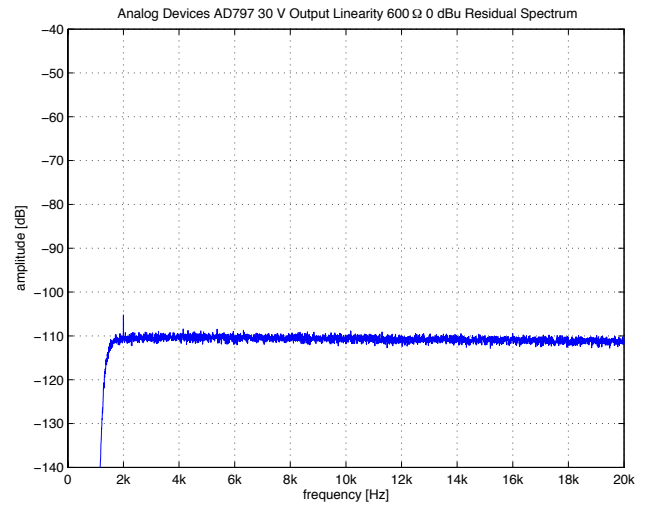
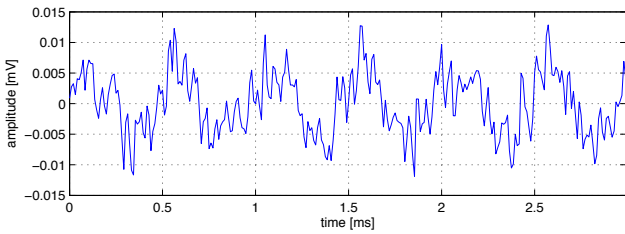
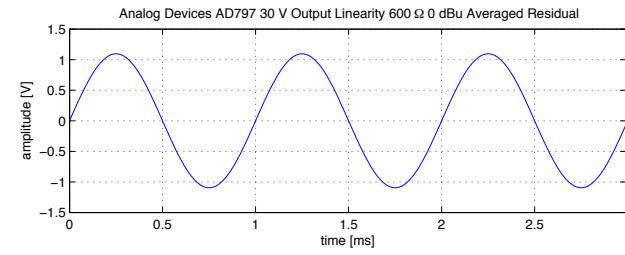
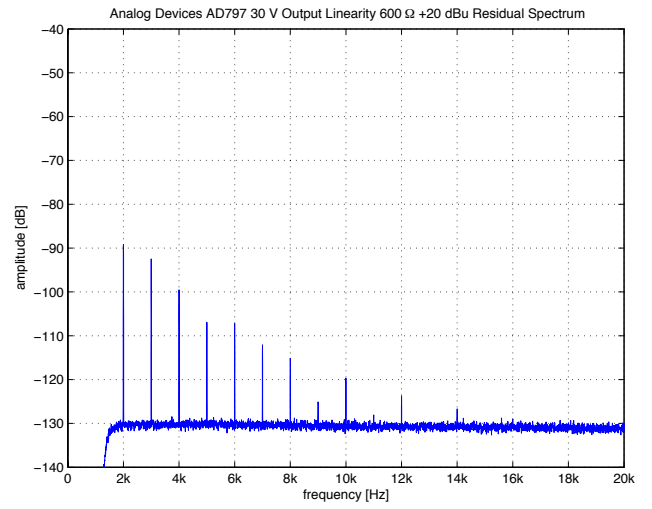
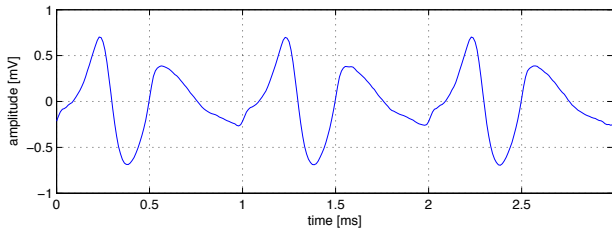
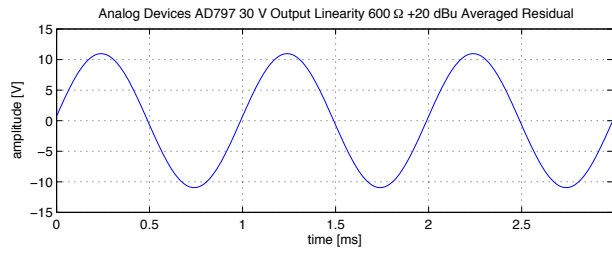
ner of the audio frequency range only and the input impedance linearity is above that typically observed for IC amplifiers (although it still is a major concern, particularly with the otherwise excellent characteristics of this amplifier). This leads to an amplifier with best overall distortion performance of all tested IC opamps—this has been verified by measuring a second amplifier with different date code, and the resulting performance was found to be consistent with the shown measurements. The signals visible in the 0 dBu and  $-20$  dBu FFT plots of the common-mode linearity appear to be interference.

An excellent choice for low distortion applications; not cheap though. And mind the input impedance modulation. . .











### 3.2 Analog Devices AD829

<b>Number of Channels</b>	1
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	2.75 US\$ at 1k units (July 2008)

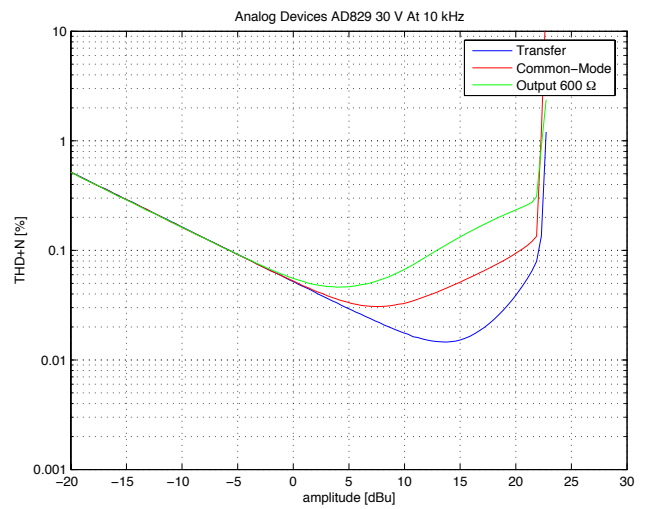
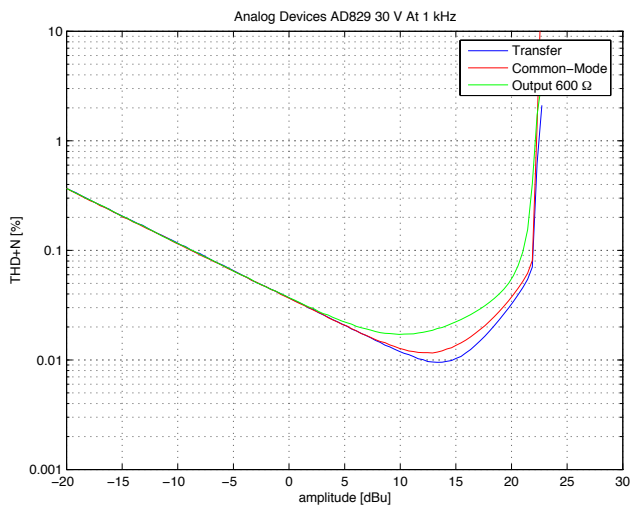
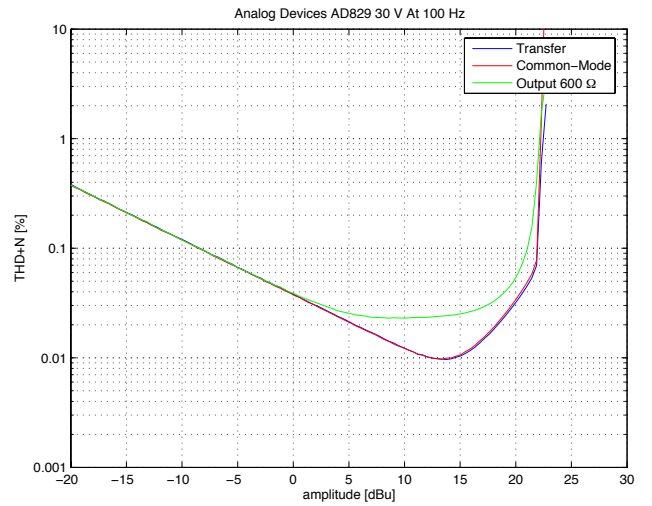
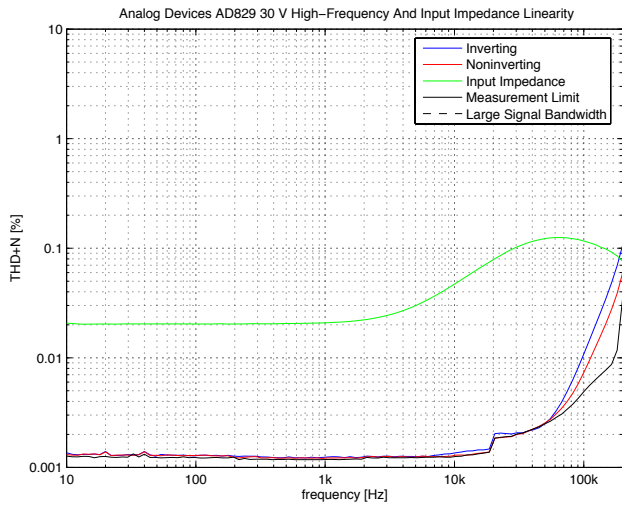
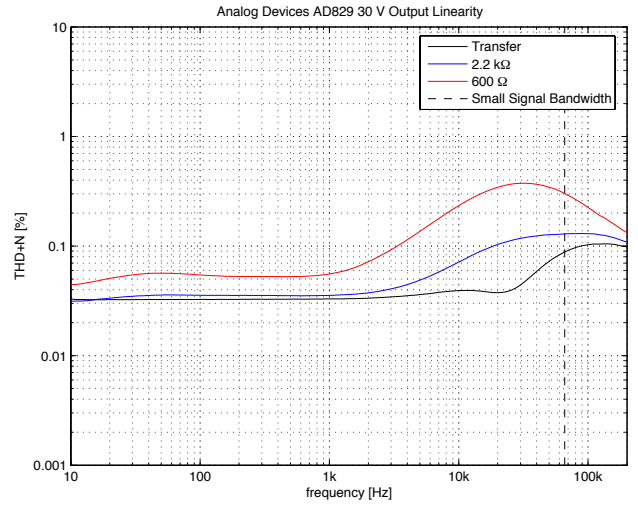
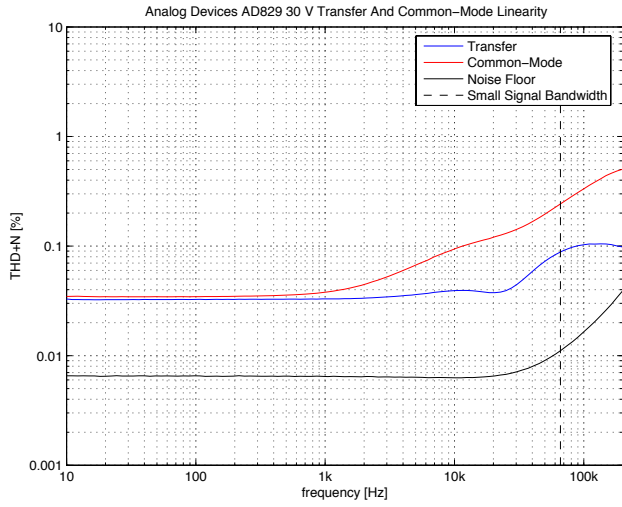
Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		0.2	1	mV
Input Bias Current		3.3	7	$\mu\text{A}$
Input Offset Current		50	500	nA
Gain Bandwidth Product		66		MHz
Slew-Rate		16		V/ $\mu\text{S}$
Input Voltage Noise (f = 1 kHz)		1.7	2	nV/ $\sqrt{\text{Hz}}$
Input Current Noise (f = 1 kHz)		1.5		pA/ $\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range		+14.3/-13.8		V
Output Voltage Swing ( $R_L = 1 \text{ k}\Omega$ )	$\pm 12$	$\pm 13.3$		V
Output Voltage Swing ( $R_L = 500 \Omega$ )	$\pm 10$	$\pm 12.2$		V
Output Current		$\pm 32$		mA
Power Supply Voltage	$\pm 4.5$		$\pm 18$	V
Quiescent Current per Amplifier		5	6.5	mA

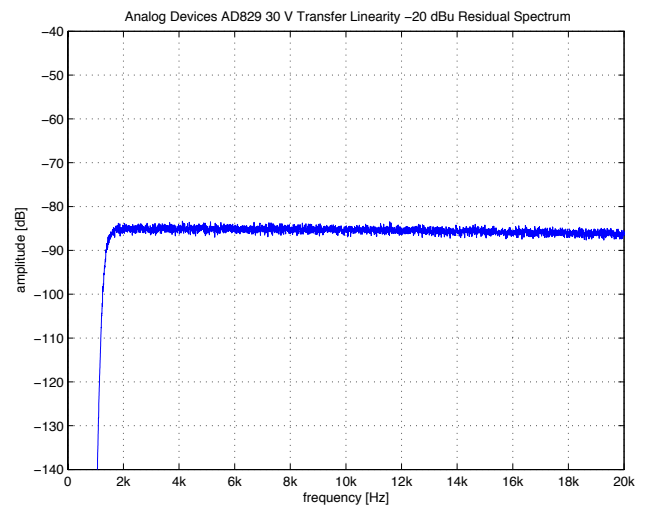
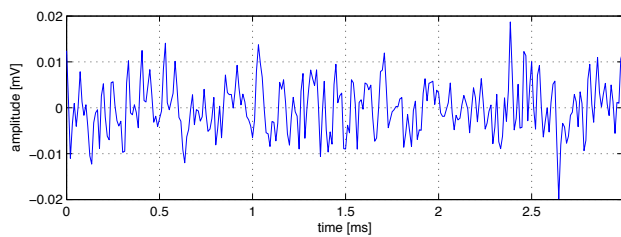
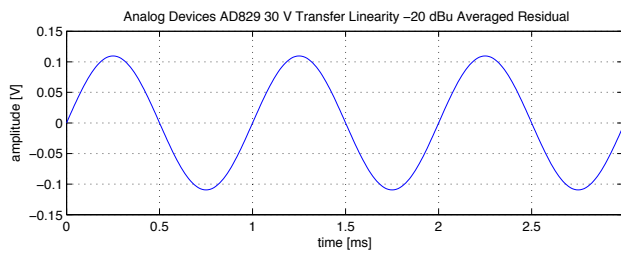
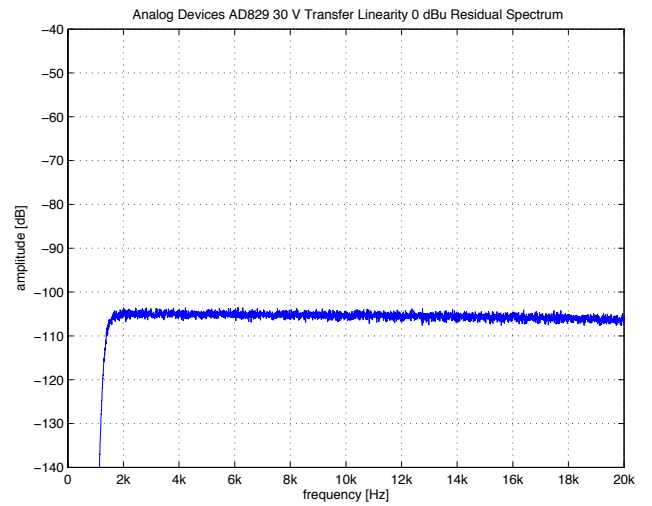
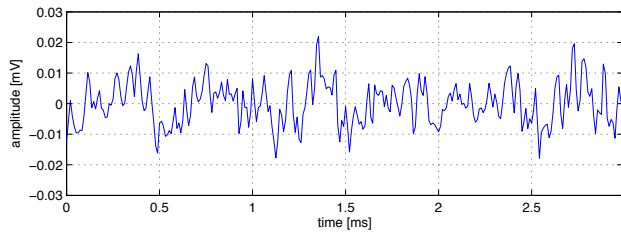
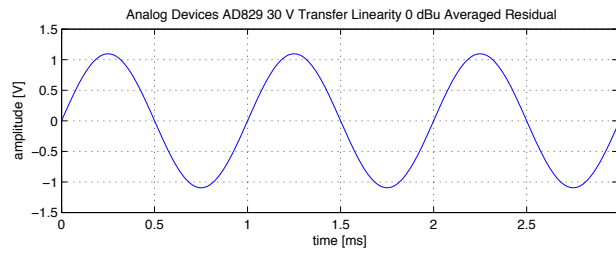
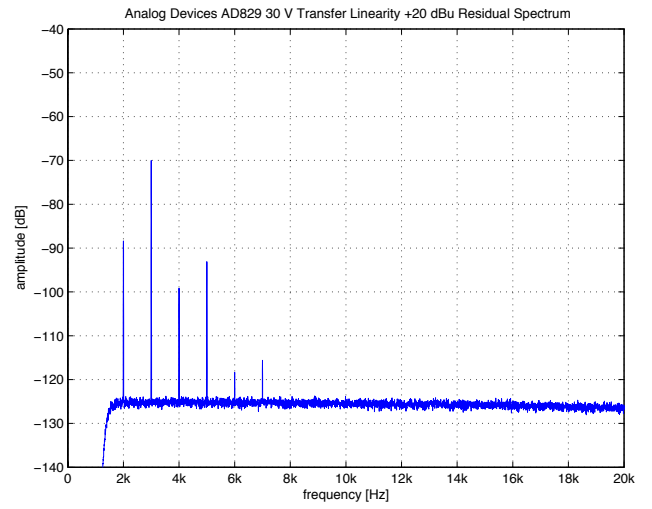
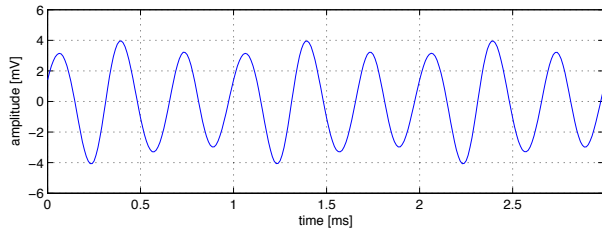
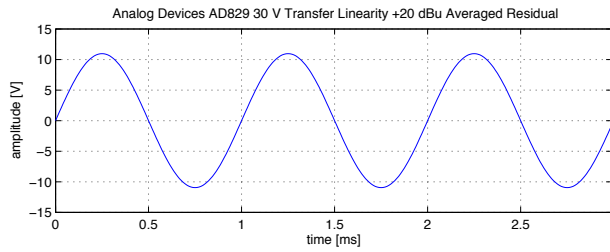
Table 3.2: Specifications for  $T_A = 25^\circ \text{C}$ ,  $V_S = \pm 15 \text{ V}$  and  $C_{\text{COMP}} = 68 \text{ pF}$ .

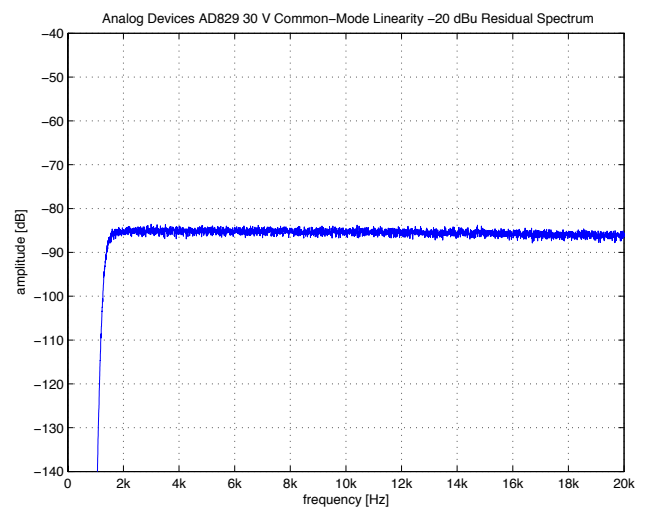
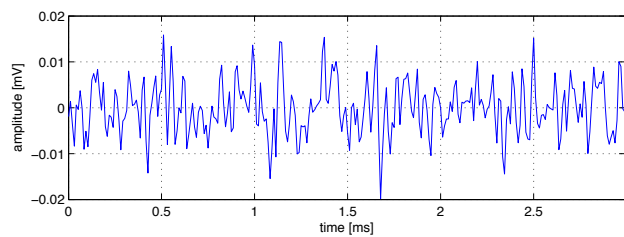
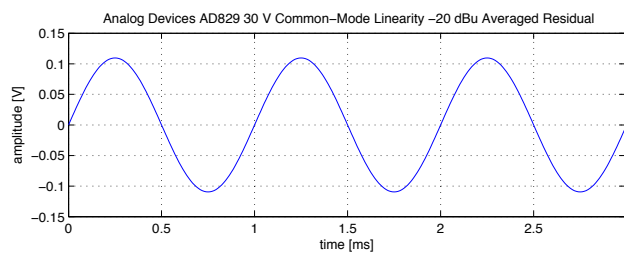
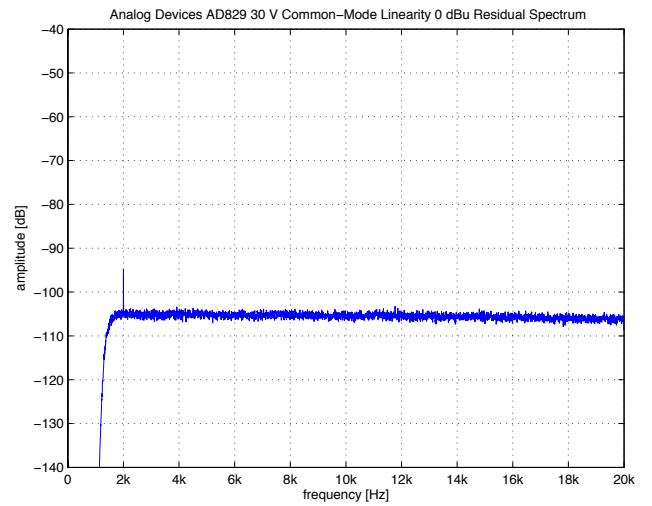
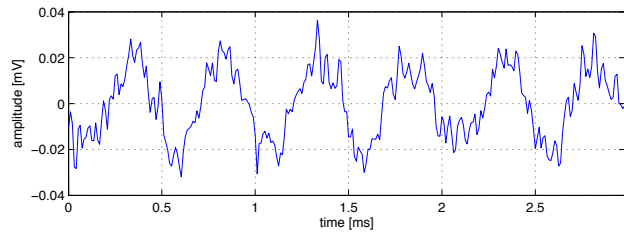
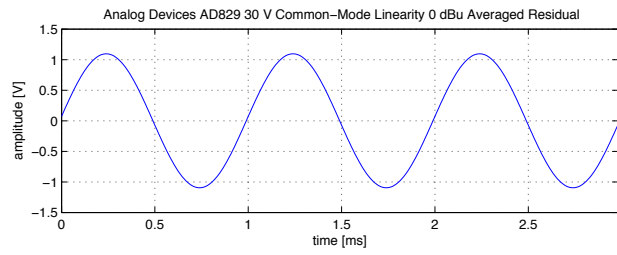
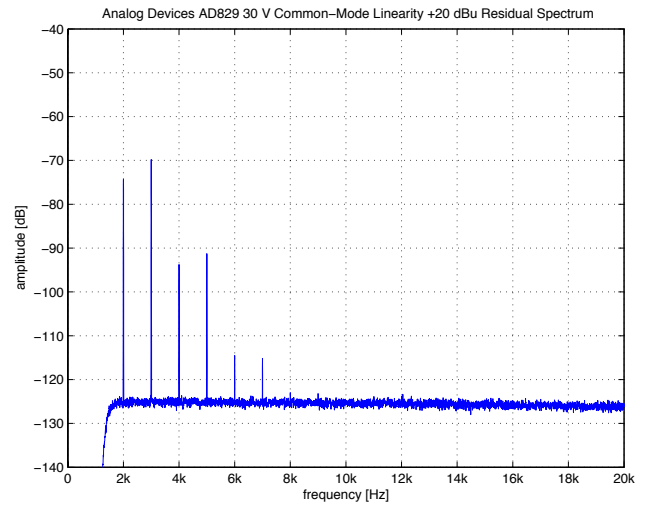
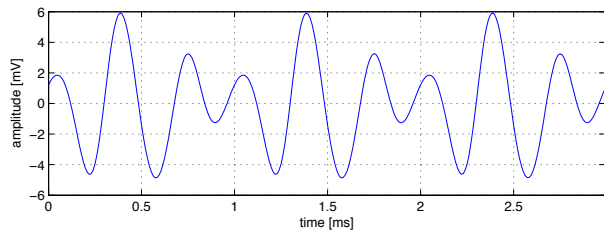
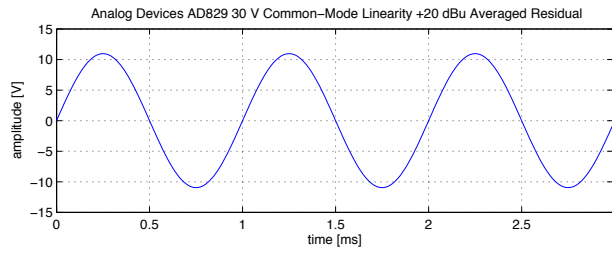
A single opamp intended mainly for video use. Based on a single-stage folded cascode architecture with BJT inputs and external compensation, tested here with unity gain compensation. This amplifier has relatively low voltage noise, at the cost of high current noise and very high input bias currents.

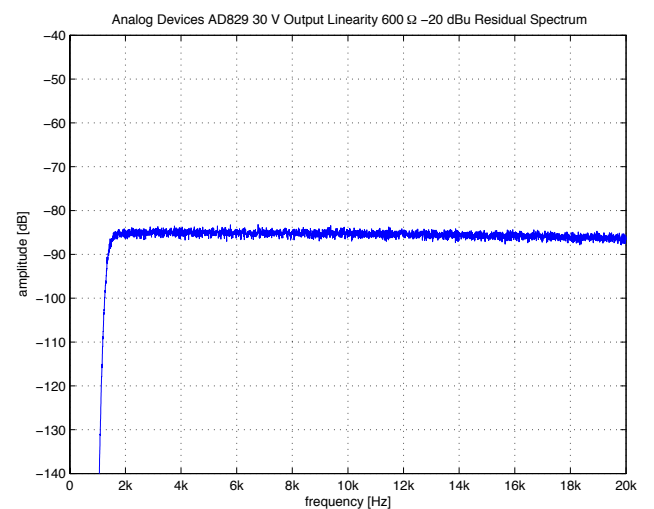
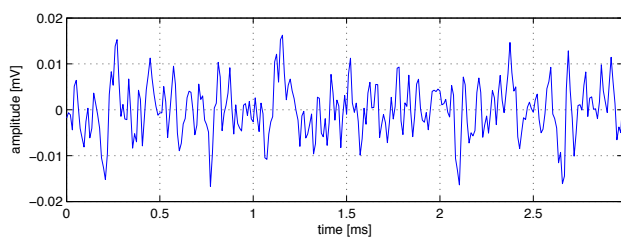
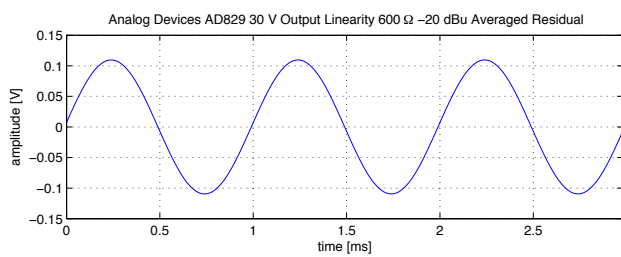
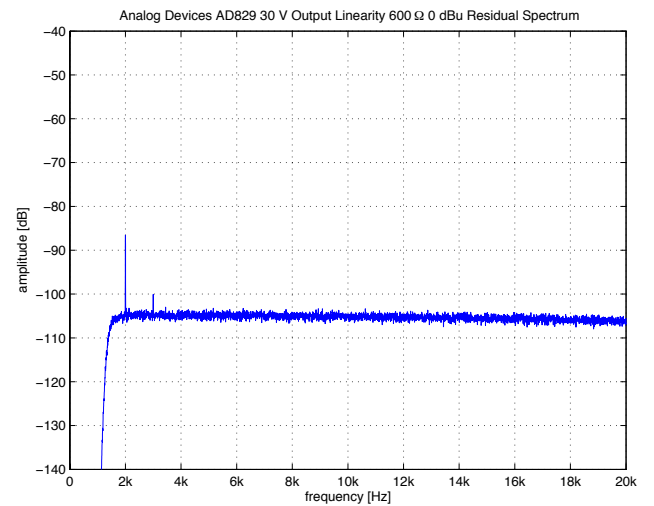
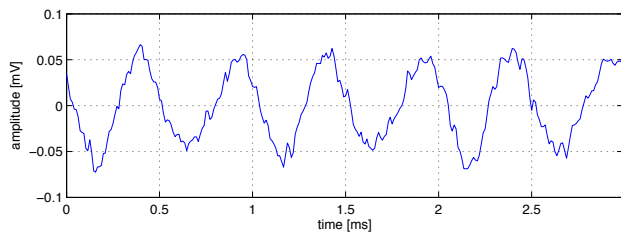
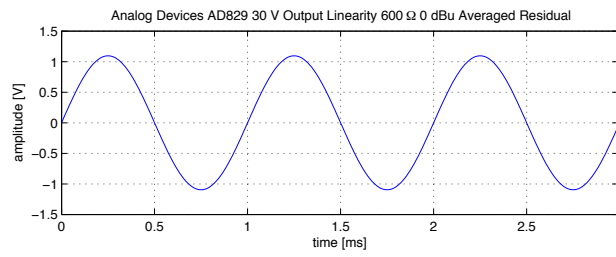
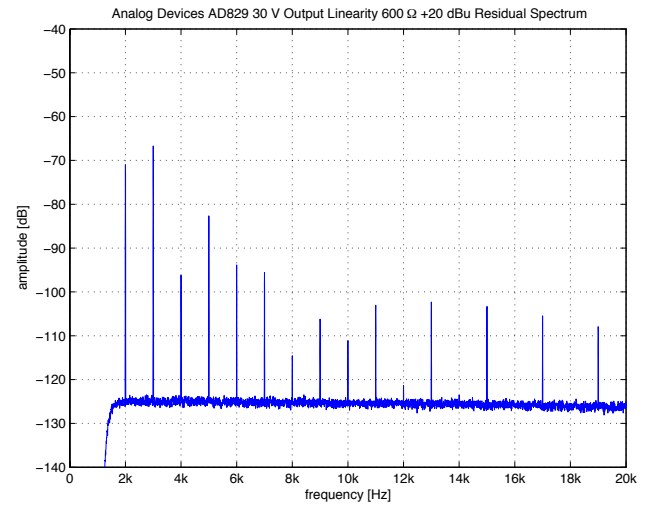
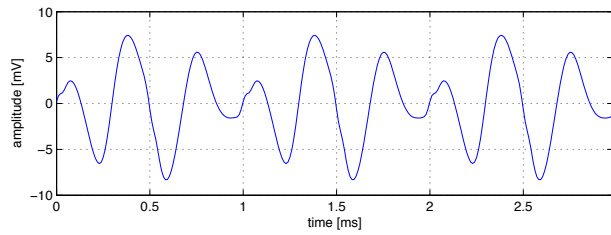
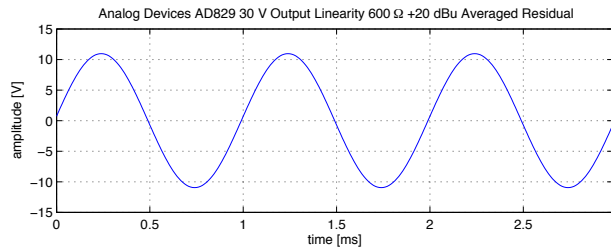
Basic transfer linearity is modestly good only but at least shows little increase within the audio frequency range, although some milde slew-induced distortion at higher frequencies is noticeable. Common-mode distortion is present but causes little increase in total harmonic distortion at low frequencies as it is masked by the dominant 3<sup>rd</sup> harmonic of the transfer linearity; input impedance linearity is poor down to low frequencies. Output loading causes a substantial increase in distortion at higher frequencies which is present at lower levels as well. Some low-frequency thermal effects which cancel other distortion contributions are visible.

Perhaps a part to be considered for higher noise gain applications where the external compensation helps optimising high-frequency loop gain and common-mode distortion is less troublesome. For lower noise gains other parts seem to be more suitable at lower cost. Care to output loading effects needed.









### 3.3 Analog Devices OP275

<b>Number of Channels</b>	1
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	0.99 US\$ at 1k units (July 2008)

Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage			1	mV
Input Bias Current		100	350	nA
Input Offset Current		2	50	nA
Gain Bandwidth Product		9		MHz
Slew-Rate	15	22		V/ $\mu$ S
Input Voltage Noise (f = 1 kHz)		6		nV/ $\sqrt{\text{Hz}}$
Input Current Noise (f = 1 kHz)		1.5		pA/ $\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 10.5$			V
Output Voltage Swing ( $R_L = 2 \text{ k}\Omega$ )	$\pm 13.5$	$\pm 13.9$		V
Power Supply Voltage	$\pm 4.5$		$\pm 22$	V
Quiescent Current per Amplifier		4	5	mA

Table 3.3: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 15 \text{V}$ .

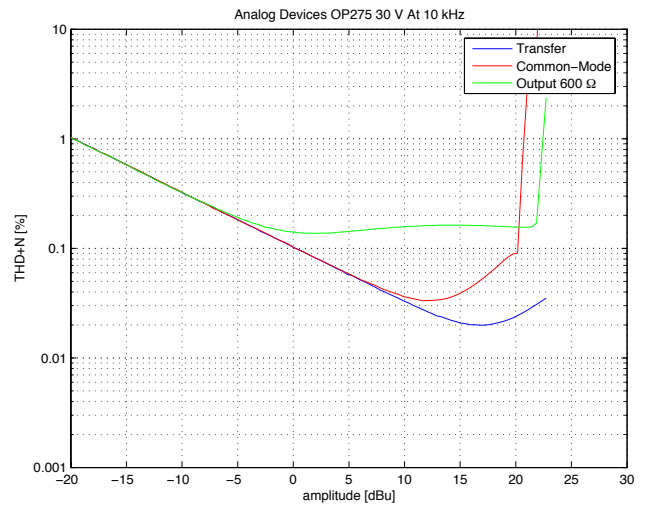
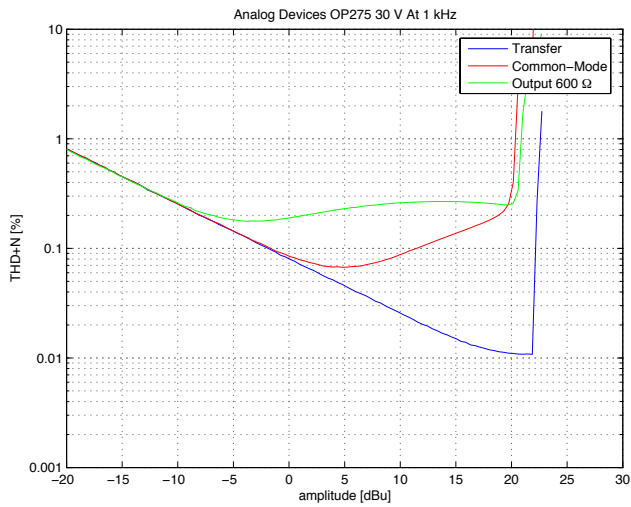
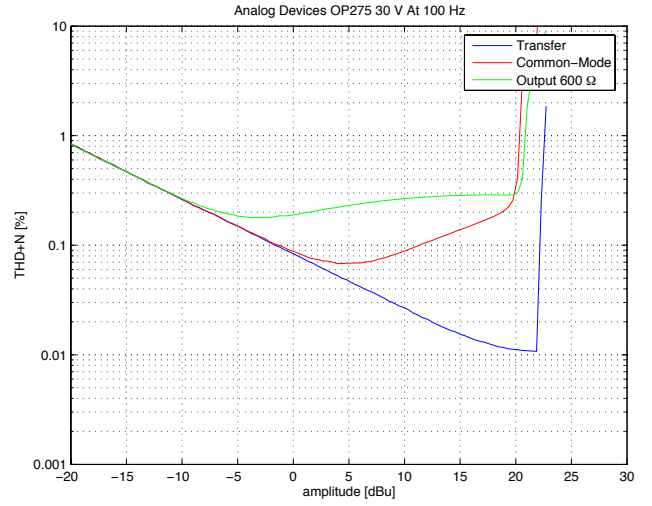
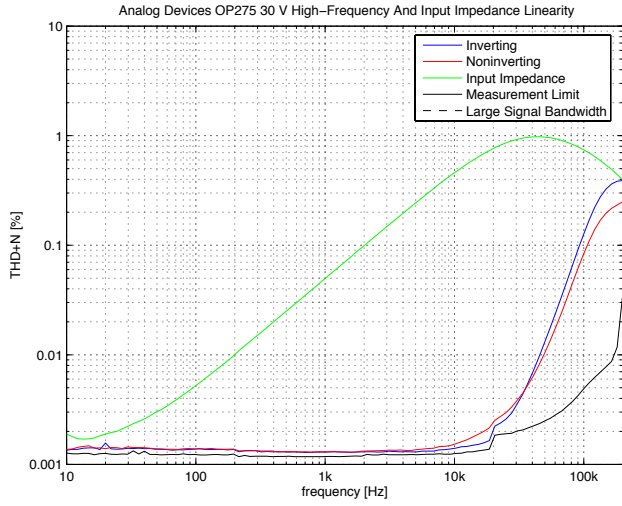
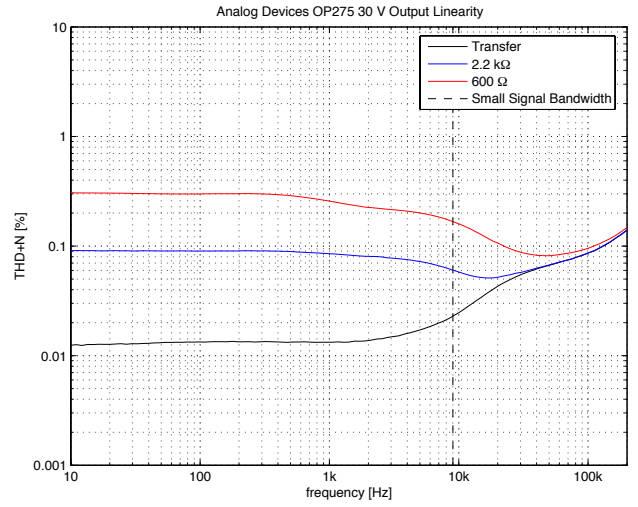
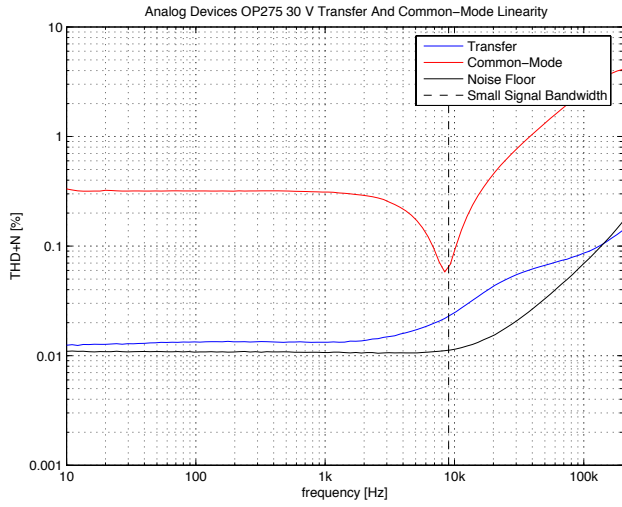
A dual opamp using a two-stage architecture with a BJT/JFET composite input stage which is supposed to improve the slew-rate of the amplifier. Current noise is very high considering the medium voltage noise performance.

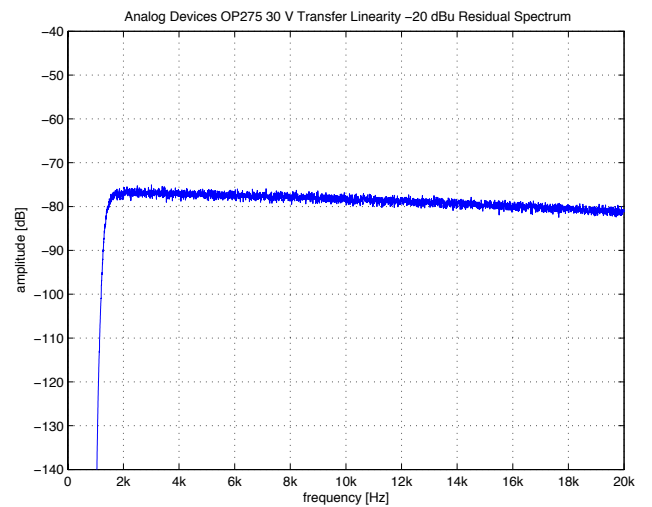
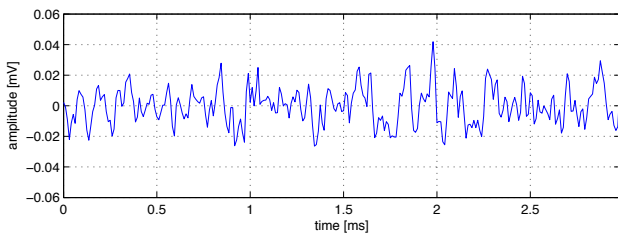
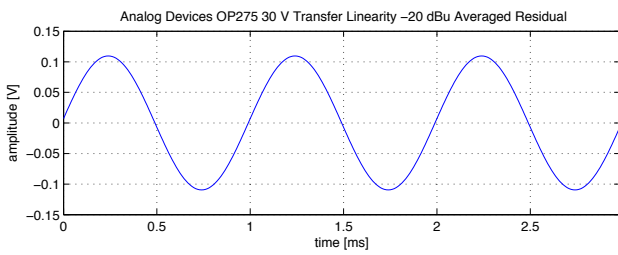
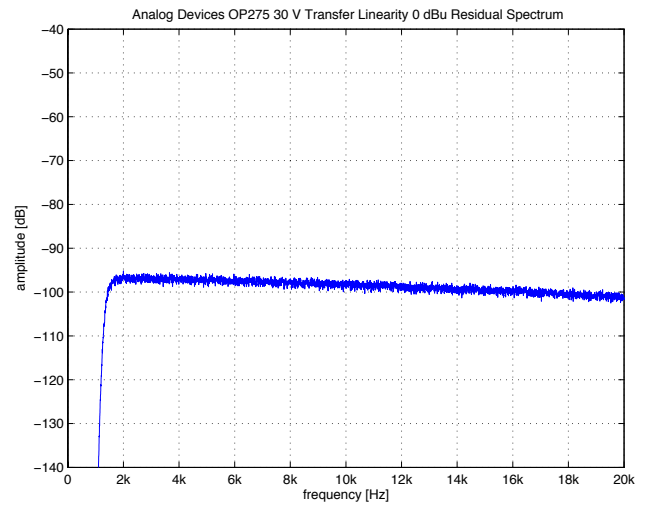
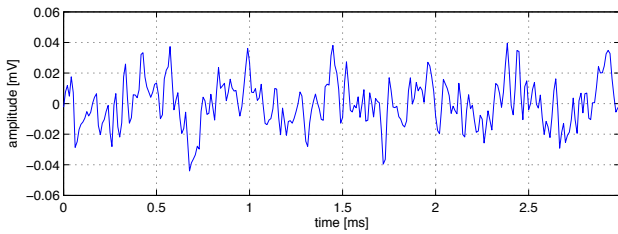
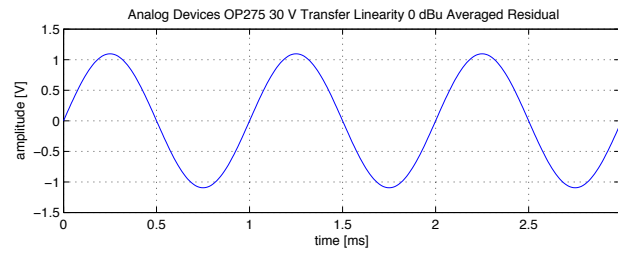
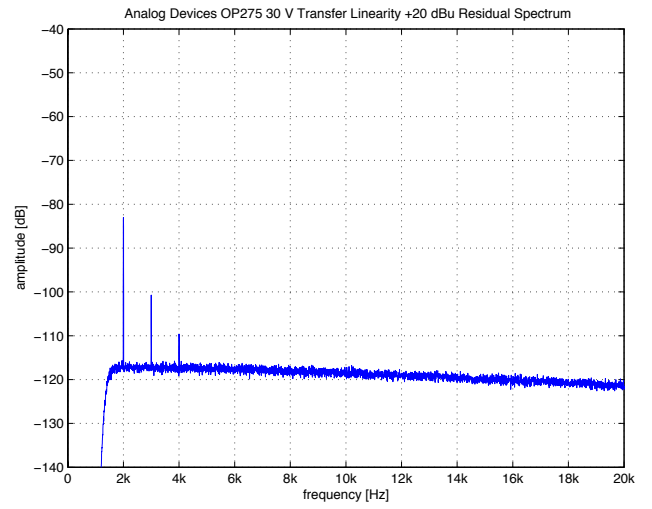
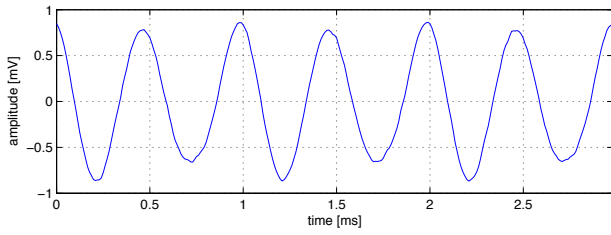
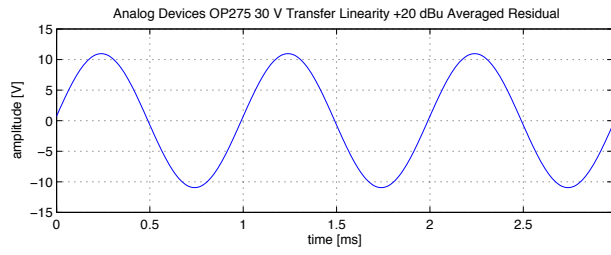
The transfer linearity of the amplifier is relatively good, up to medium frequencies. At higher frequencies the linearity degrades although the slew-rate is high.<sup>3</sup> Common-mode, input impedance and output linearity is very poor; one wonders why the datasheet claims low distortion for this part.

Well, at that cost there seem to be more suitable amplifiers out there if low distortion is asked for.

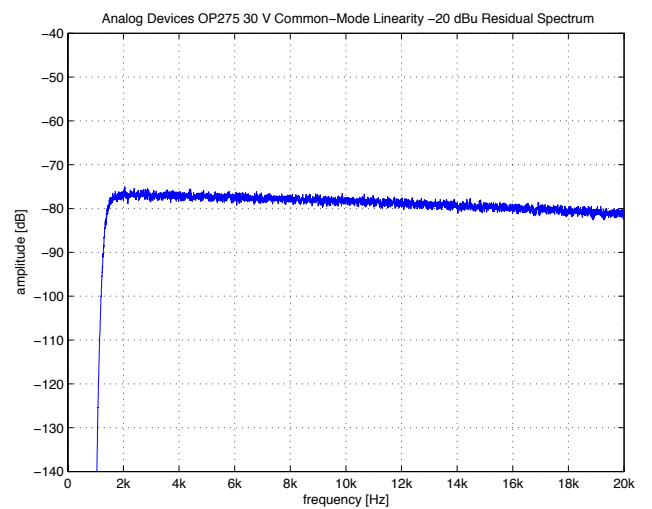
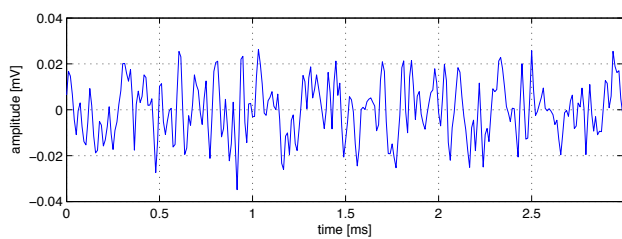
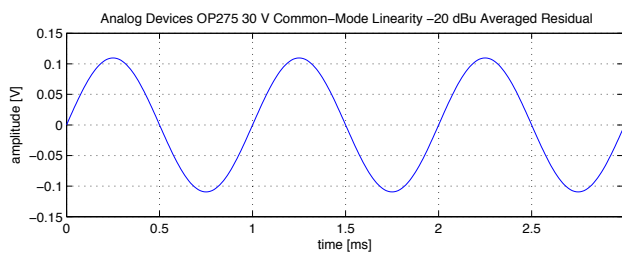
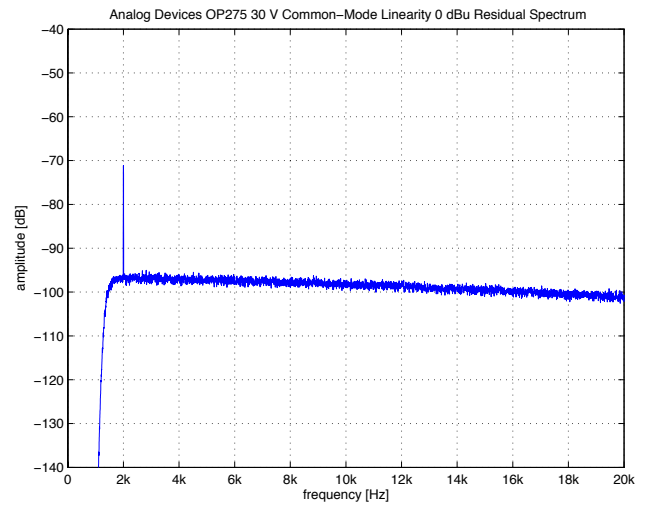
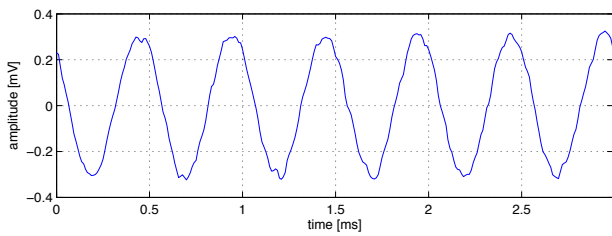
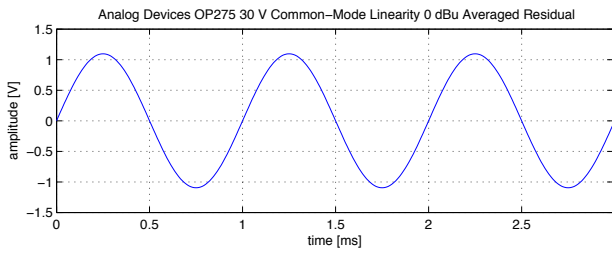
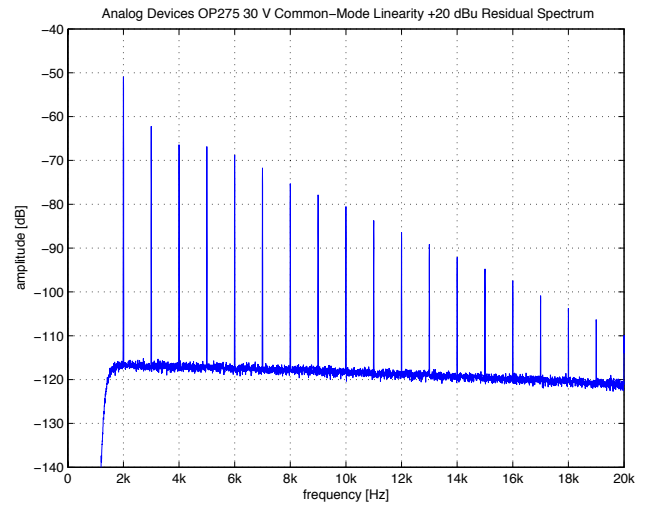
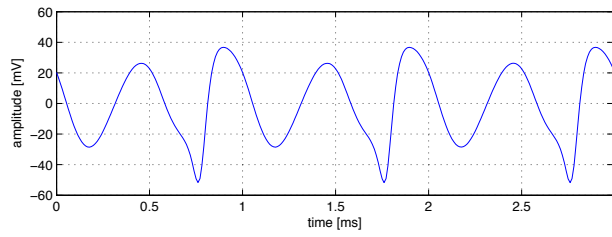
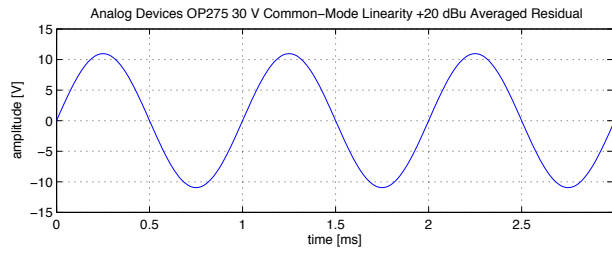
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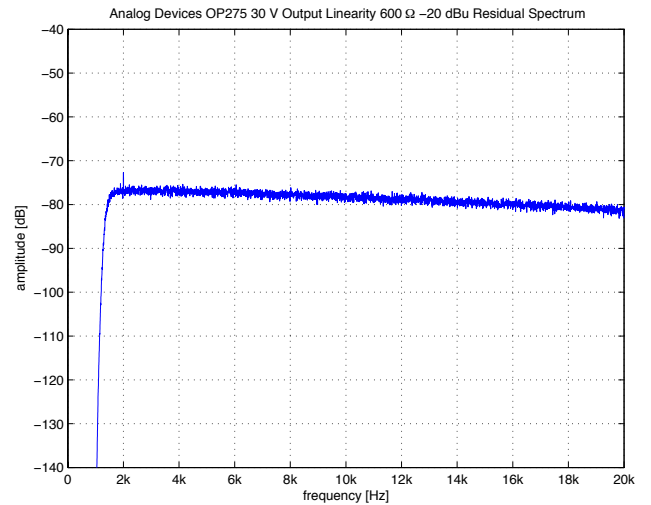
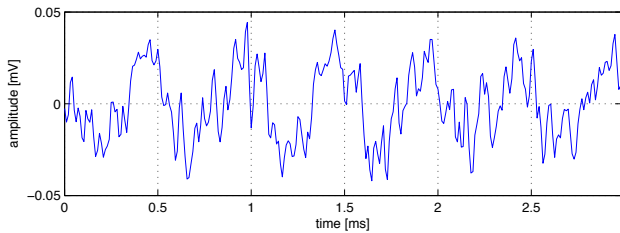
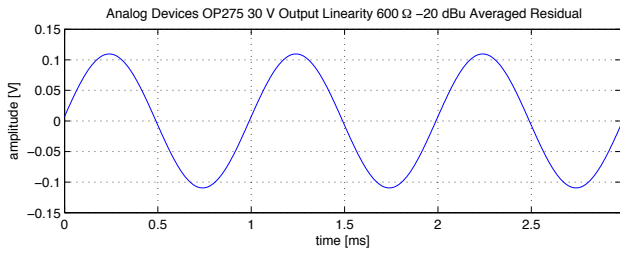
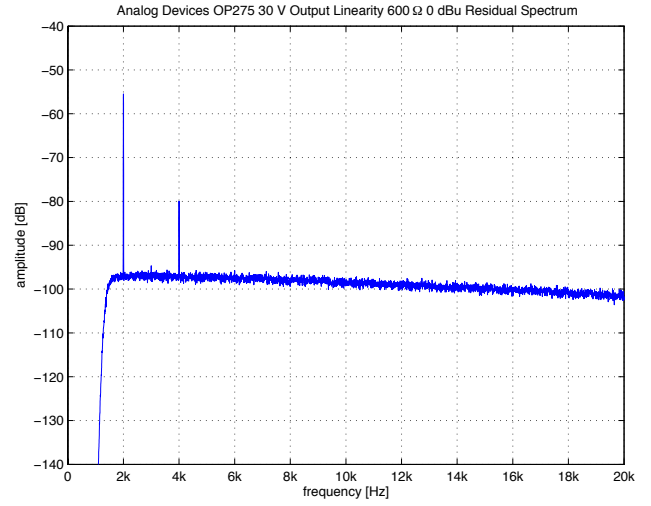
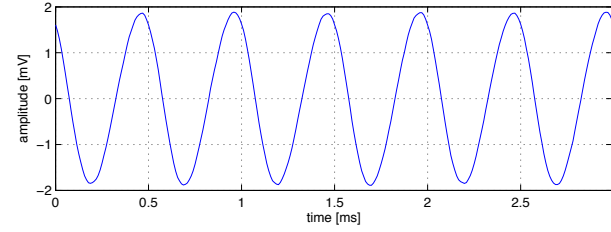
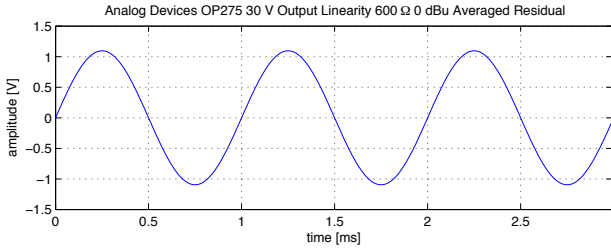
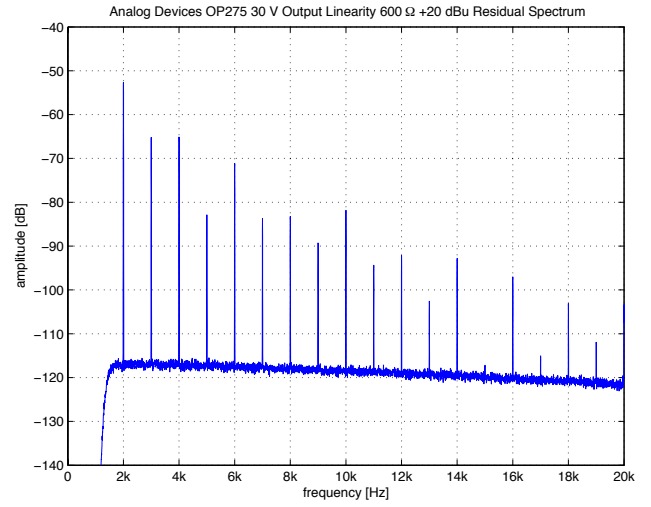
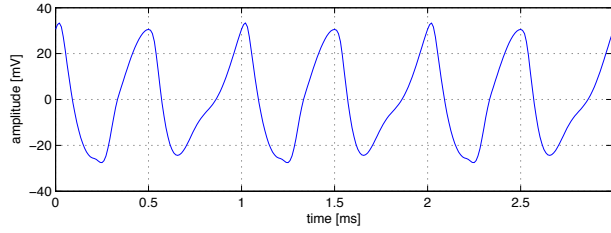
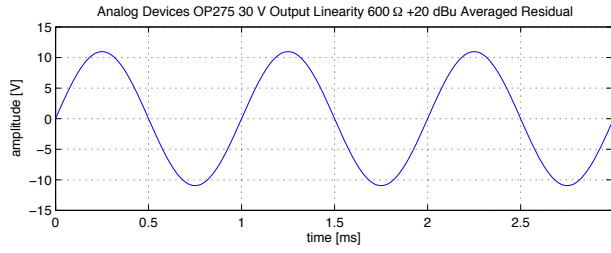
<sup>3</sup>This is a typical result for slew-enhanced input stages—which the used composite topology essentially is.

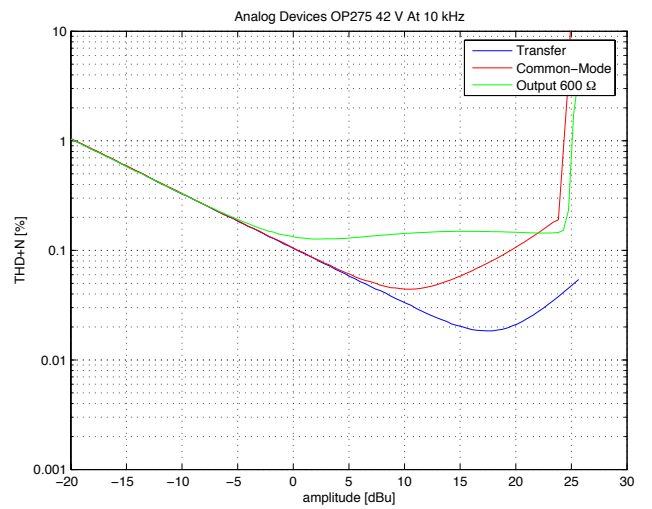
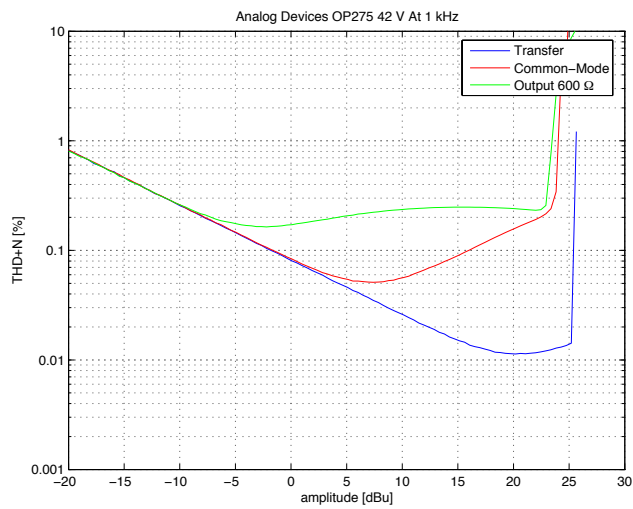
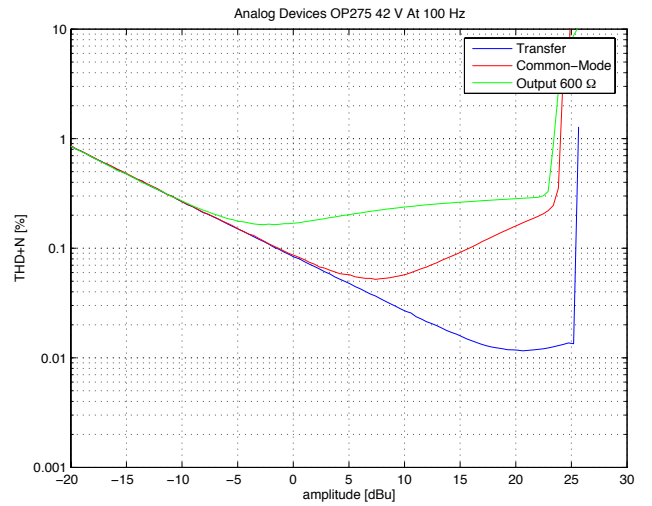
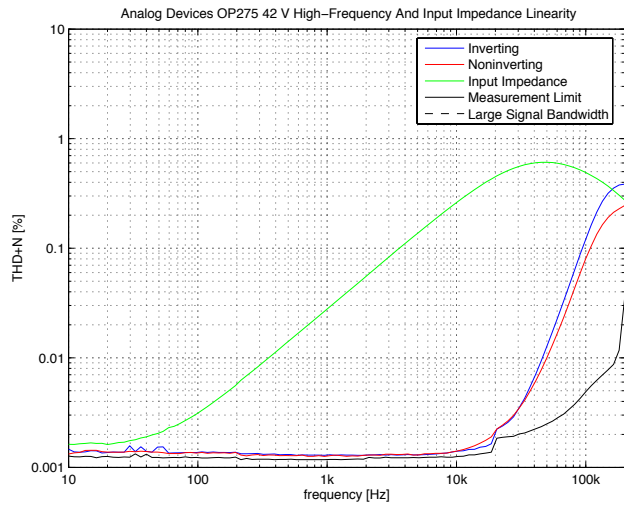
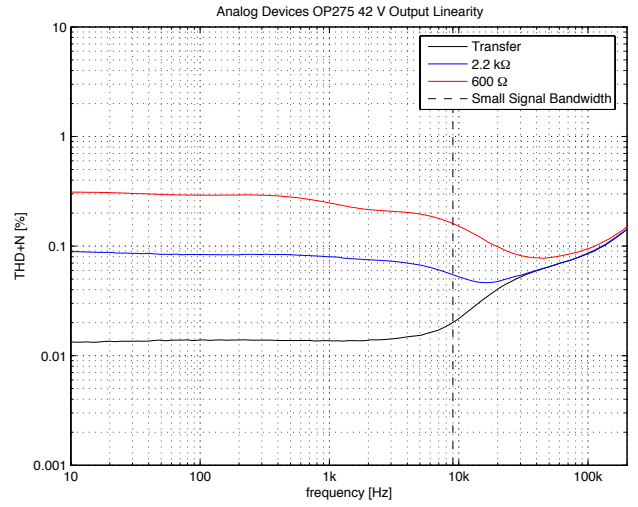
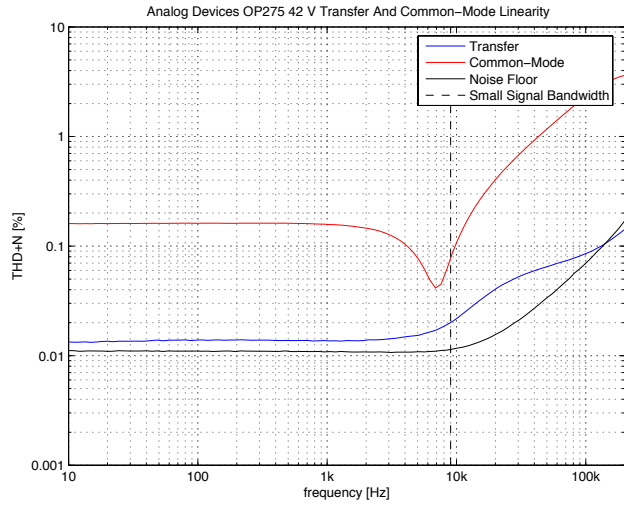


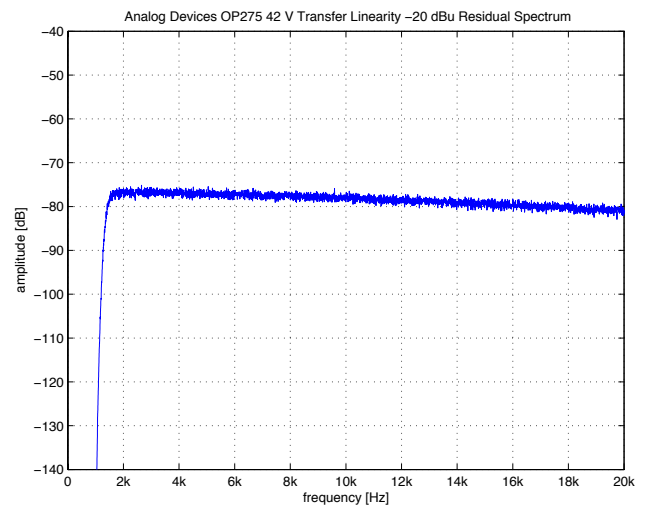
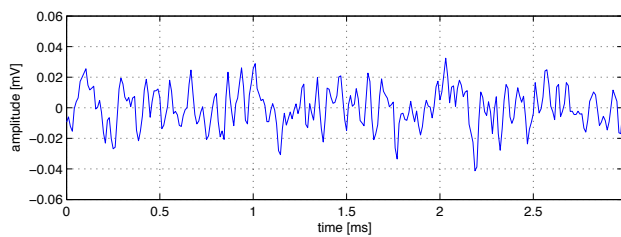
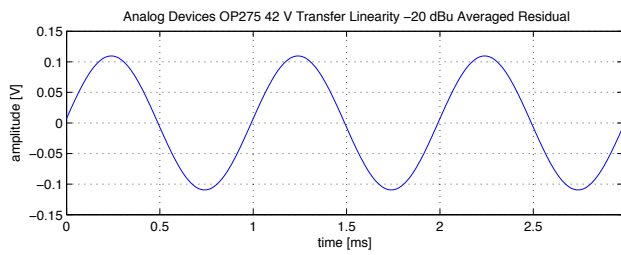
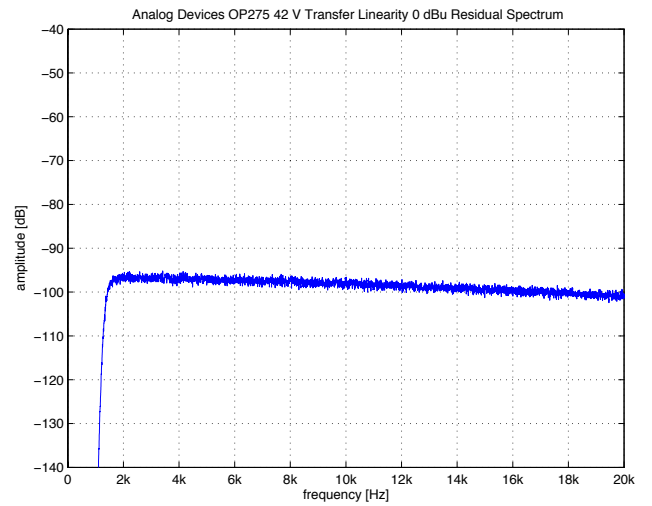
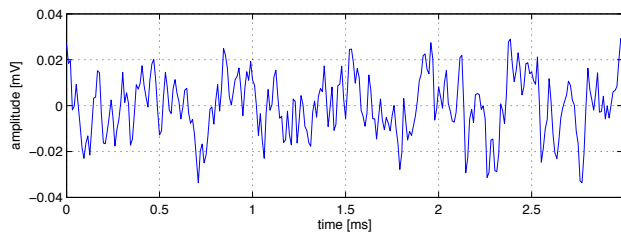
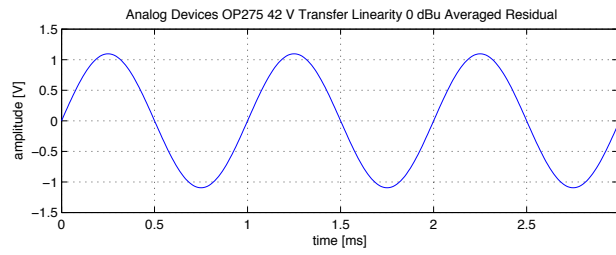
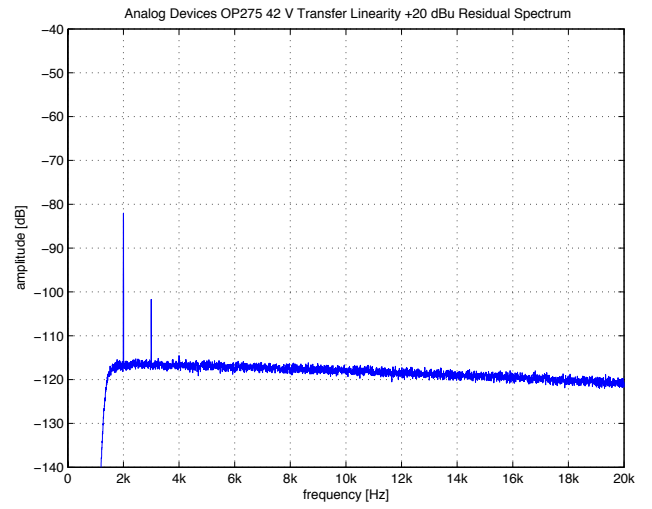
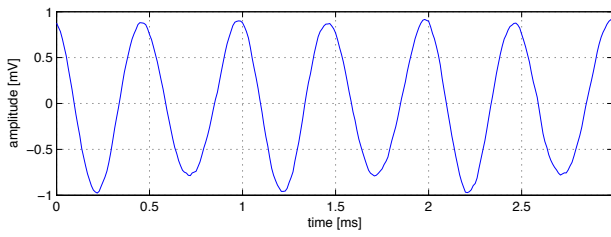
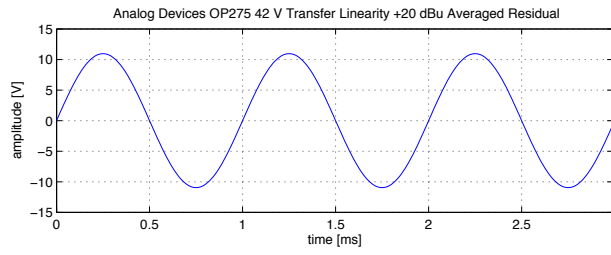


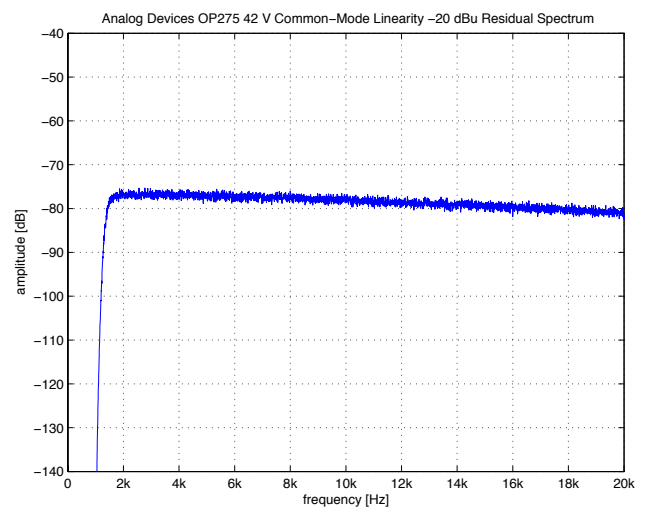
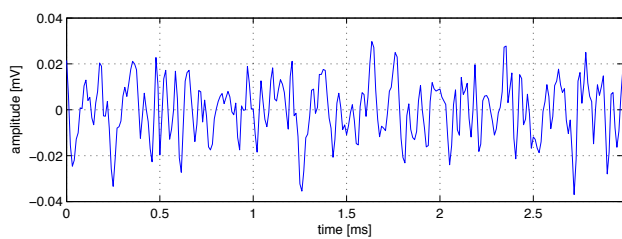
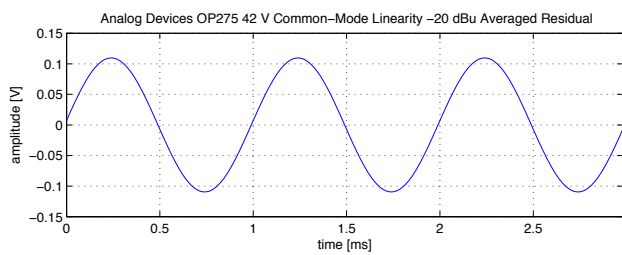
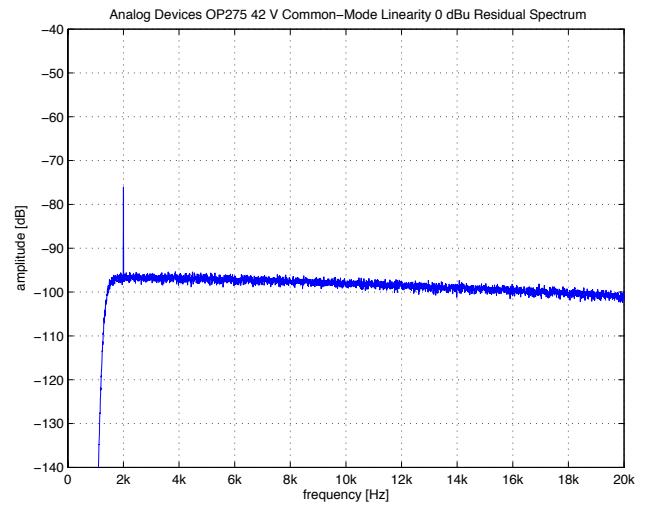
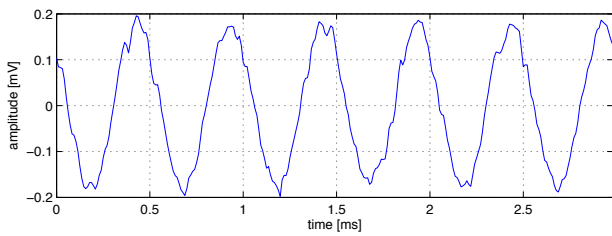
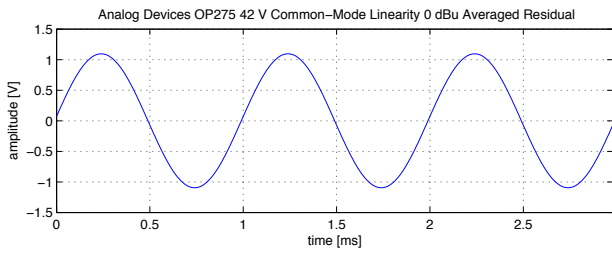
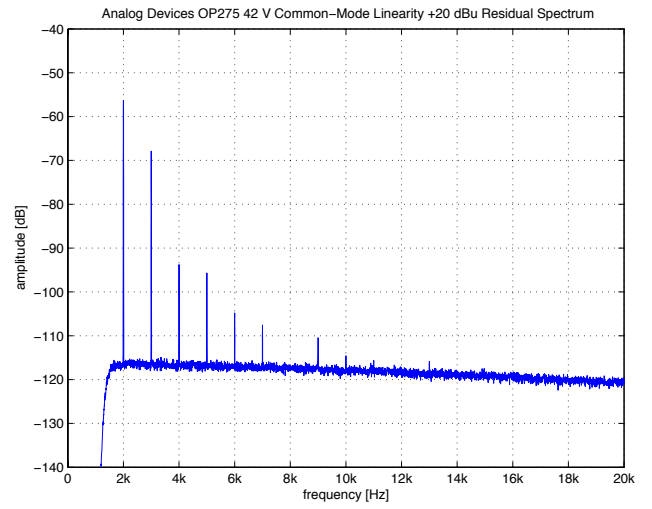
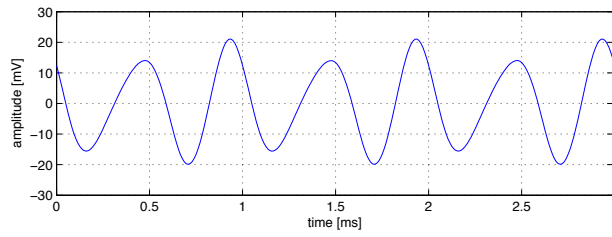
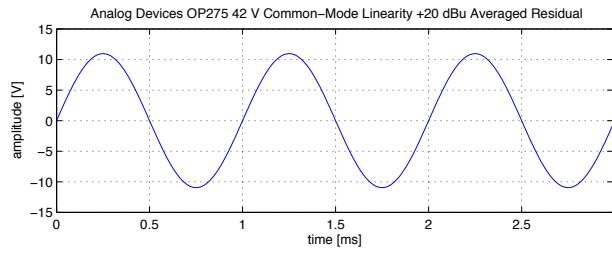


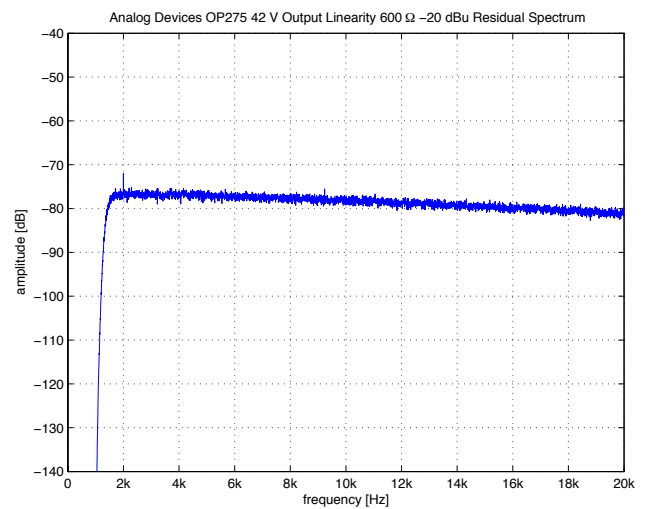
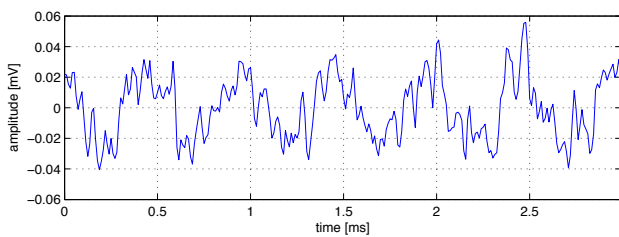
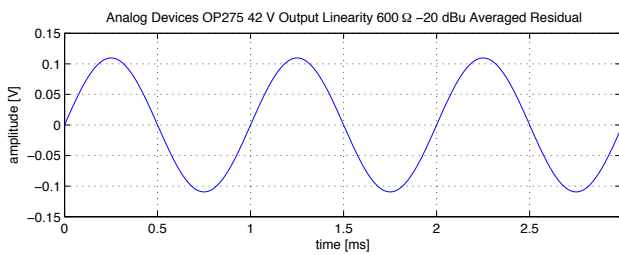
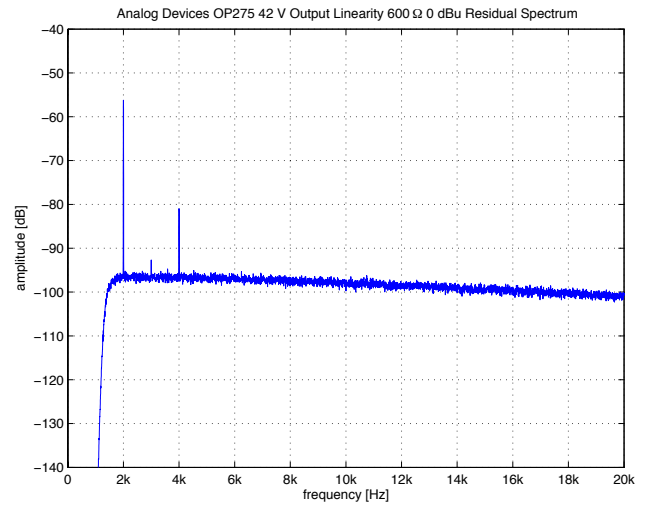
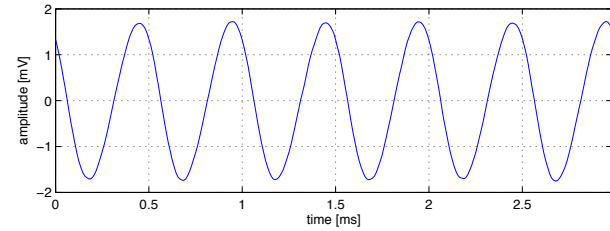
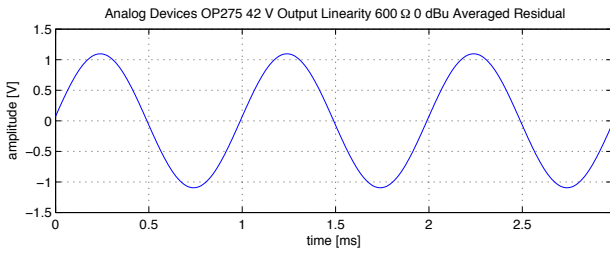
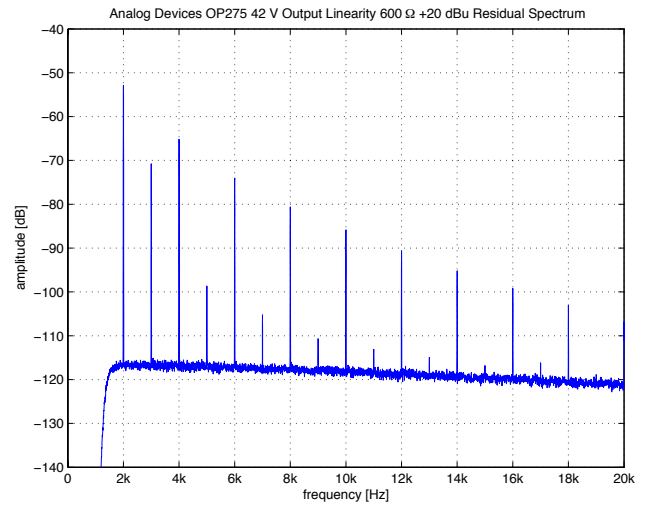
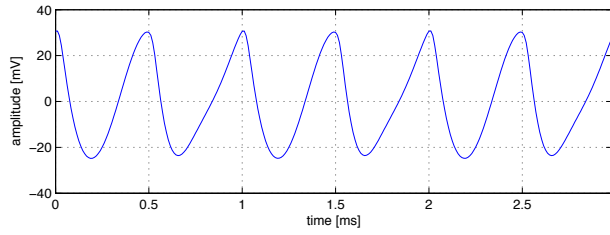
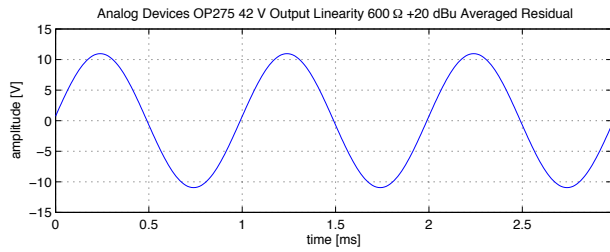












### 3.4 Analog Devices OP471

<b>Number of Channels</b>	4
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	1.23 US\$ at 1k units (August 2008)

Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		1	1.8	mV
Input Bias Current		25	60	nA
Input Offset Current		12	30	nA
Gain Bandwidth Product		6.5		MHz
Slew-Rate	6.5	8		V/ $\mu$ S
Input Voltage Noise (f = 1 kHz)		6.5	11	nV/ $\sqrt{\text{Hz}}$
Input Current Noise (f = 1 kHz)		0.4		pA/ $\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 11$	$\pm 12$		V
Output Voltage Swing ( $R_L = 2 \text{ k}\Omega$ )	$\pm 12$	$\pm 13$		V
Power Supply Voltage	$\pm 5$		$\pm 18$	V
Quiescent Current per Amplifier		2.3	2.75	mA

Table 3.4: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 15 \text{V}$ .

A quad amplifier with relatively low quiescent current. It uses a unique two-stage topology which allows good AC and DC precision at low quiescent currents. The input stage is a degenerated bipolar one (the OP470 is the not degenerated version which offers lower voltage noise but has lower slew-rate). Noise performance will be optimum for medium-high source impedances as voltage noise is relatively high.

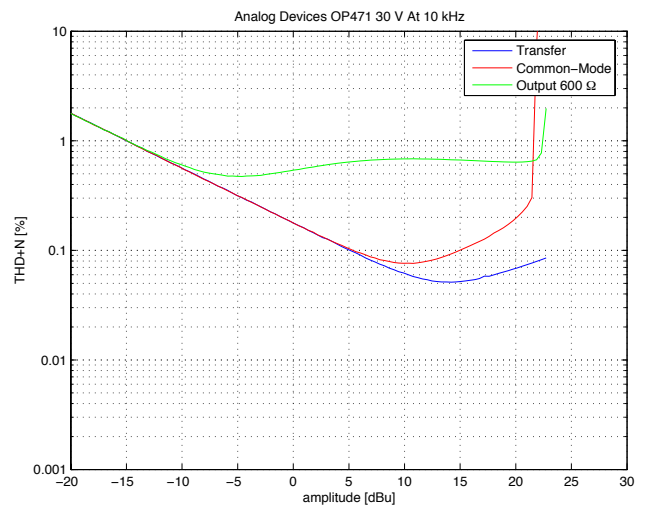
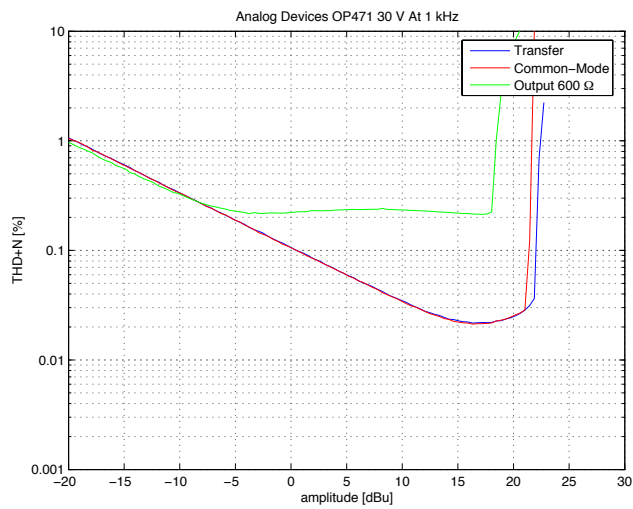
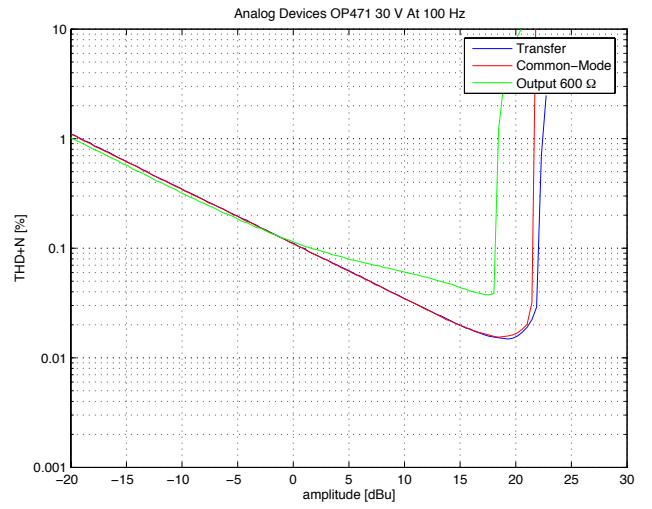
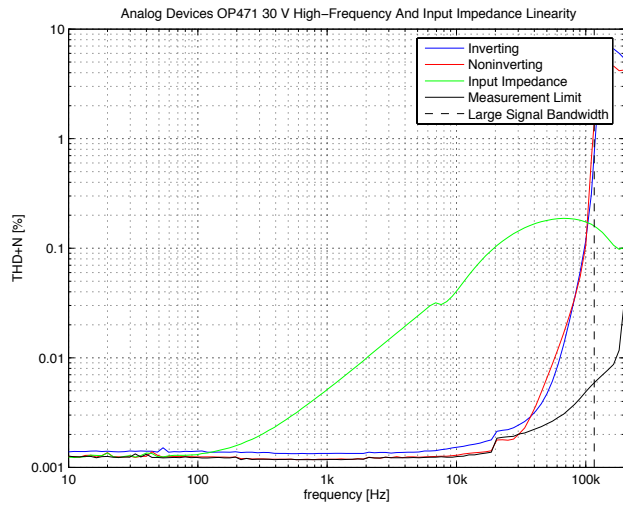
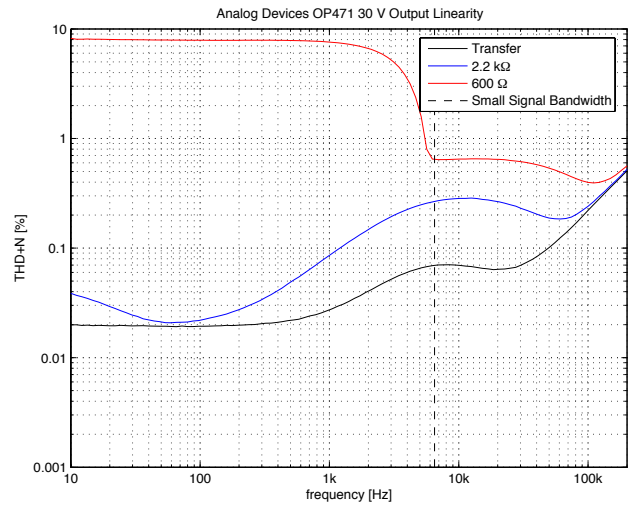
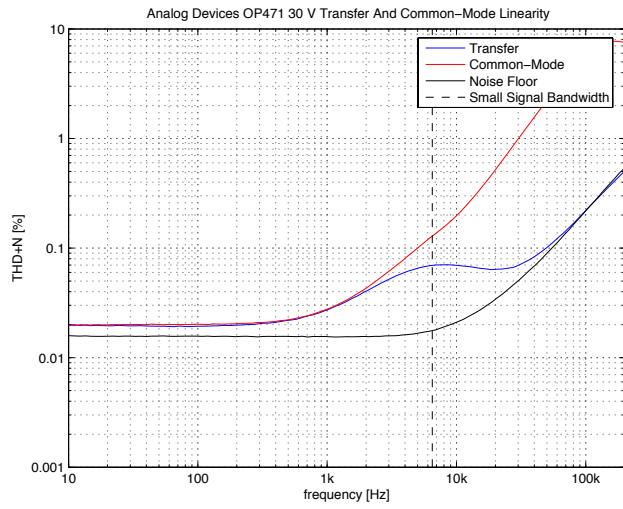
Both transfer and common-mode linearity is good at low frequencies but degrades significantly towards higher frequencies, particularly as slew-induced distortion becomes noticeable. The amplifier is not able to drive a  $600 \Omega$  load to  $+20 \text{ dBu}$  without current limiting<sup>4</sup>, and already  $2.2 \text{ k}\Omega$  causes thermal effects and a substantial increase in distortion at higher frequencies. Input impedance linearity is very good at low frequencies (although the amplifier uses input bias current cancellation which usually degrades input impedance linearity down to DC) but shows the usual capacitive effects. Note that the THD+N vs. amplitude plots at  $10 \text{ kHz}$  are only of limited significance as the gain bandwidth product of the amplifier limits the bandwidth to about  $6.5 \text{ kHz}$ .

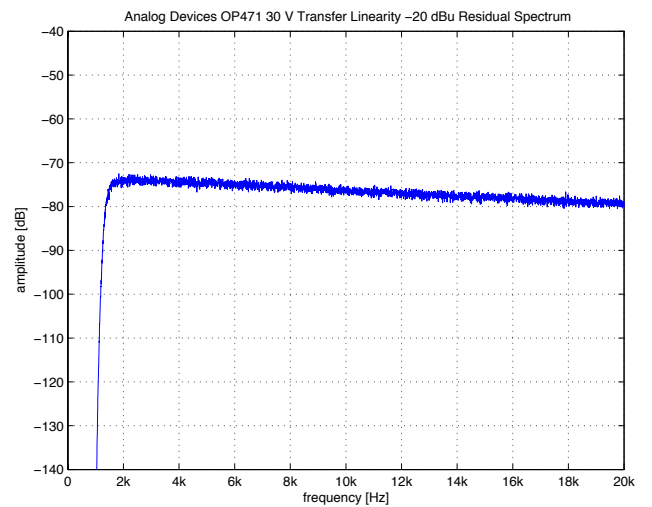
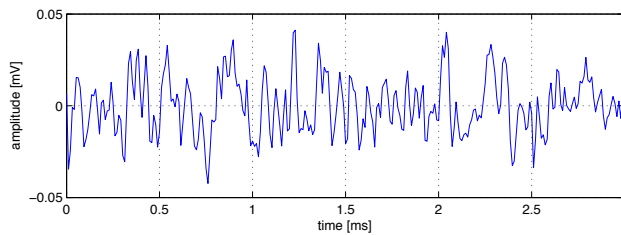
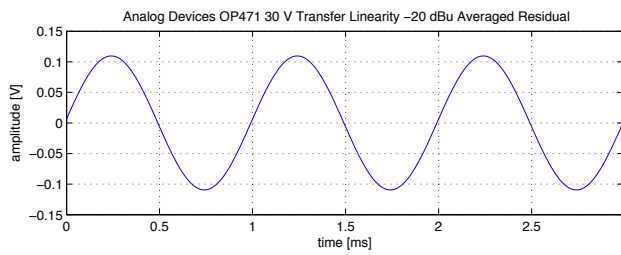
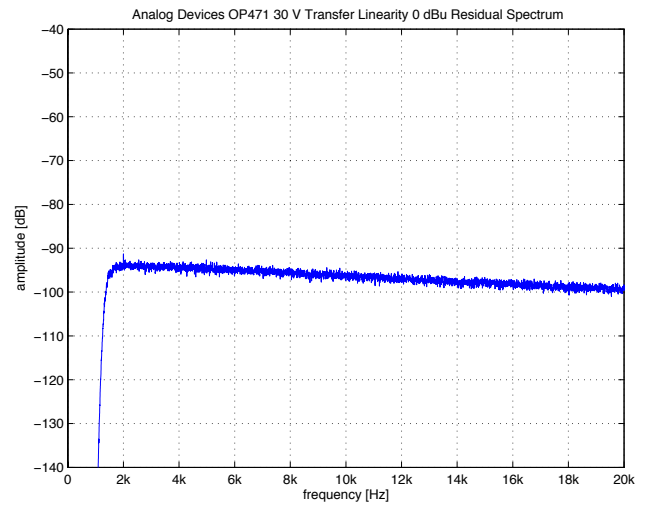
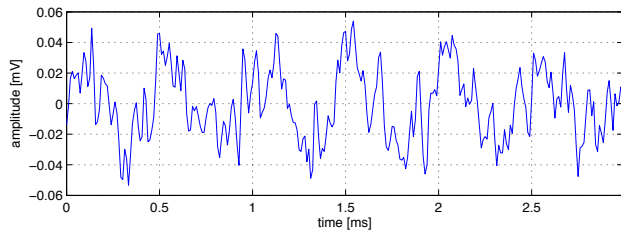
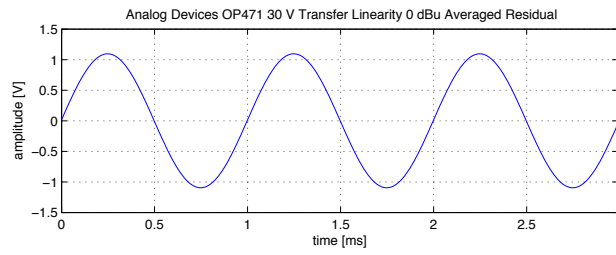
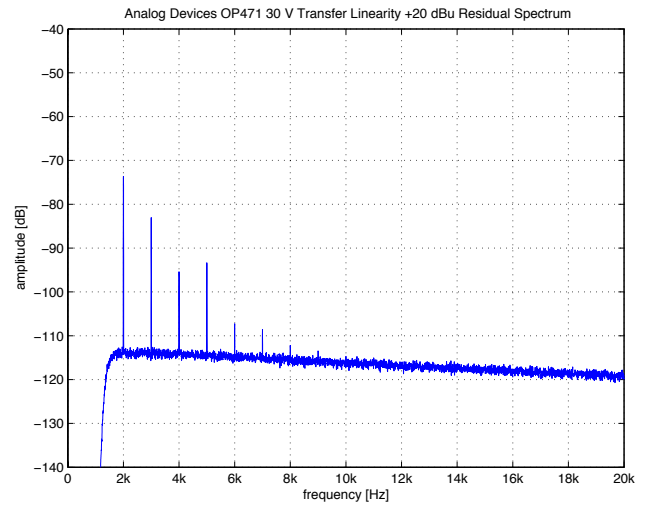
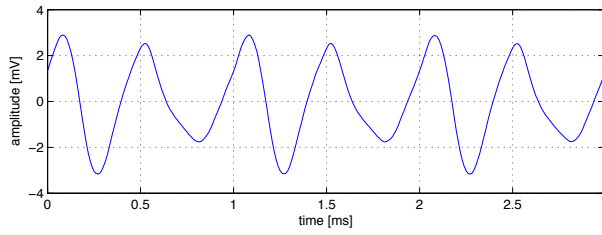
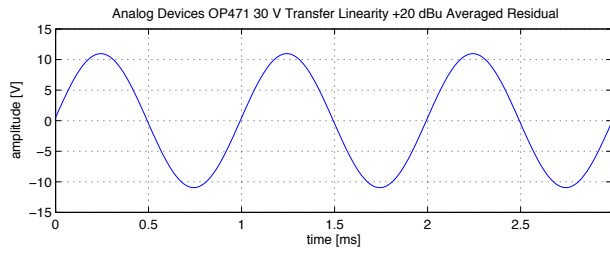
May be of use for applications which require excellent low-frequency linearity (assuming the output loading effects can be dealt with) at low

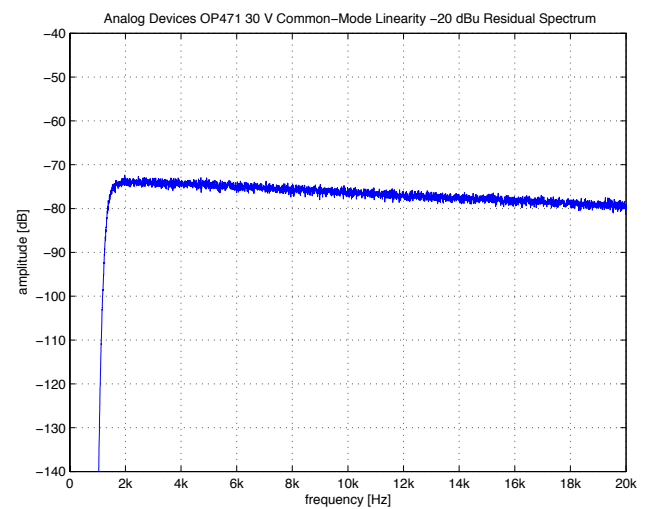
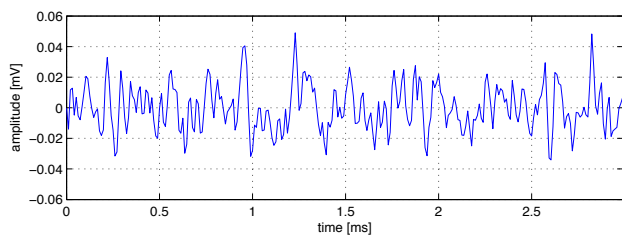
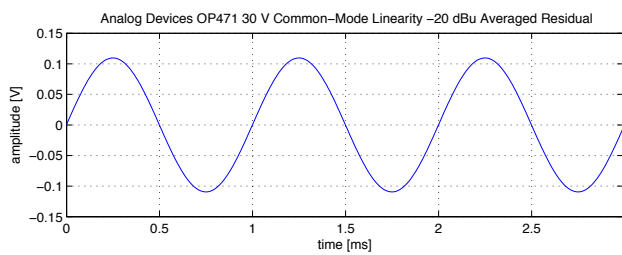
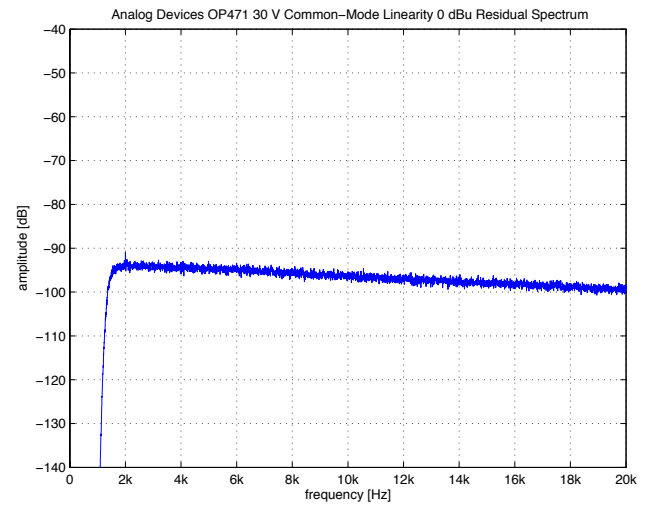
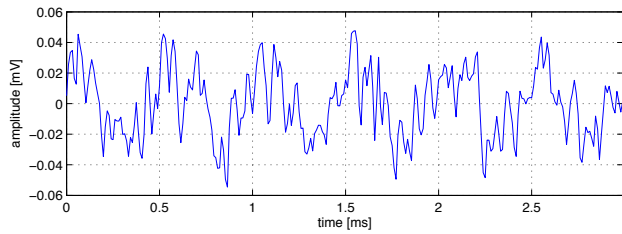
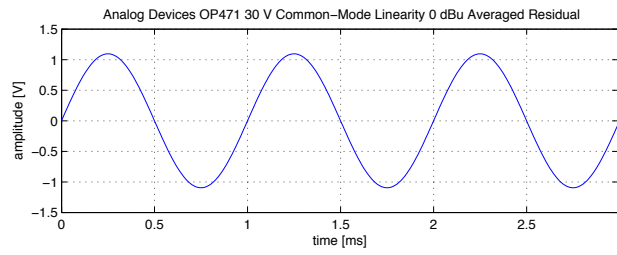
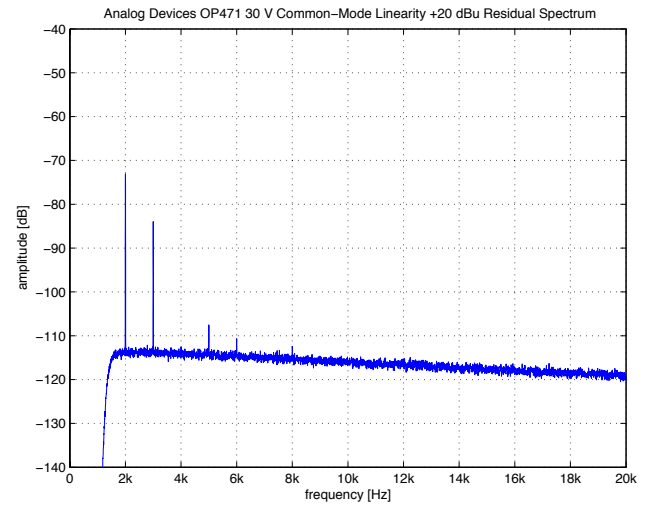
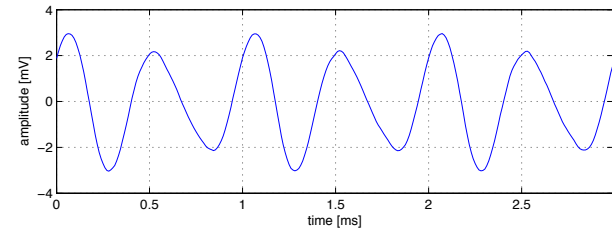
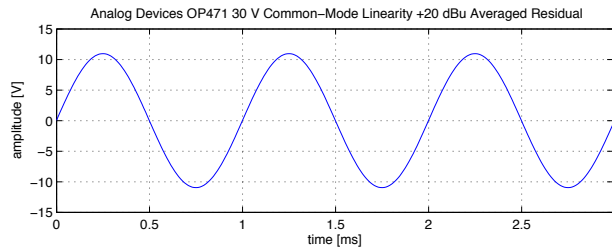
<sup>4</sup>The hum visible in the according FFT plot is probably a result of the current limiting causing reduced open-loop gain and hence PSRR.

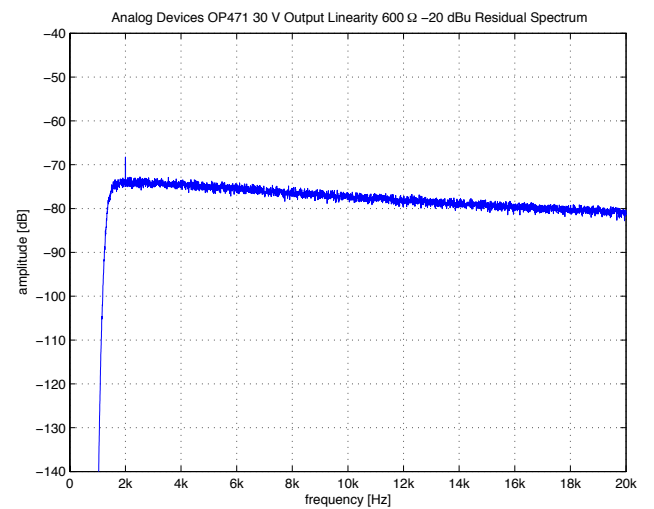
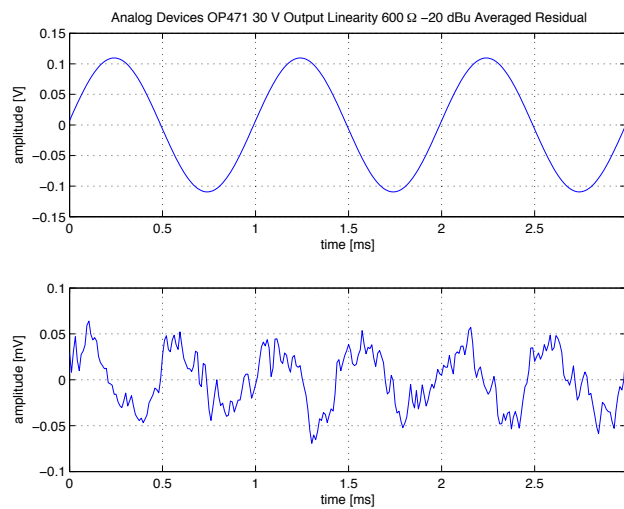
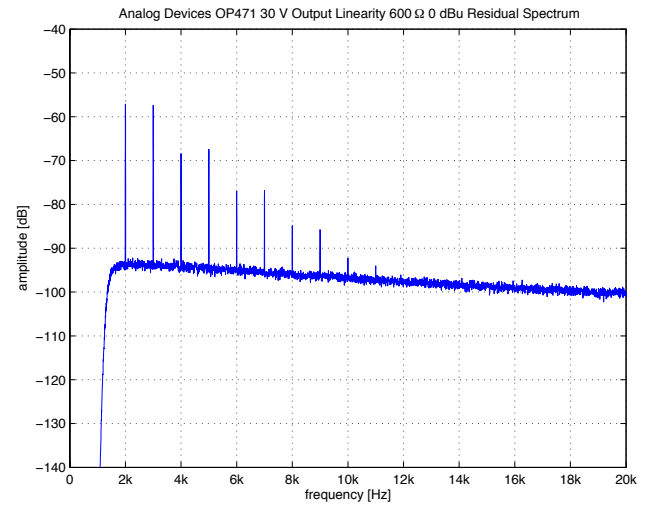
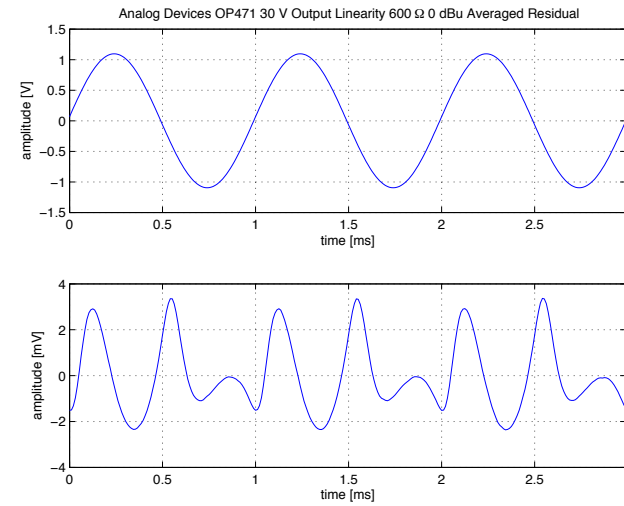
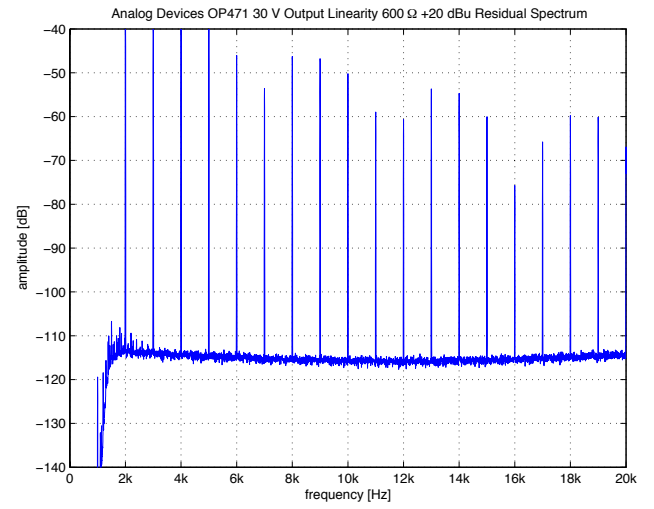
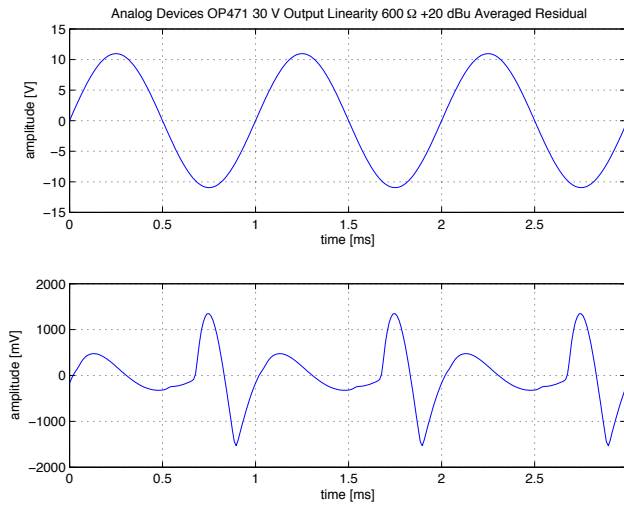
quiescent current. For general use in the audio frequency range probably better replaced with other amplifiers. Reasonably priced considering the DC precision (particularly the low input bias current).











### 3.5 Linear Technology LT1007

<b>Number of Channels</b>	1
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	1.90 US\$ at 1k units (August 2008)

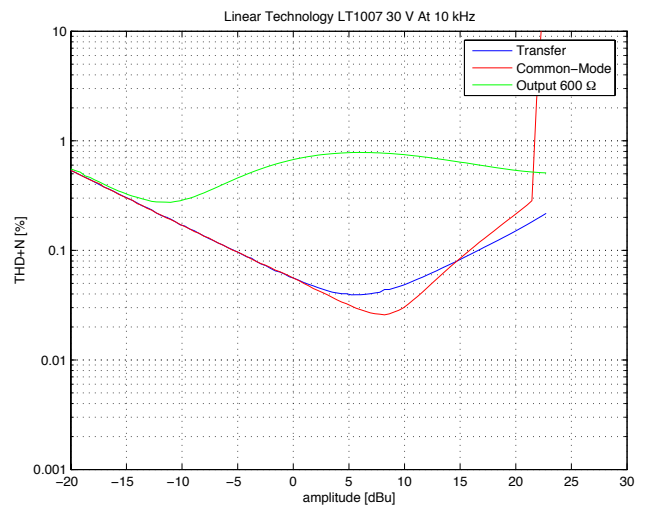
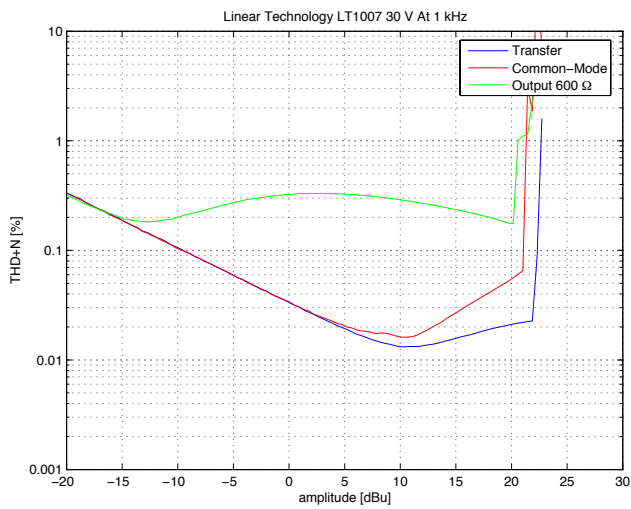
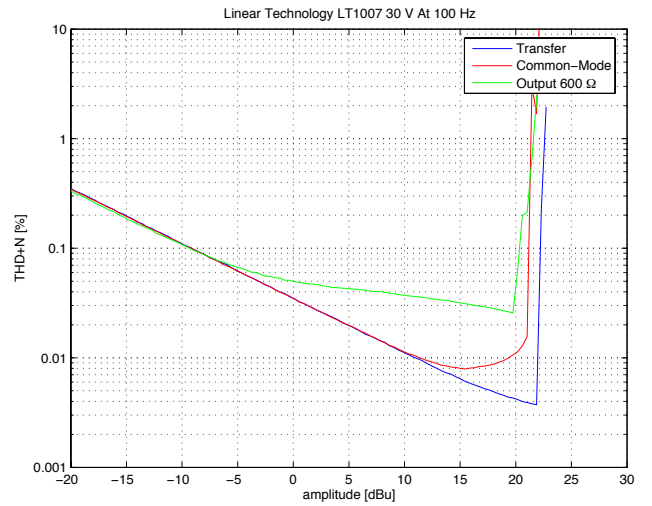
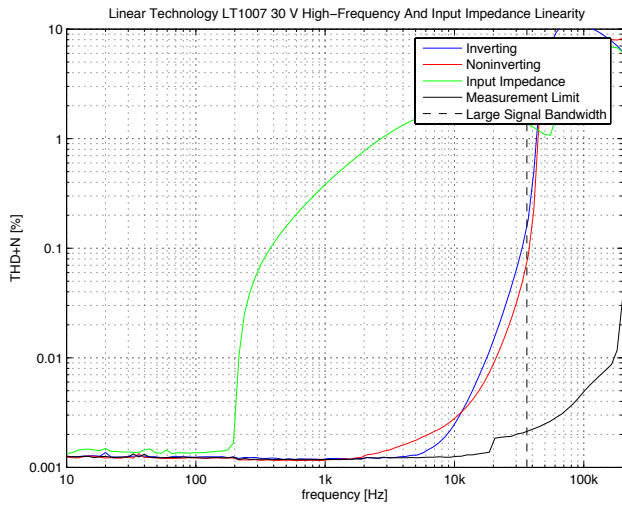
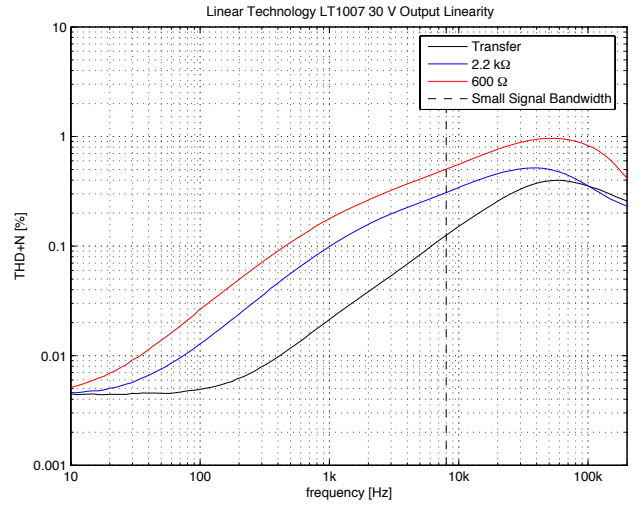
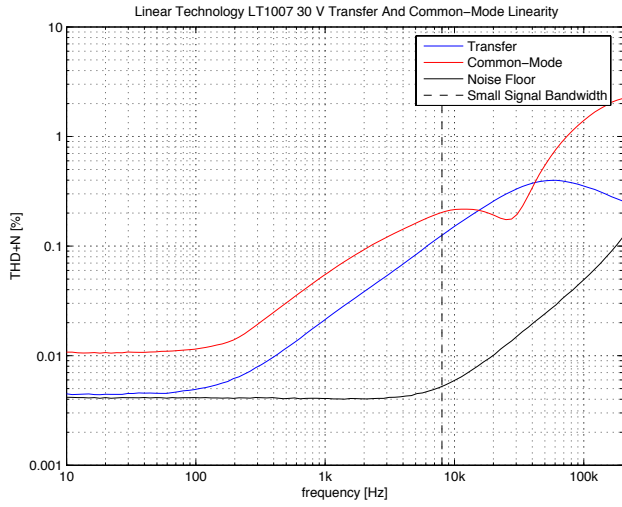
Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		20	60	$\mu\text{V}$
Input Bias Current		15	55	nA
Input Offset Current		12	50	nA
Gain Bandwidth Product	5	8		MHz
Slew-Rate	1.7	2.5		$\text{V}/\mu\text{S}$
Input Voltage Noise ( $f = 1 \text{ kHz}$ )		2.5	3.8	$\text{nV}/\sqrt{\text{Hz}}$
Input Current Noise ( $f = 1 \text{ kHz}$ )		0.4	0.6	$\text{pA}/\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 11$	$\pm 12.5$		V
Output Voltage Swing ( $R_L = 2 \text{ k}\Omega$ )	$\pm 12.5$	$\pm 13.5$		V
Output Voltage Swing ( $R_L = 600 \Omega$ )	$\pm 10.5$	$\pm 12.5$		V
Power Supply Voltage	$\pm 2.5$		$\pm 22$	V

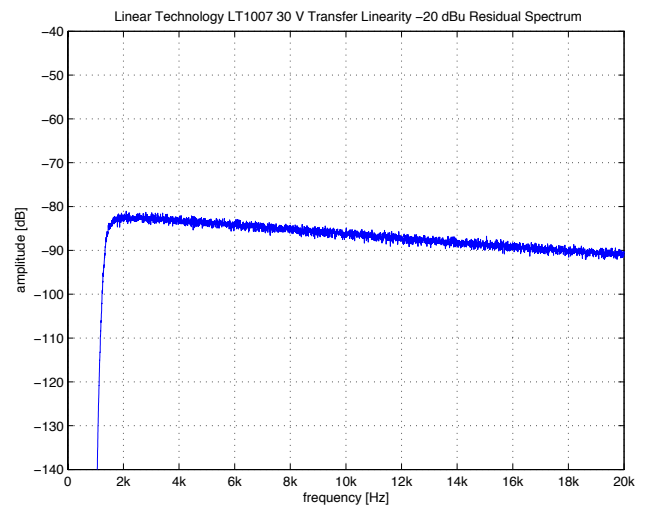
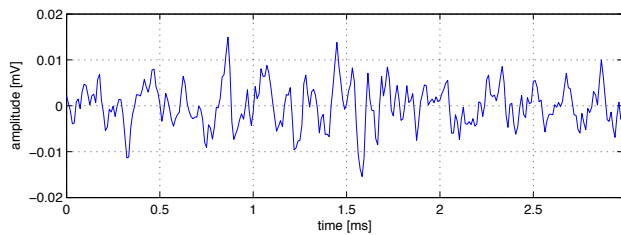
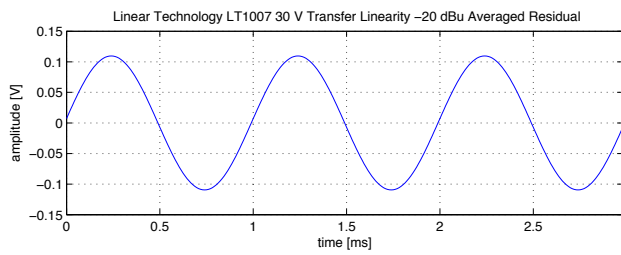
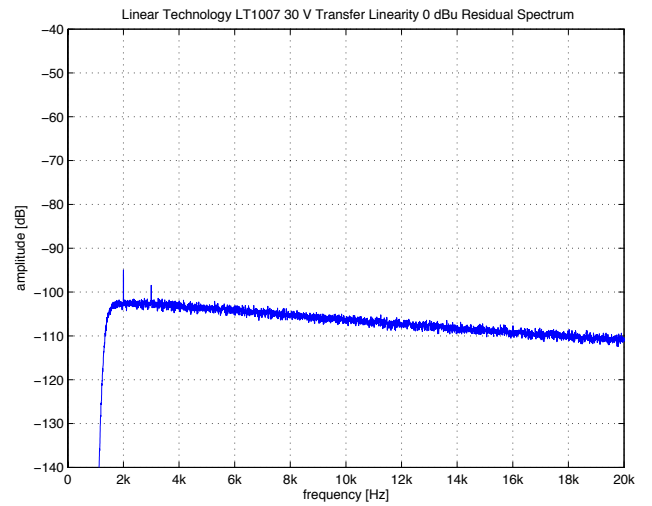
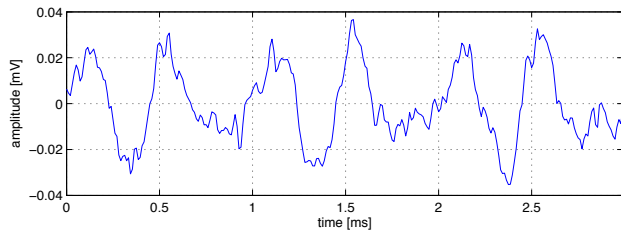
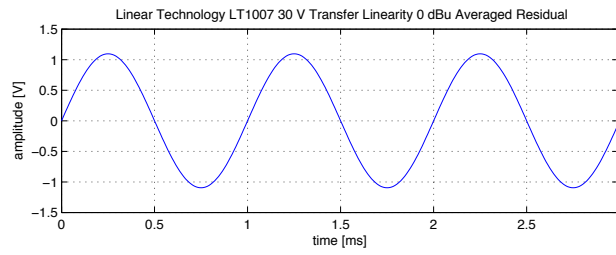
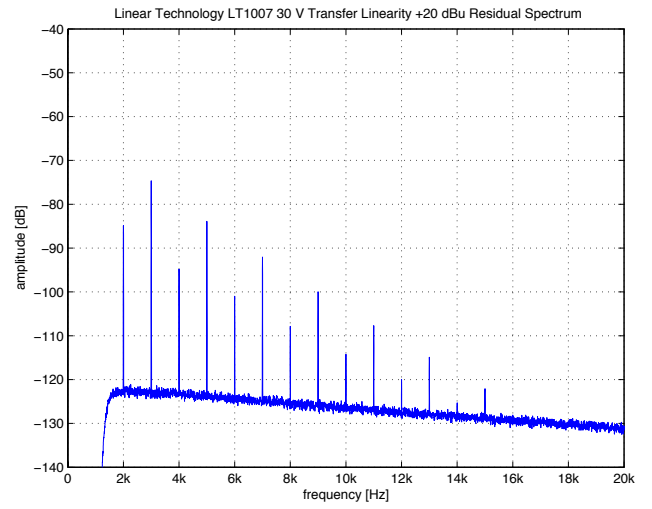
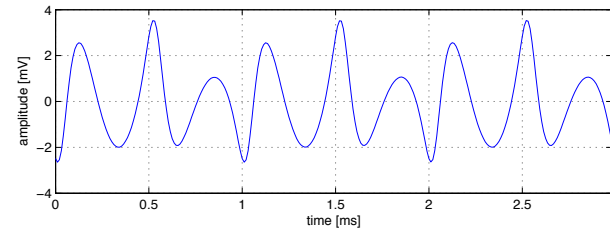
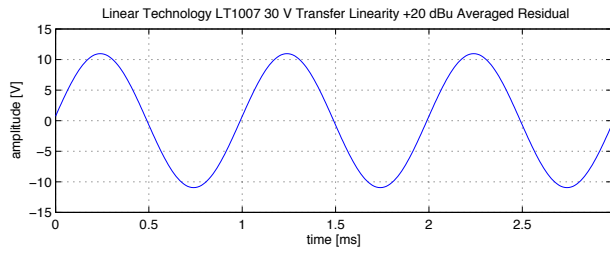
Table 3.5: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 15 \text{ V}$ .

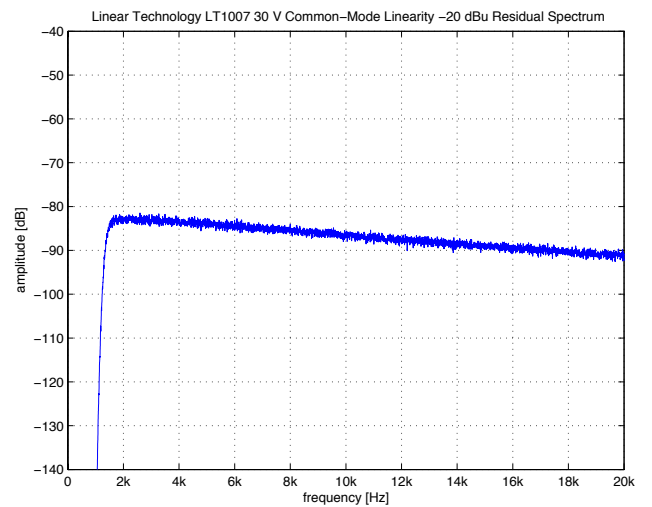
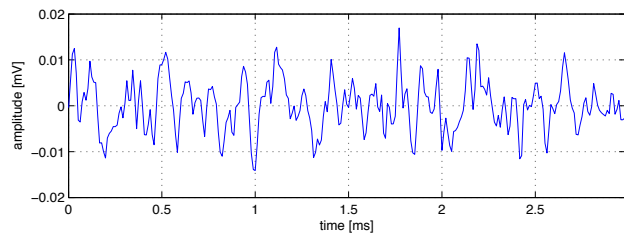
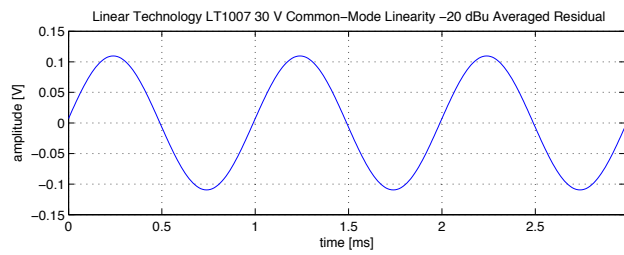
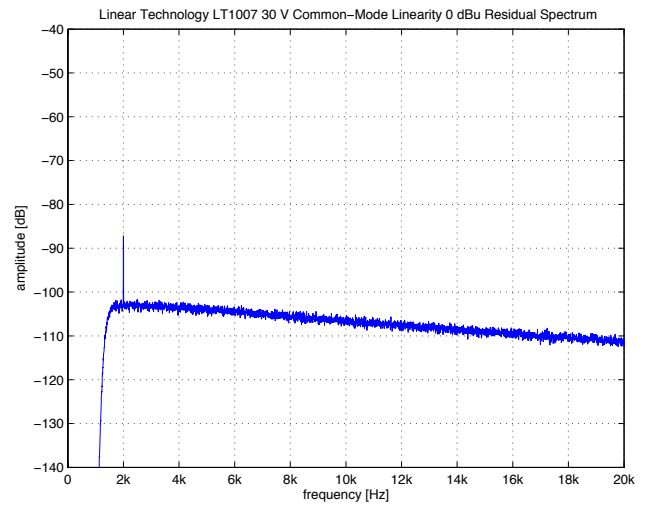
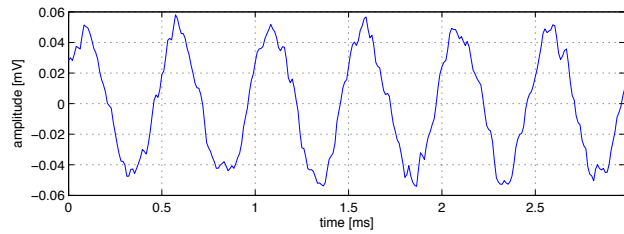
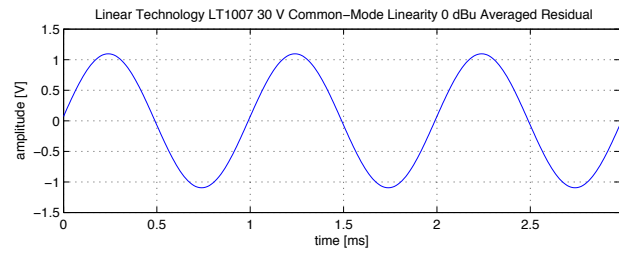
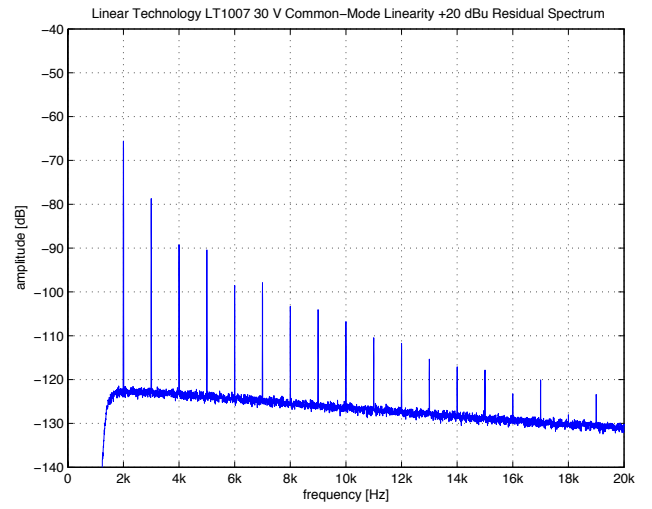
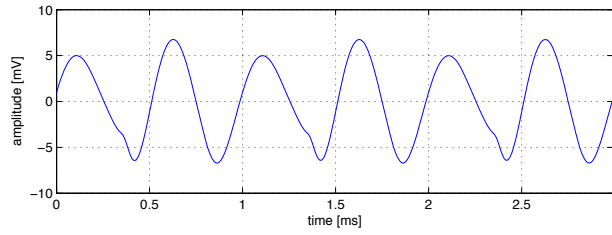
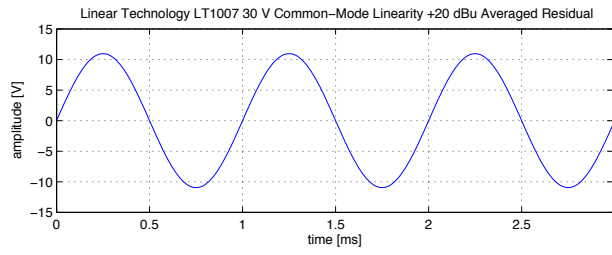
A precision amplifier based on a standard three-stage topology with bipolar inputs. Voltage noise is low, and current noise not too bad either. Speed is very limited though. Supports wide power supply range.

Not an amplifier with particularly low distortion; while linearity at low frequencies is typically very good things clearly degrade with increasing frequency. Particularly bad is output distortion (which shows significant crossover distortion) and slew-induced high-frequency distortion. The input impedance linearity shows idiosyncratic behaviour; while no distortion is measurable up to 200 Hz an almost immediate increase above this frequency shows up and leads to serious distortion values. The datasheet does not reveal any hint for a possible cause of this behaviour; a second device was measured and identical distortion was found. Higher supply voltages somewhat reduce common-mode distortion but do not address the other problem areas.

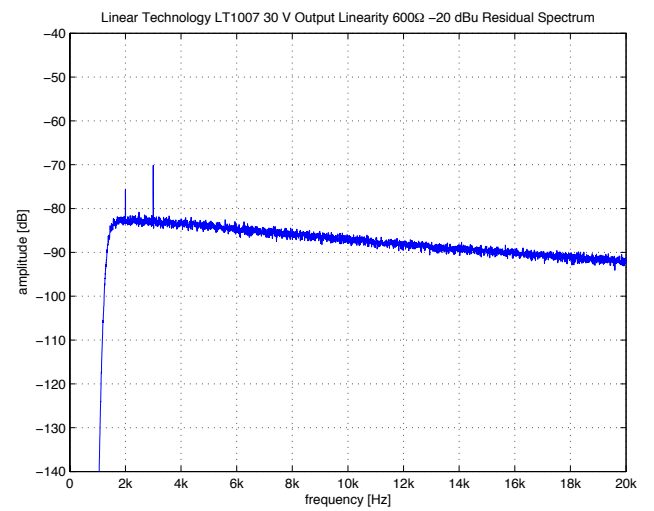
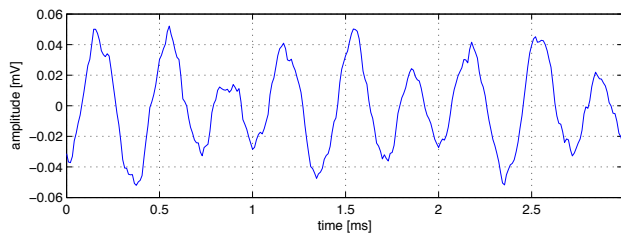
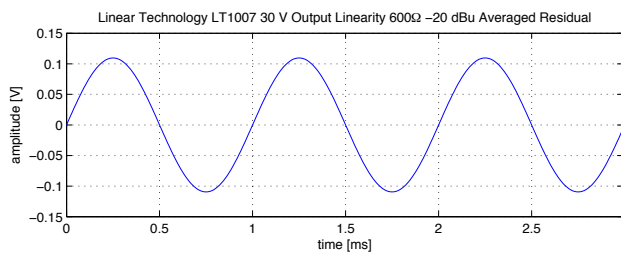
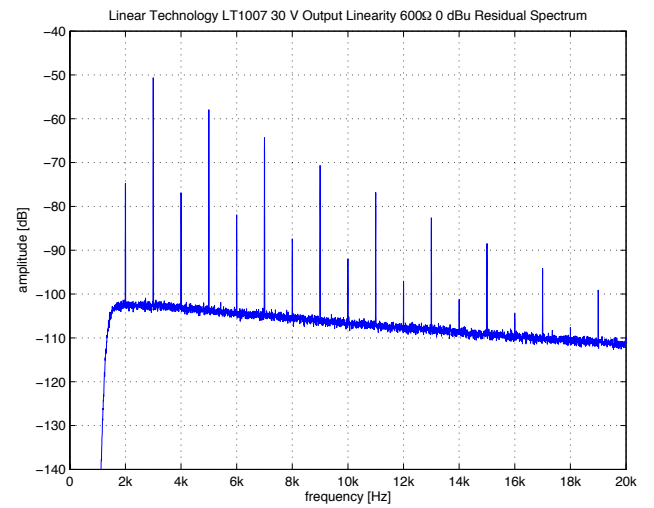
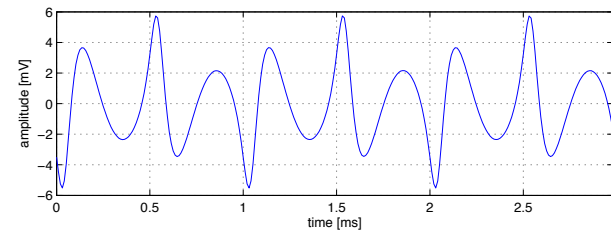
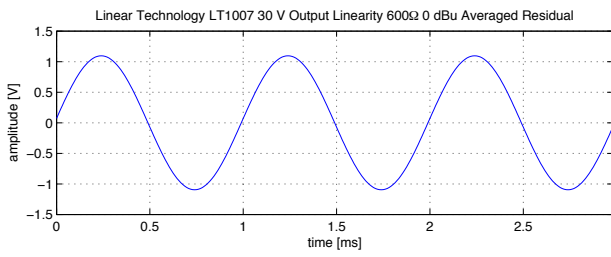
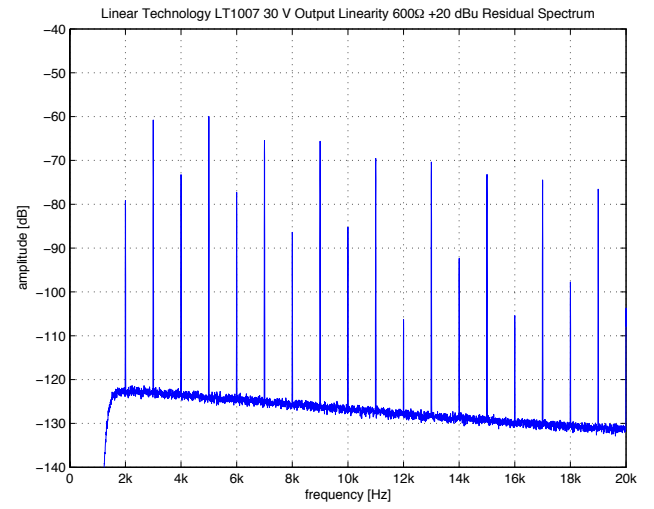
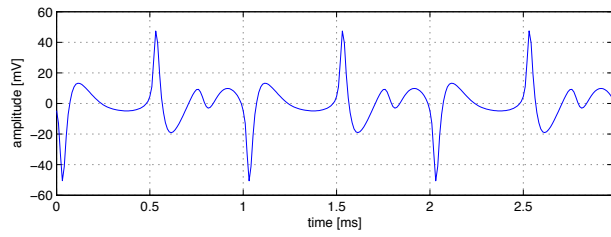
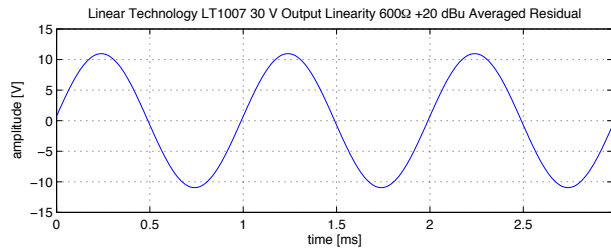
Probably not of much use for low distortion applications.

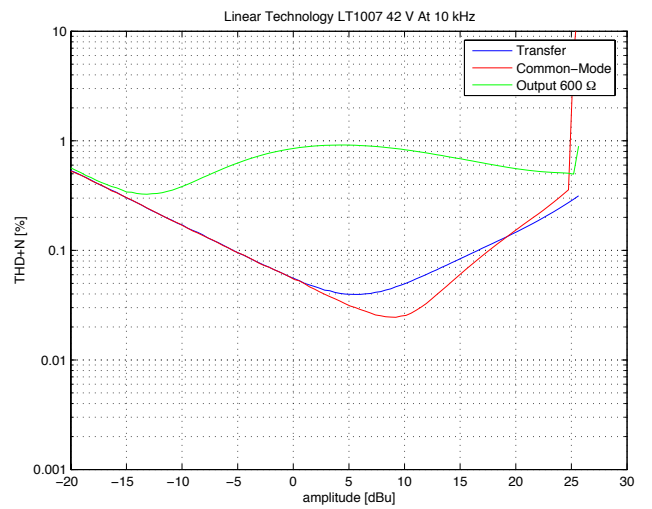
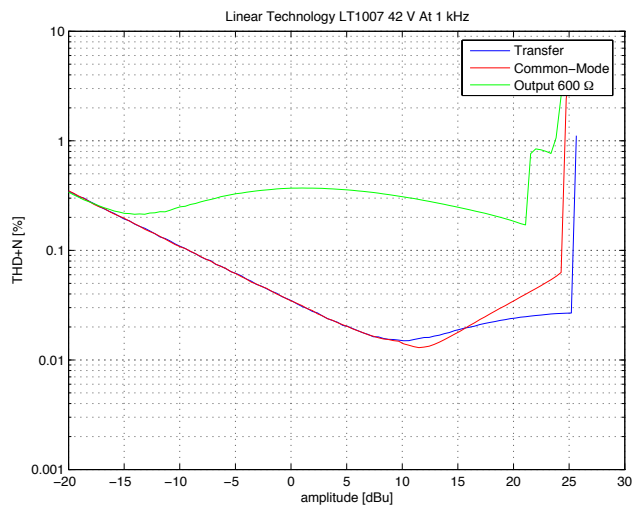
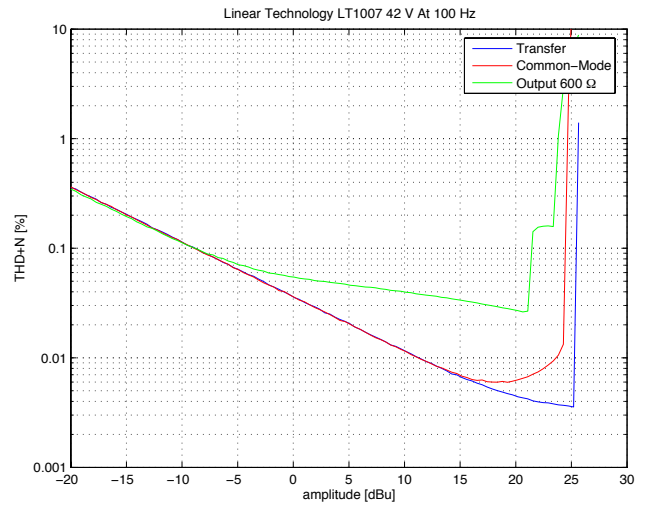
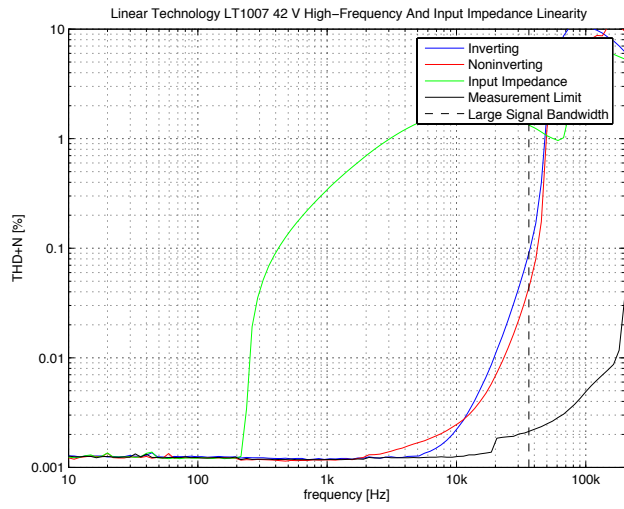
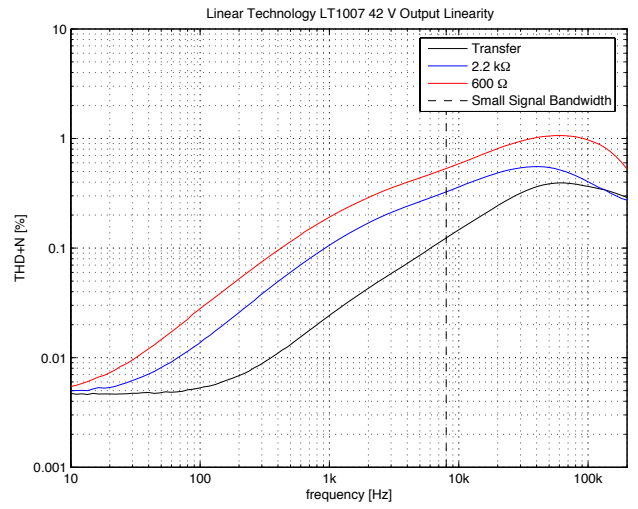
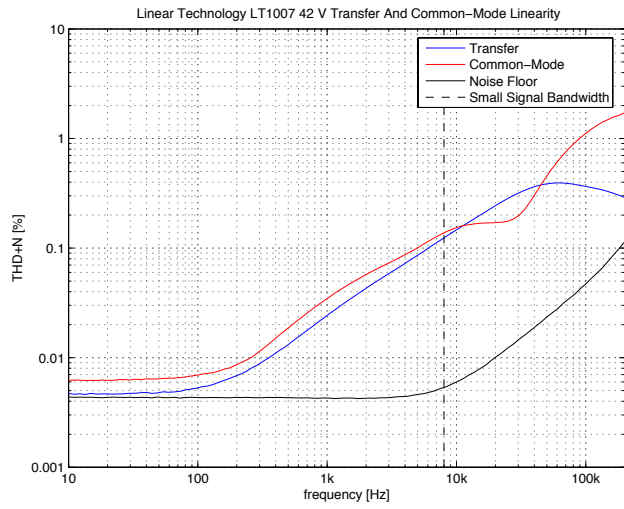


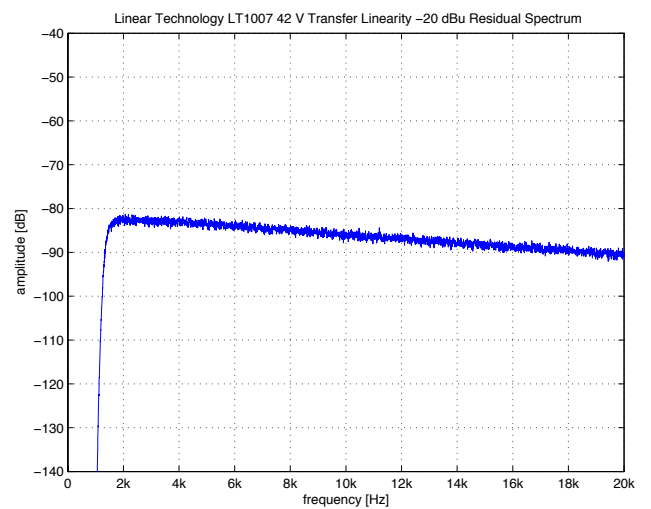
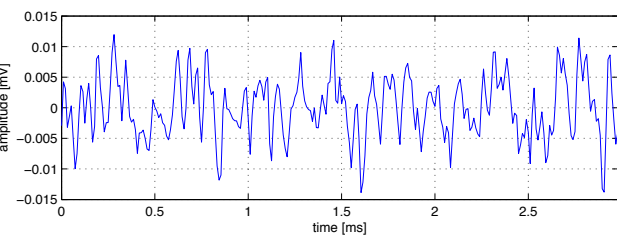
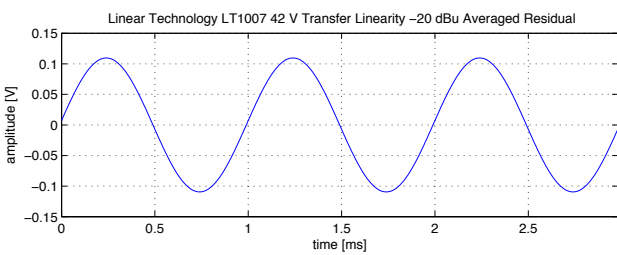
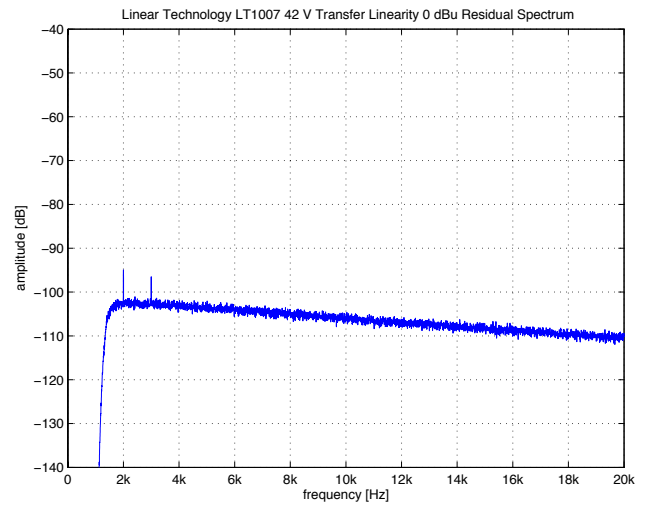
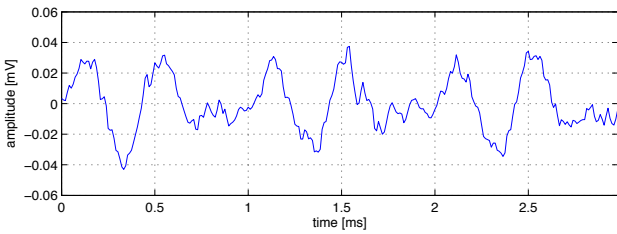
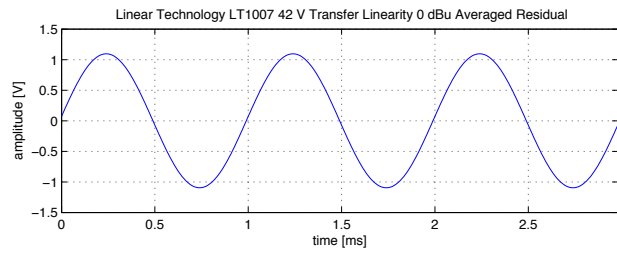
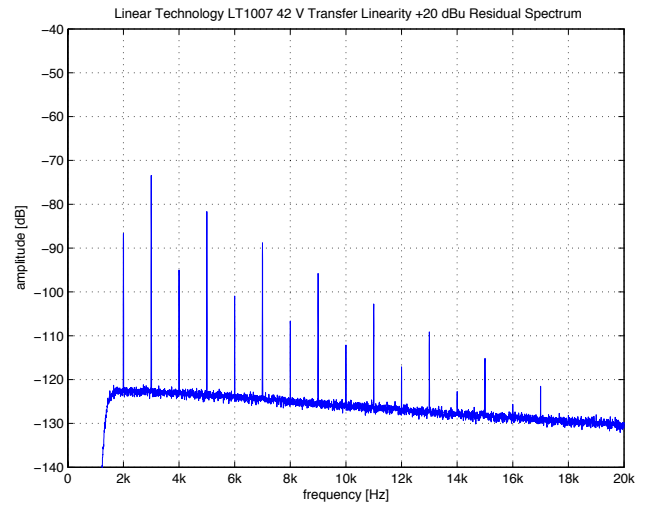
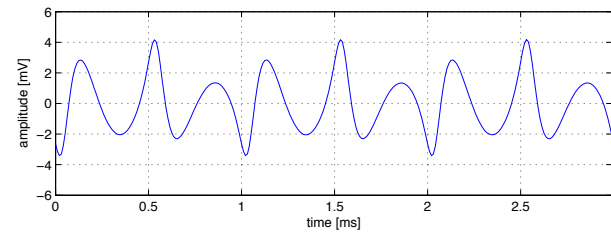
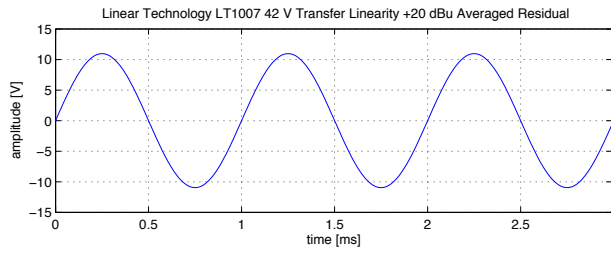


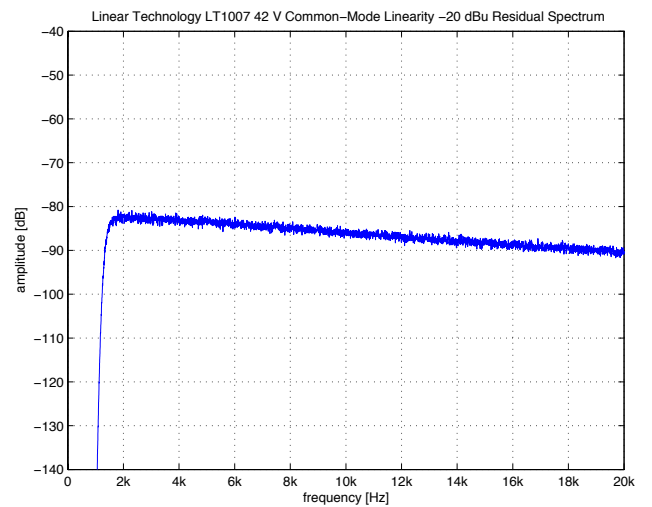
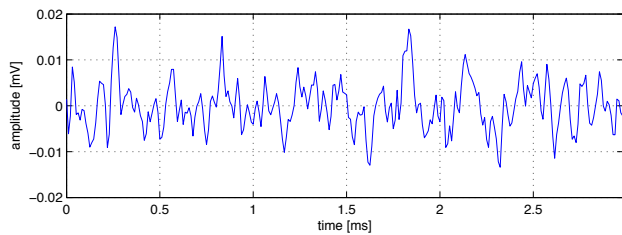
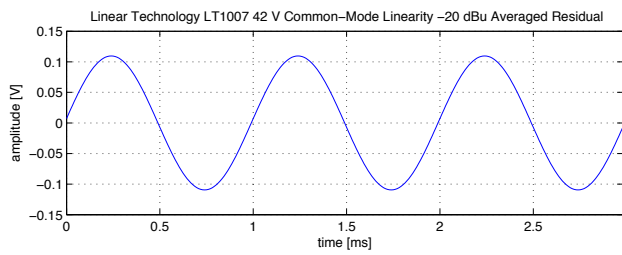
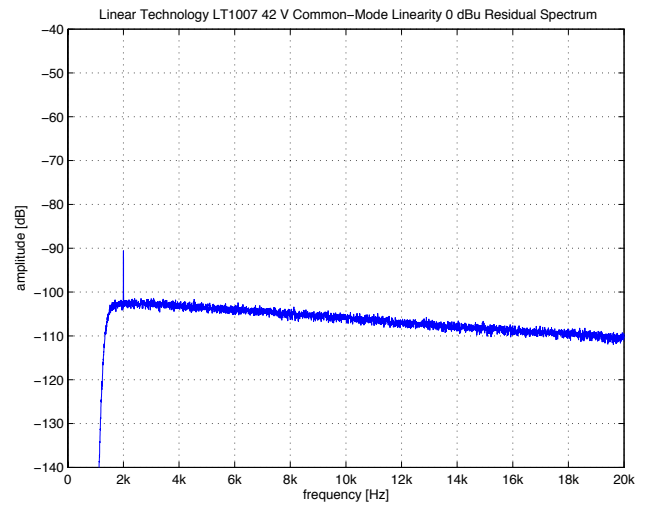
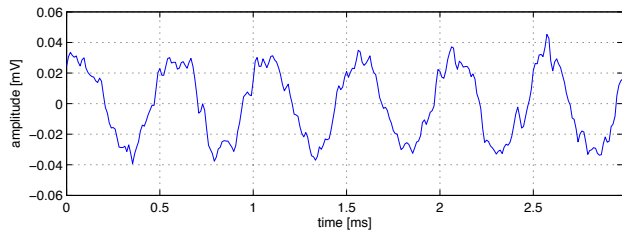
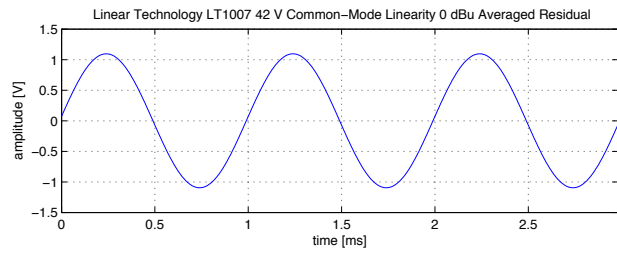
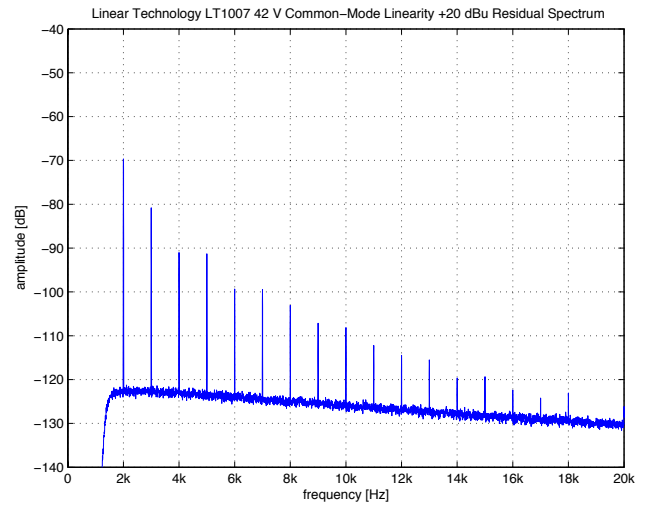
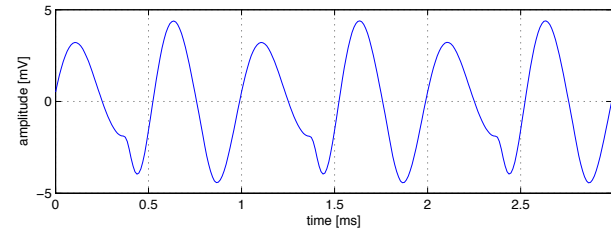
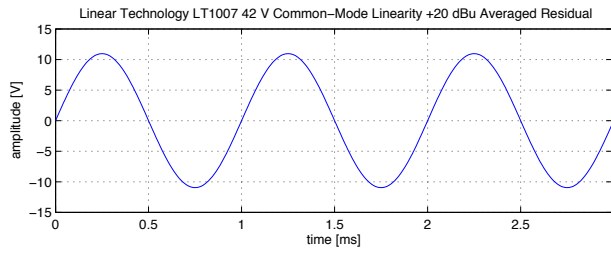


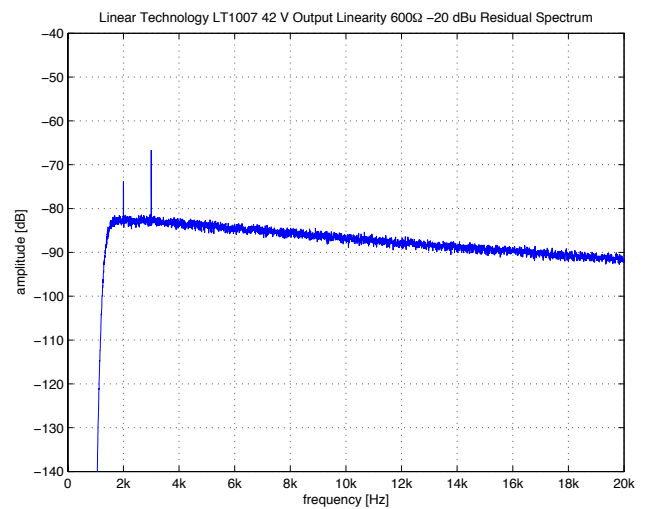
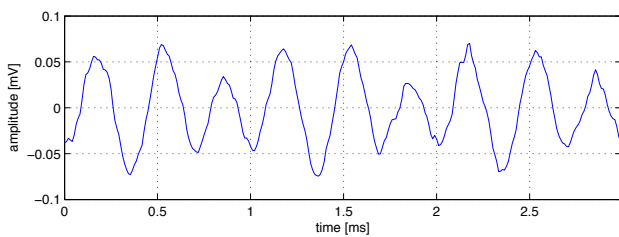
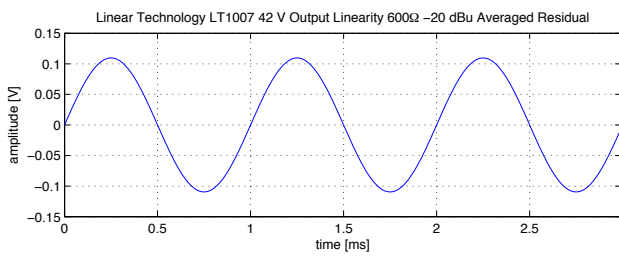
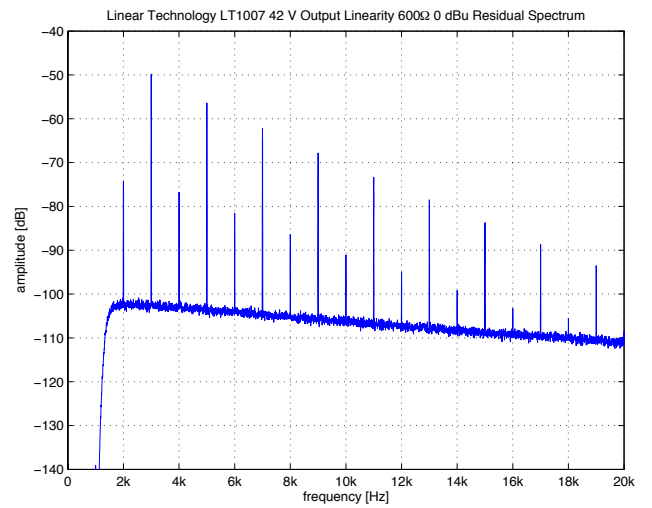
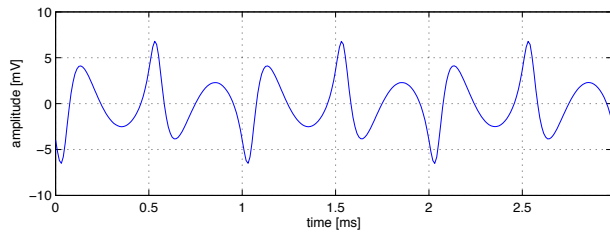
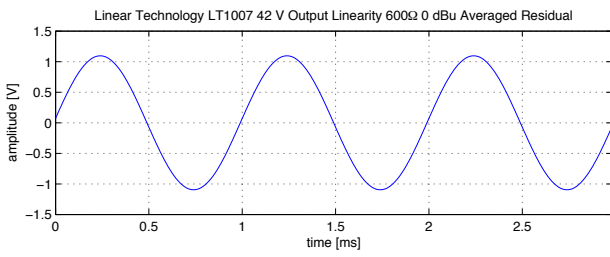
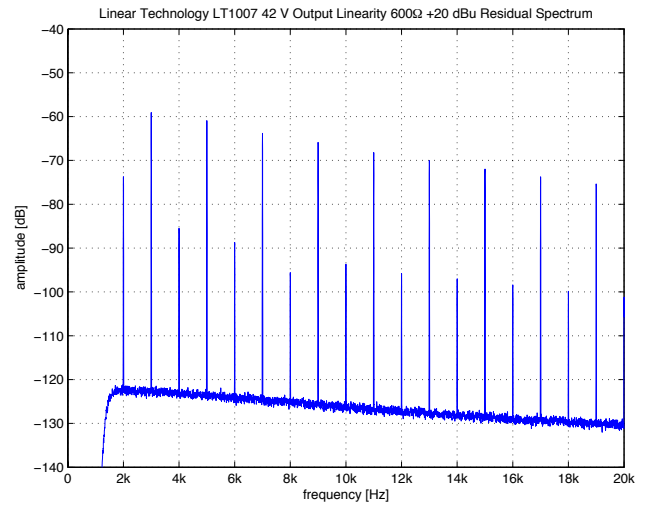
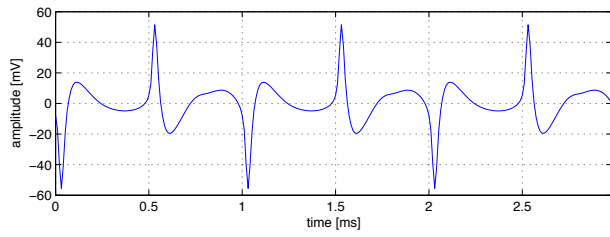
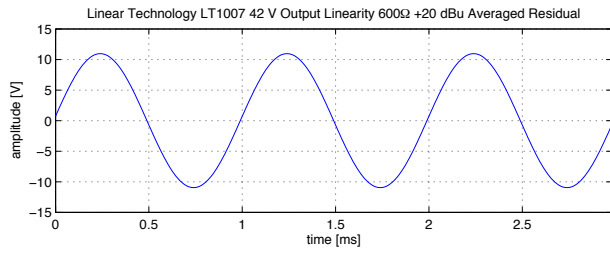












### 3.6 Linear Technology LT1115

<b>Number of Channels</b>	1
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	2.90 US\$ at 1k units (July 2008)

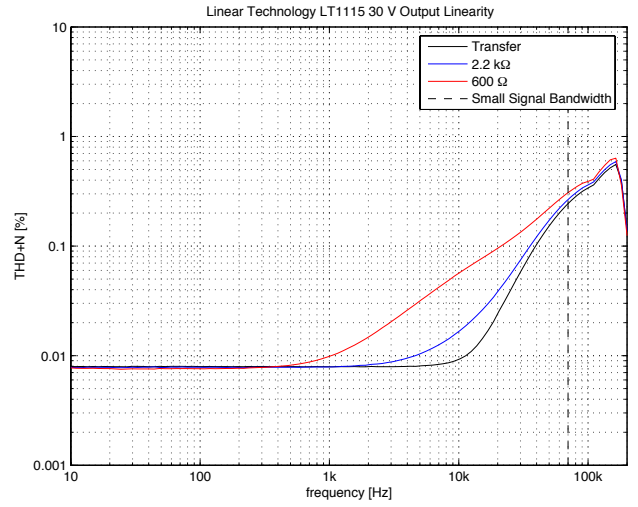
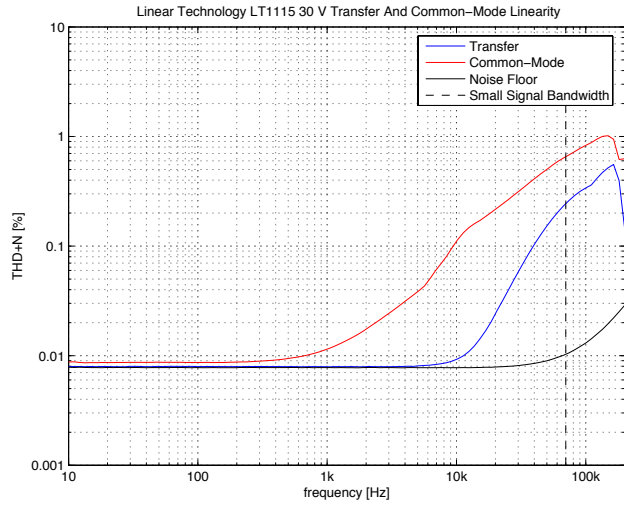
Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		50	200	$\mu\text{V}$
Input Bias Current		50	380	nA
Input Offset Current		30	200	nA
Gain Bandwidth Product	40	70		MHz
Slew-Rate	10	15		$\text{V}/\mu\text{S}$
Input Voltage Noise ( $f = 1 \text{ kHz}$ )		0.9	1.2	$\text{nV}/\sqrt{\text{Hz}}$
Input Current Noise ( $f = 1 \text{ kHz}$ )		1.2	2.2	$\text{pA}/\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 13.5$	$\pm 15$		V
Output Voltage Swing ( $R_L = 2 \text{ k}\Omega$ )	$\pm 14.5$	$\pm 15.5$		V
Output Voltage Swing ( $R_L = 600 \Omega$ )	$\pm 11$	$\pm 14.5$		V
Power Supply Voltage			$\pm 44$	V
Quiescent Current per Amplifier		8.5	11.5	mA

Table 3.6: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 18 \text{ V}$ .

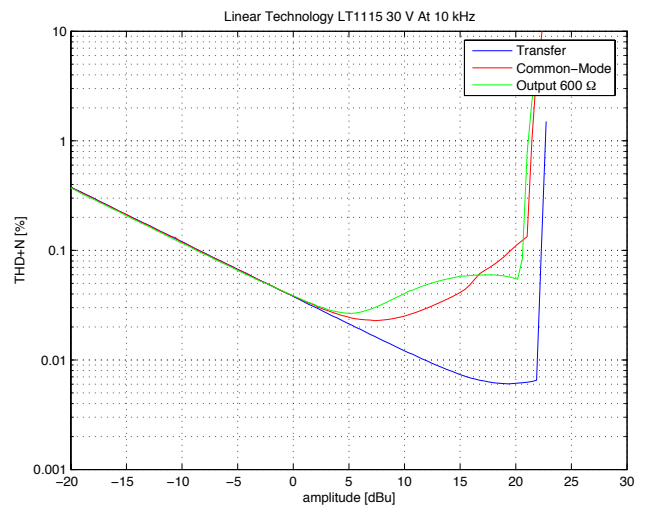
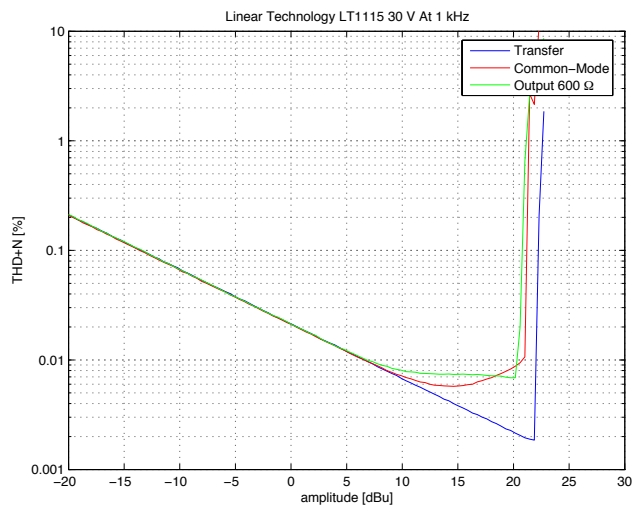
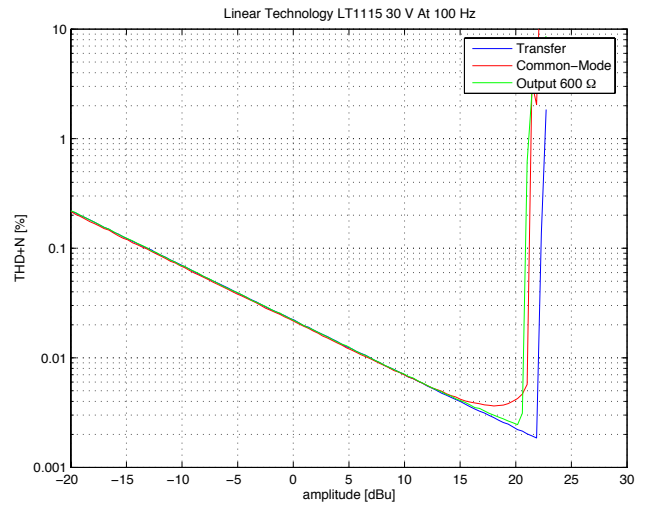
Although the datasheet shows no topological details this amplifier seems to use the same architecture as the LT1028/LT1128 (i.e. a three-stage topology with bipolar input); the slightly different specifications are presumably a result from somewhat changed bias and compensation details. This opamp is only stable at noise gains of about 2 or more, hence no high-frequency and input impedance plots are shown. Voltage noise is very low, and current noise good as well for the given voltage noise level.

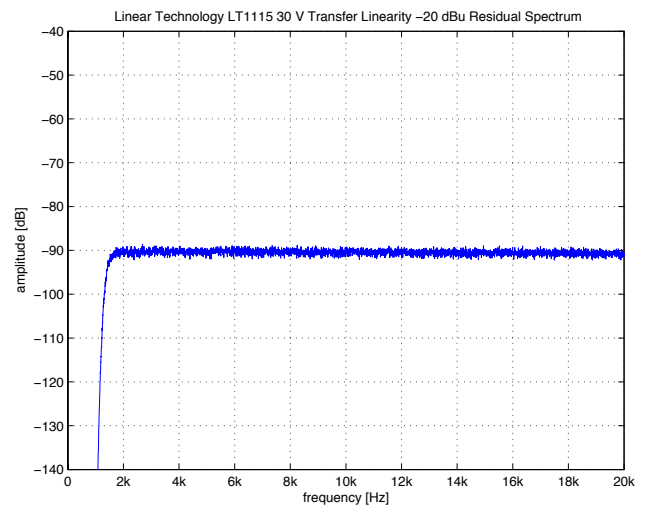
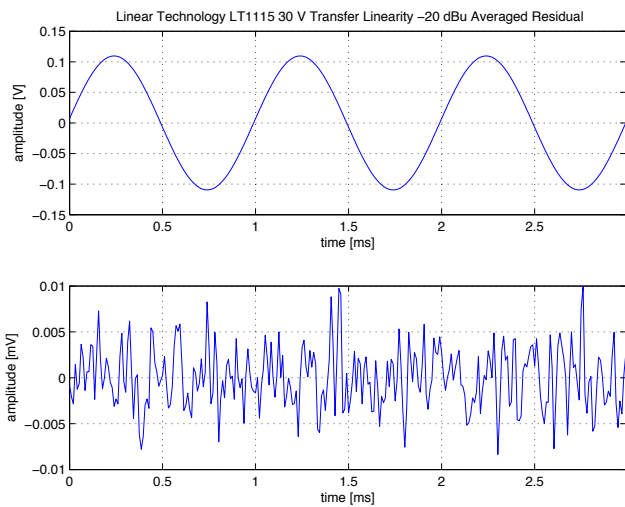
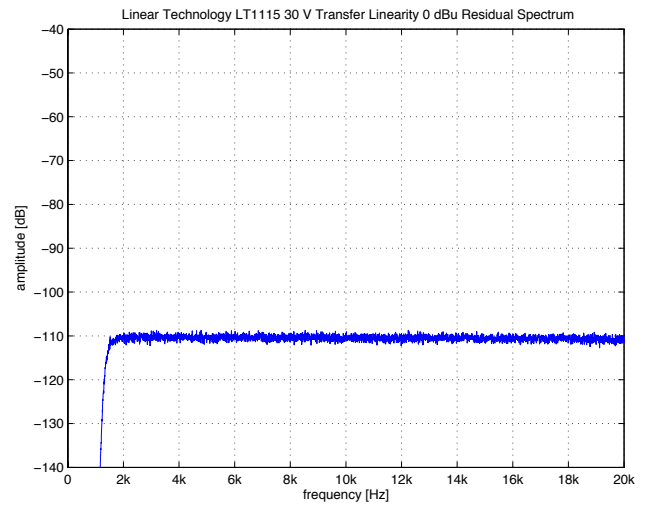
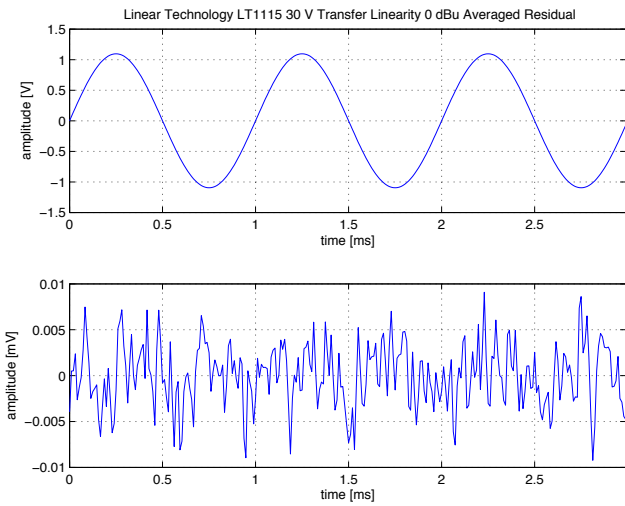
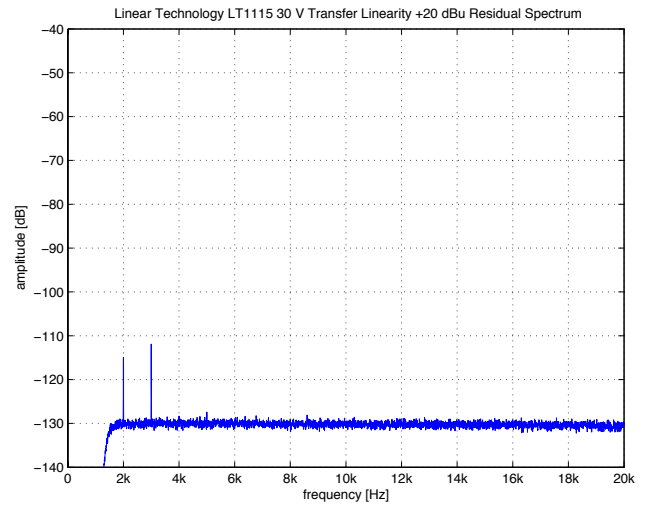
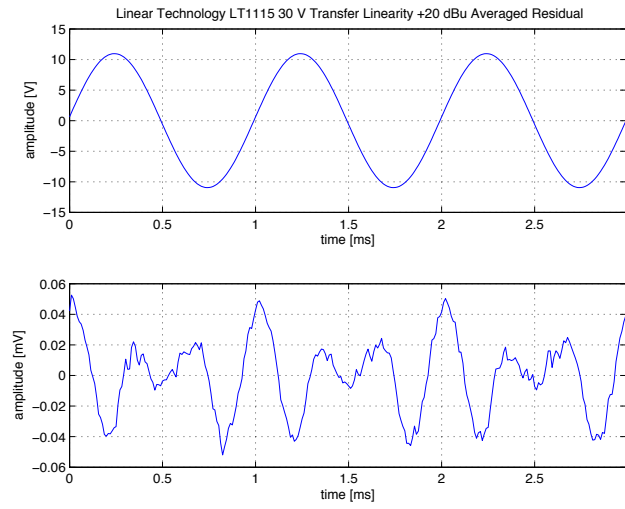
The basic transfer linearity is exceptionally good within the audio band, rises relatively fast above that frequency range though. Distortion from common-mode and output loading effects do clearly degrade the transfer linearity performance. Higher supply voltages at least somewhat reduce common-mode distortion. Note that there is some interference right below 3 kHz visible in the FFT plots of the common-mode linearity which might at first look like 3<sup>rd</sup> harmonic distortion.

The overall distortion is good as long as common-mode and output effects do not become dominant; probably a particularly interesting part for applications where low distortion is needed in conjunction with low voltage noise and/or relatively good DC precision. Otherwise the high price tag is perhaps not to justify.

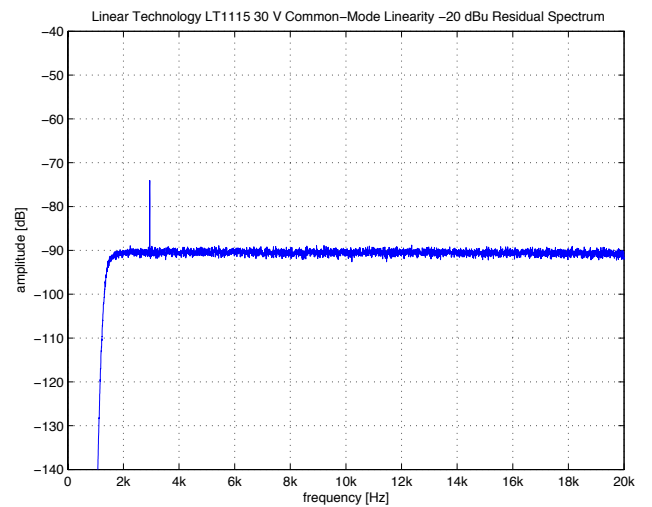
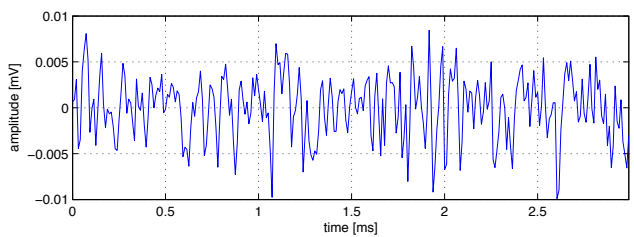
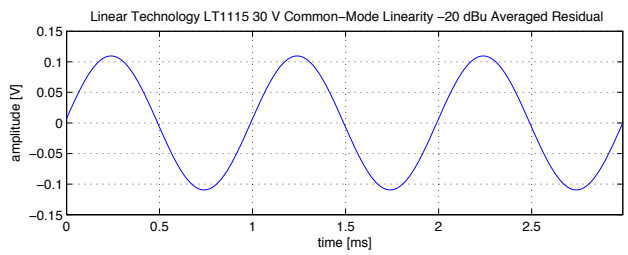
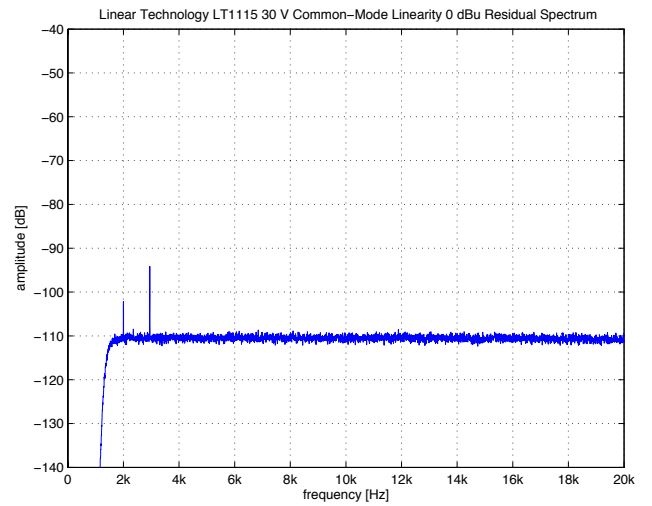
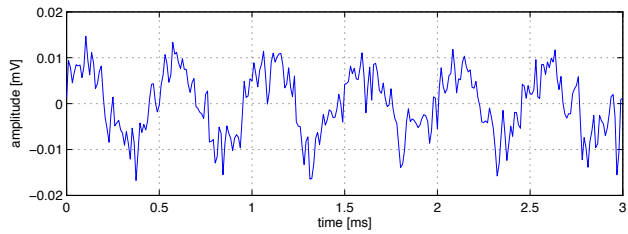
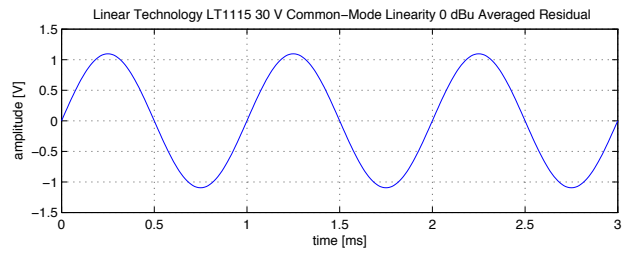
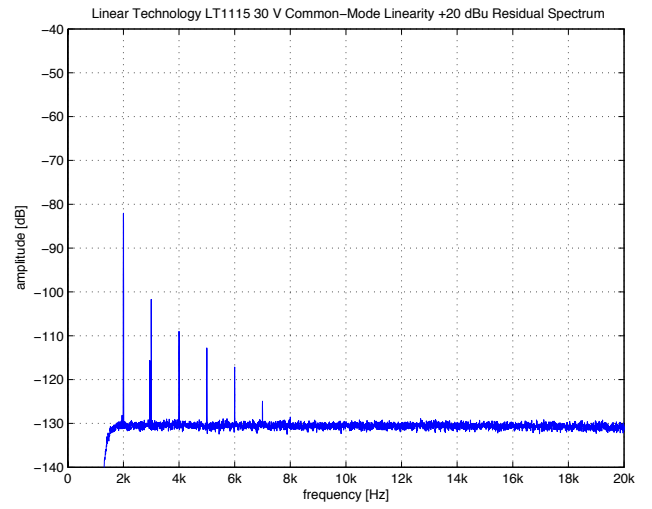
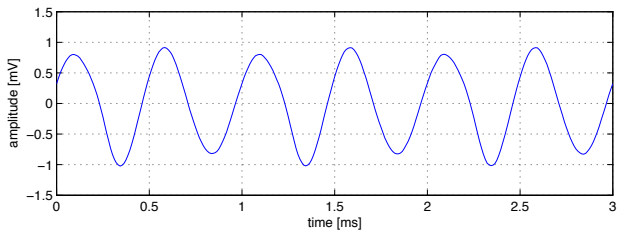
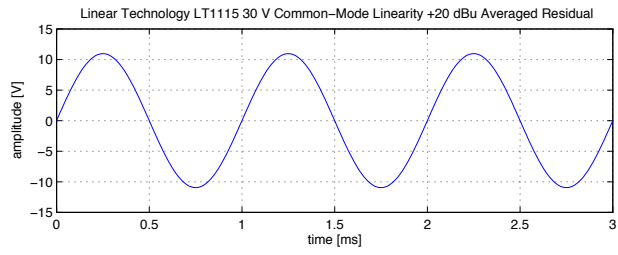


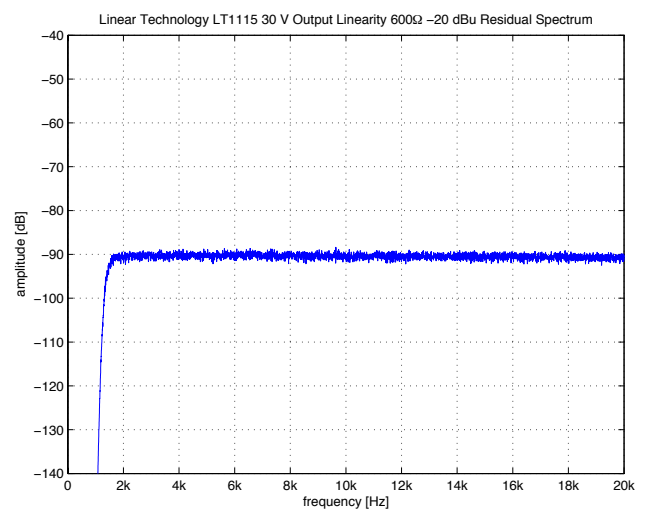
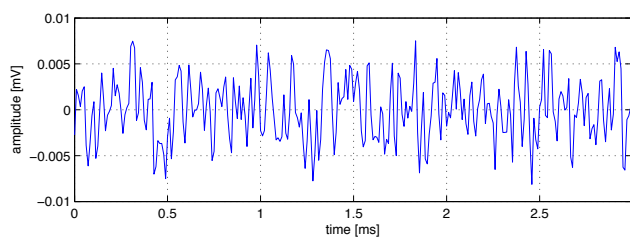
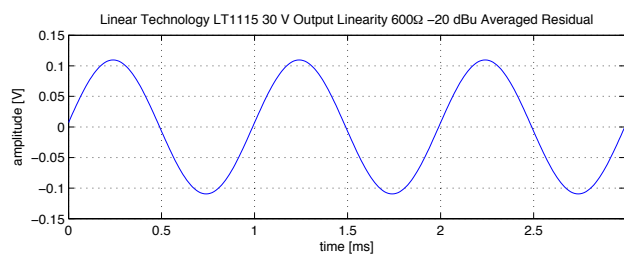
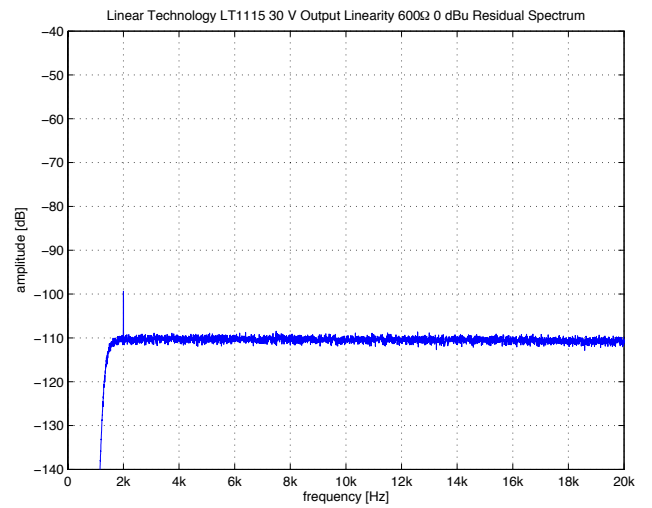
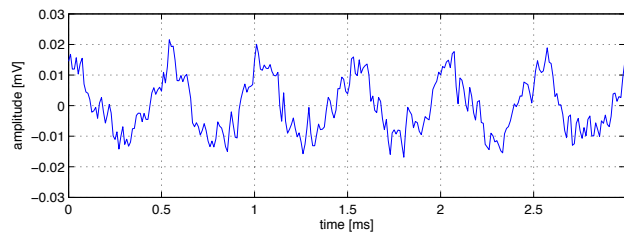
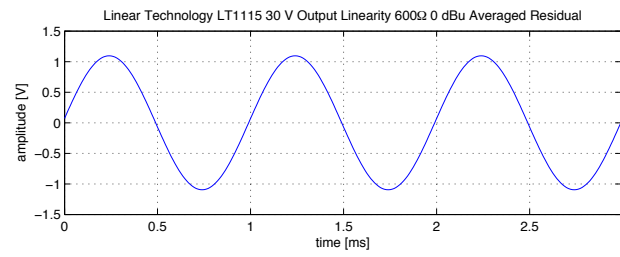
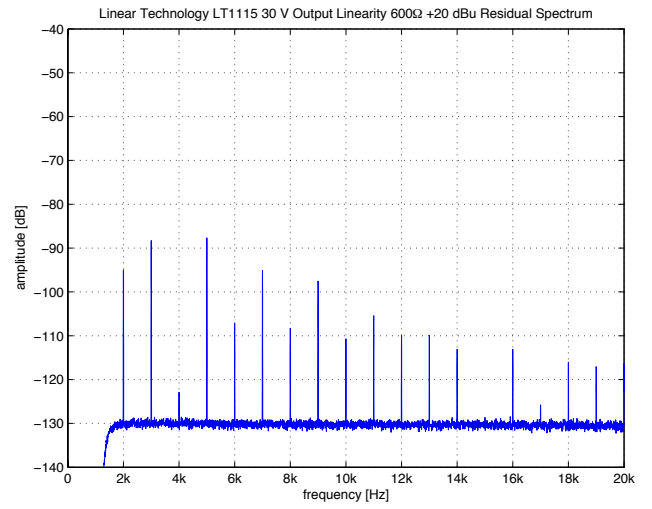
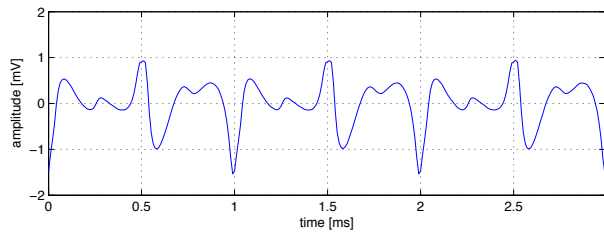
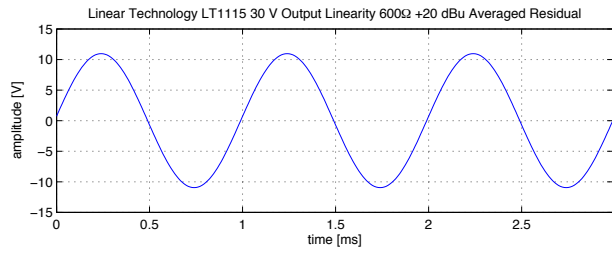
Graph Not Available

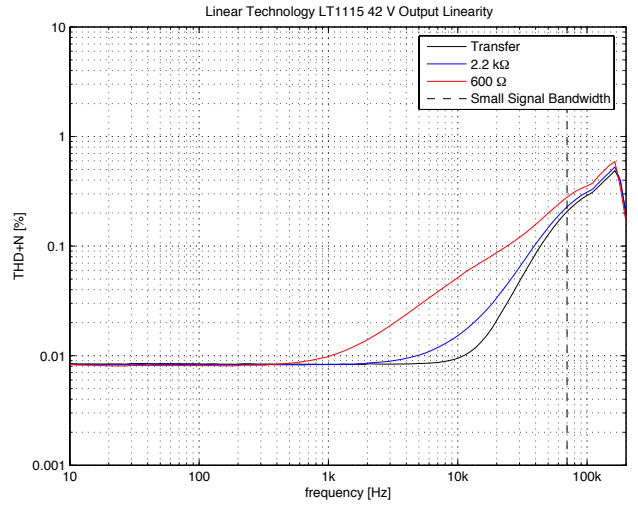
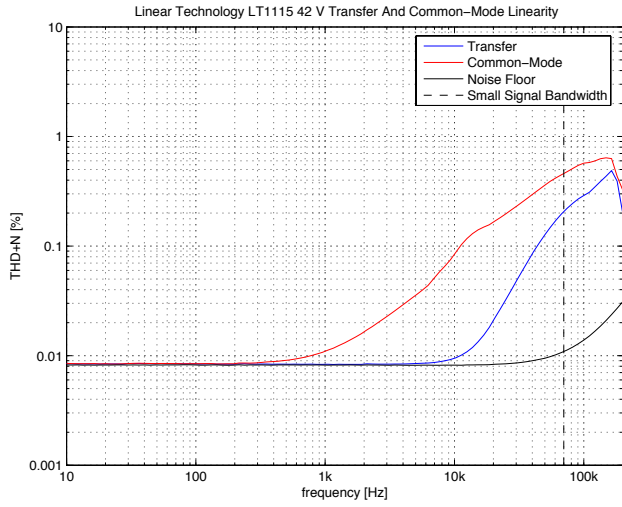




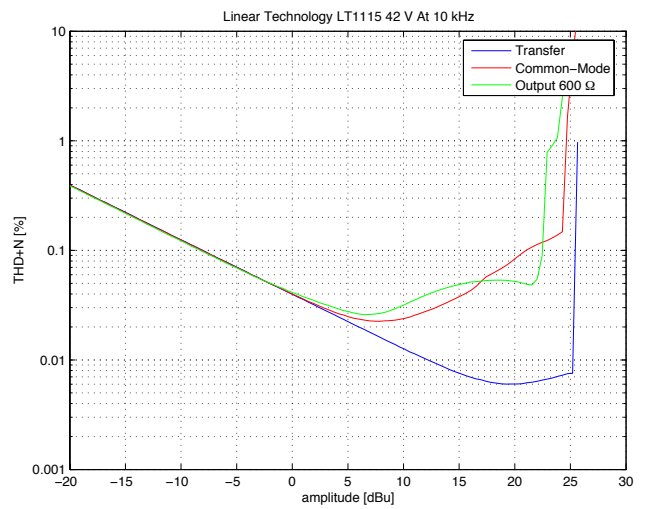
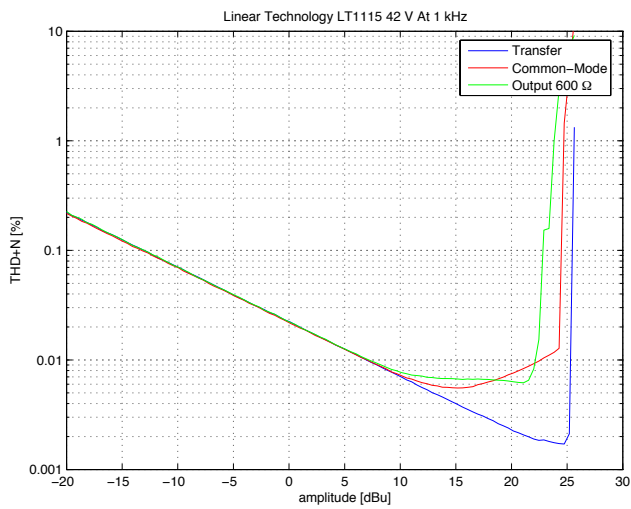
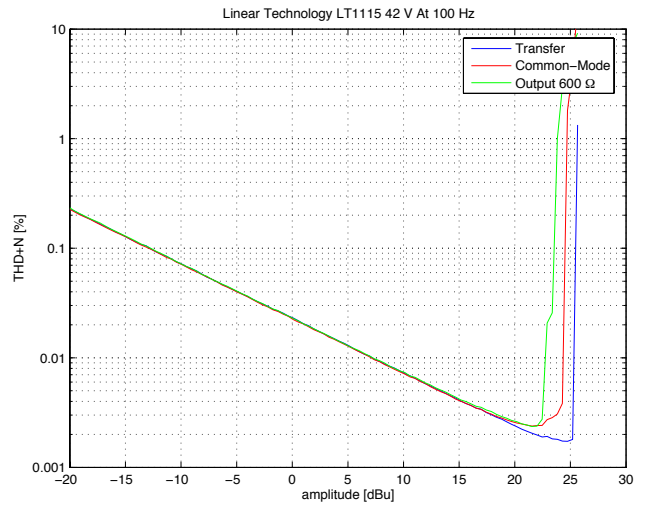


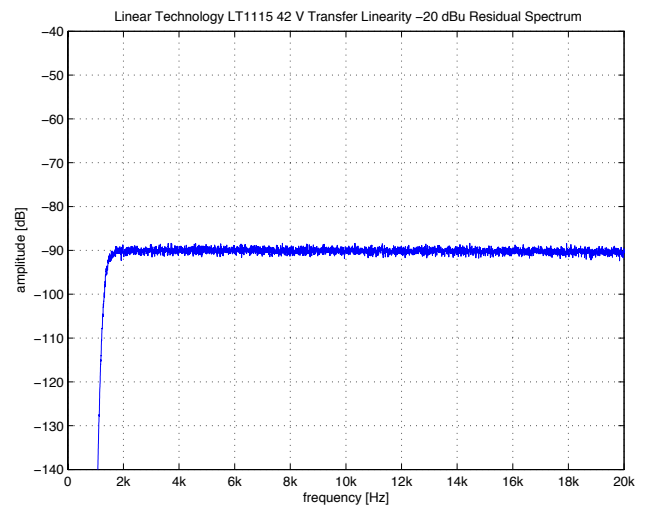
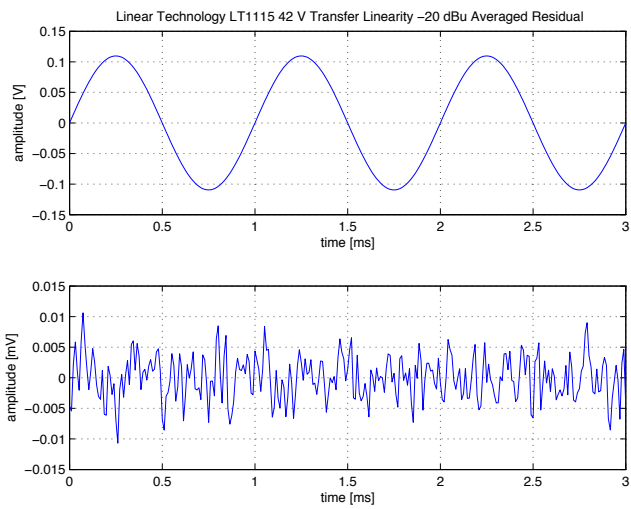
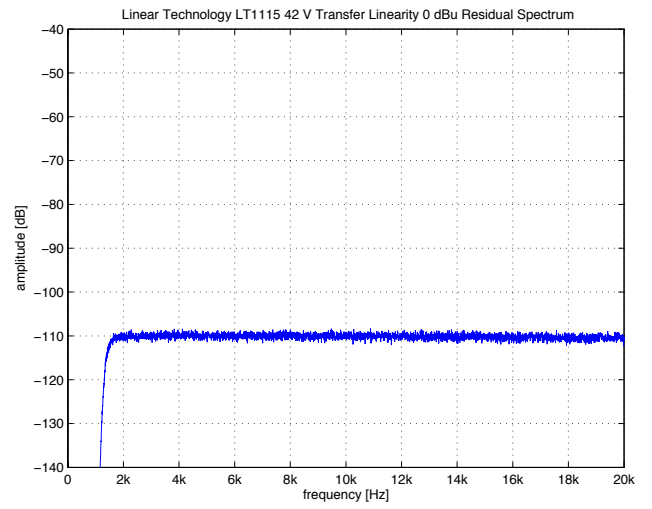
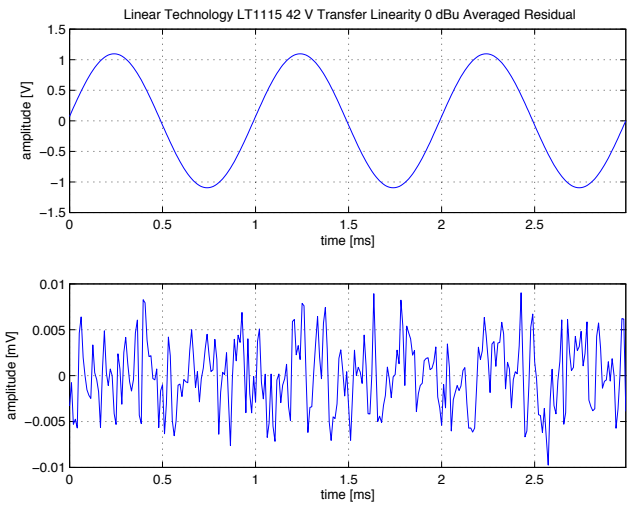
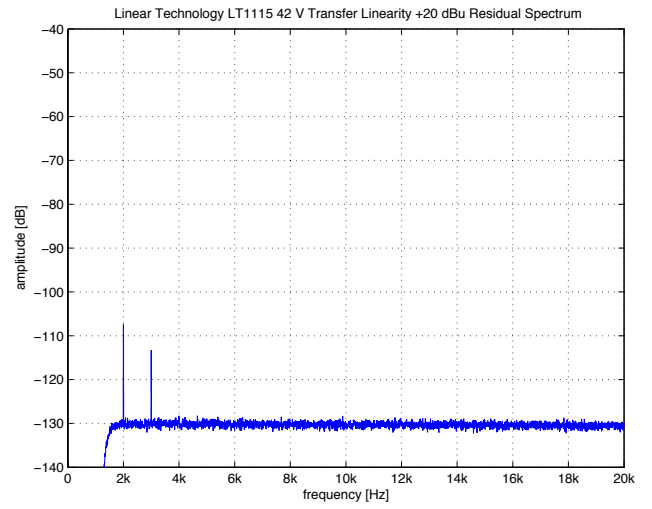
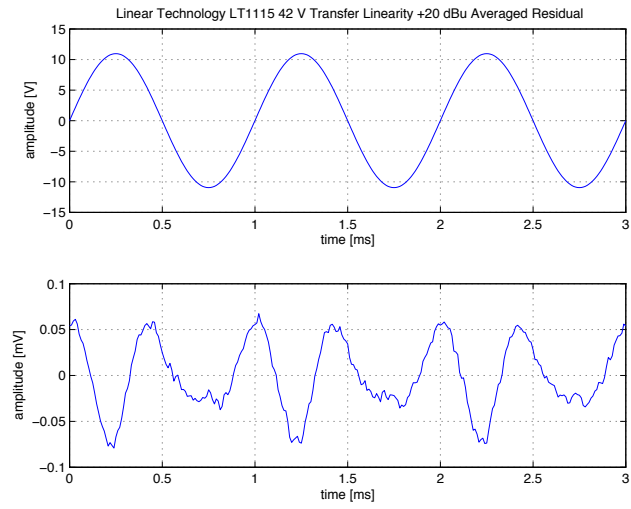


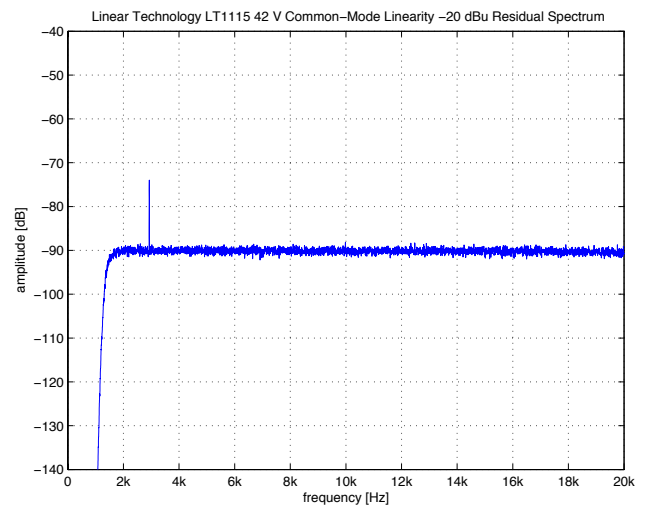
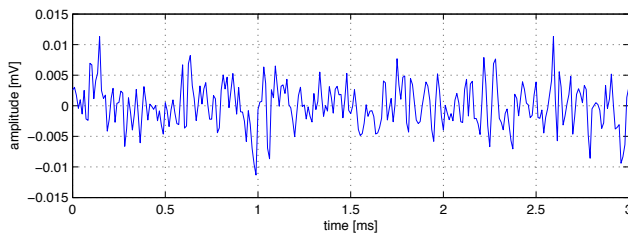
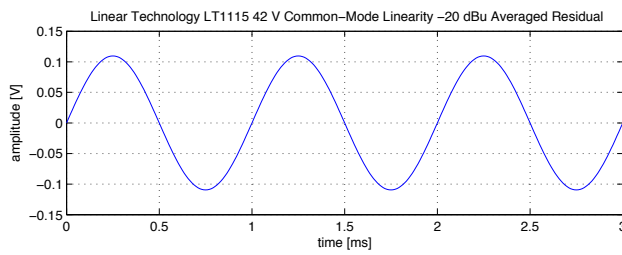
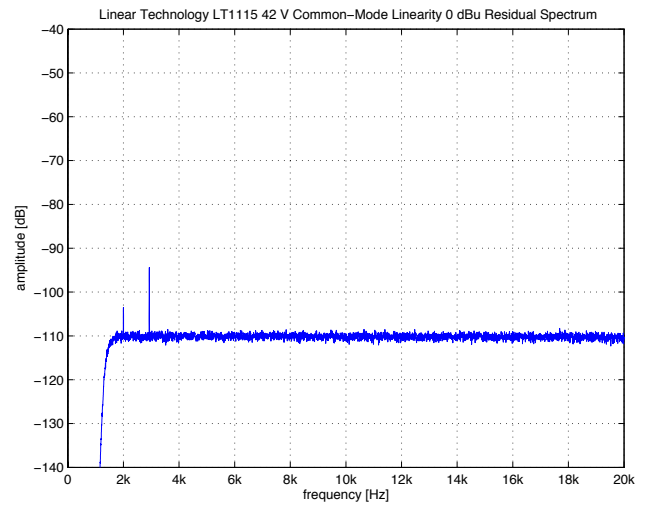
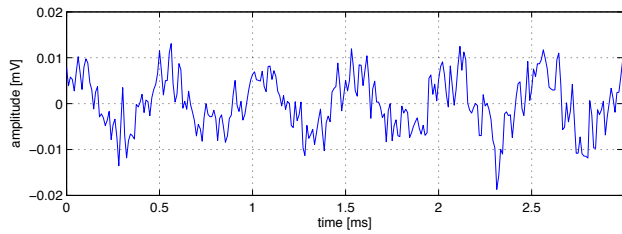
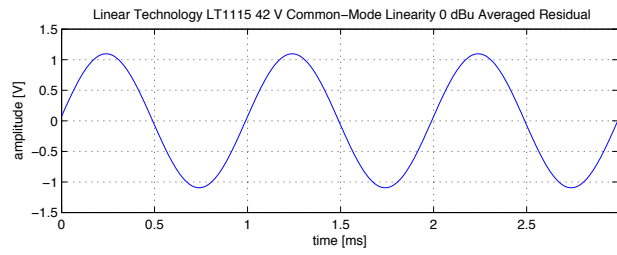
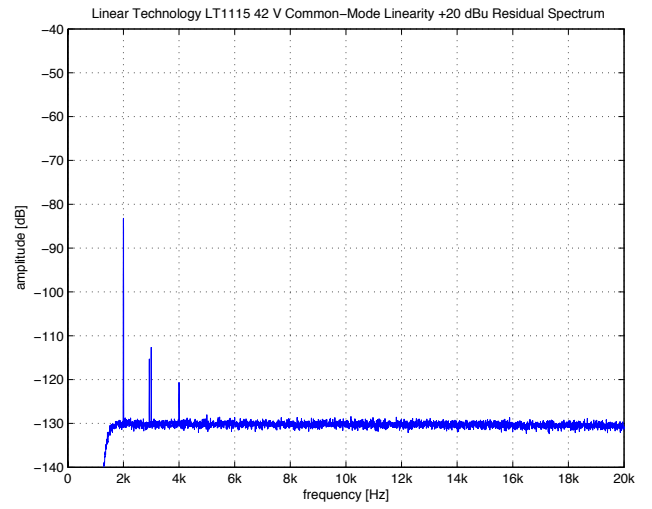
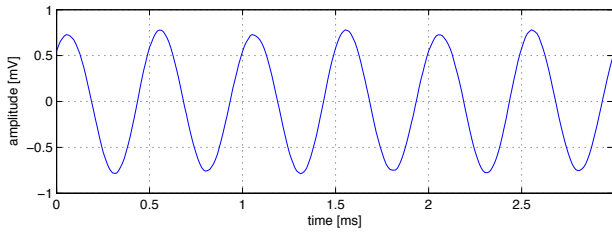
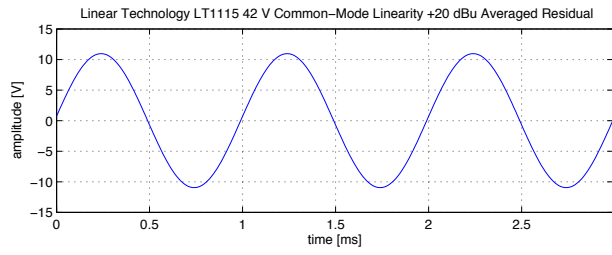


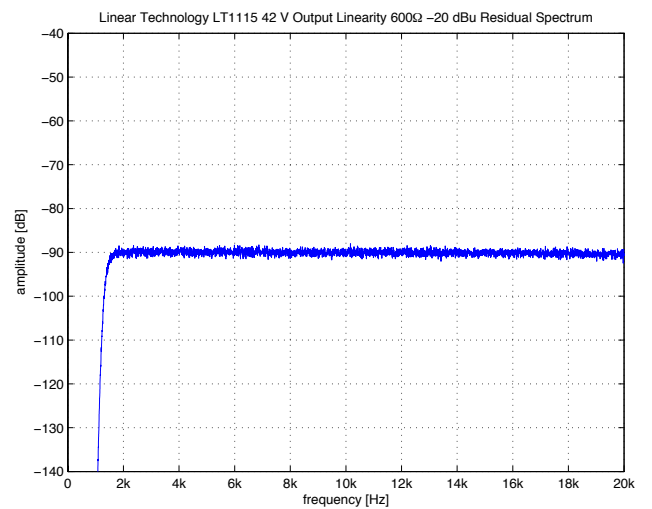
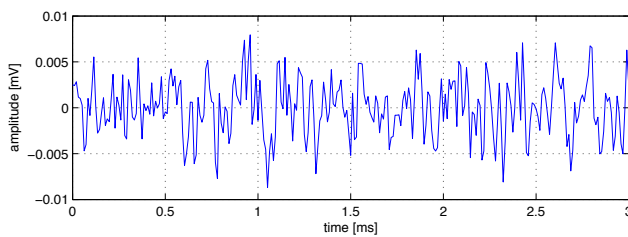
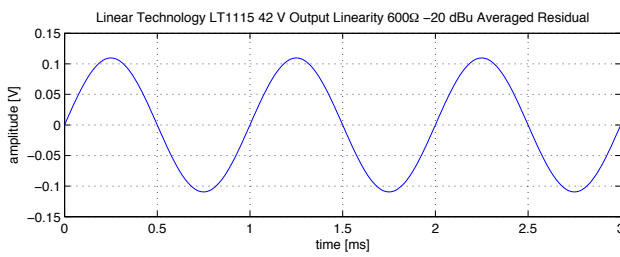
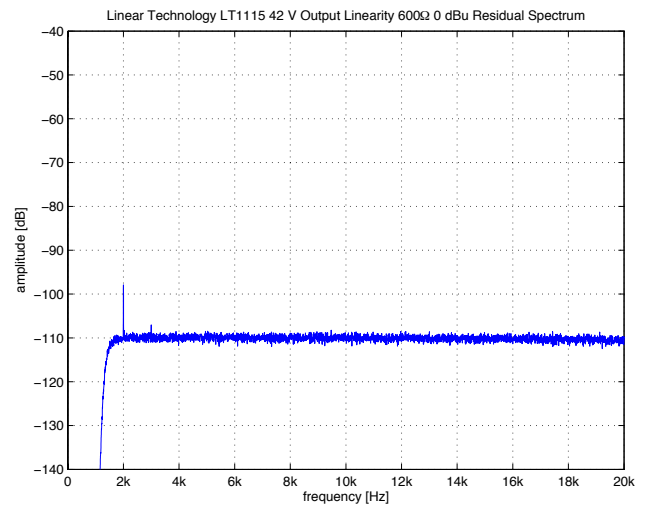
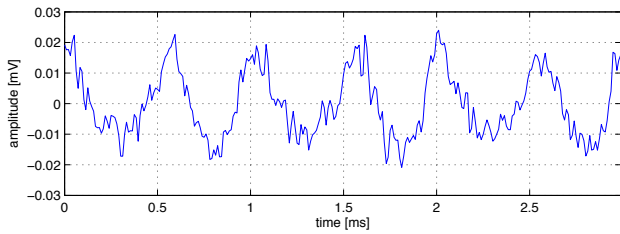
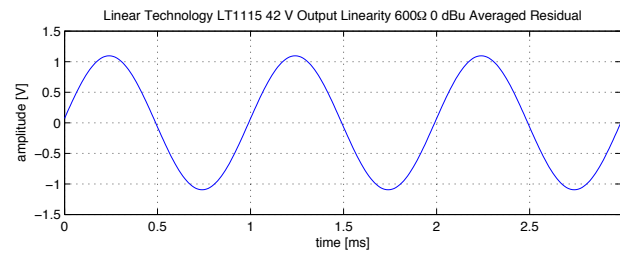
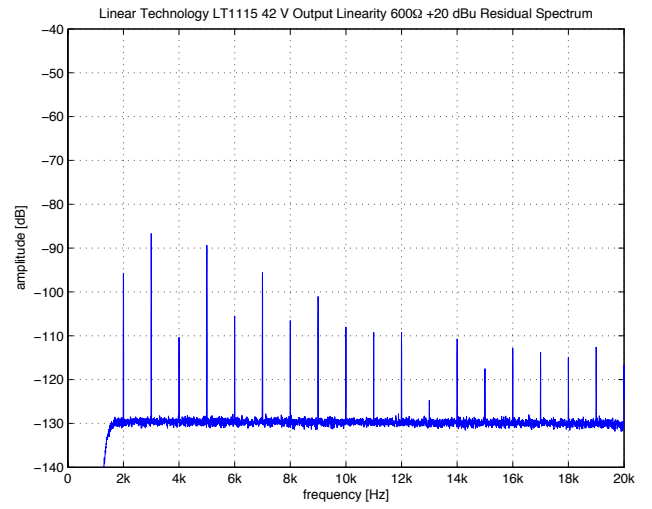
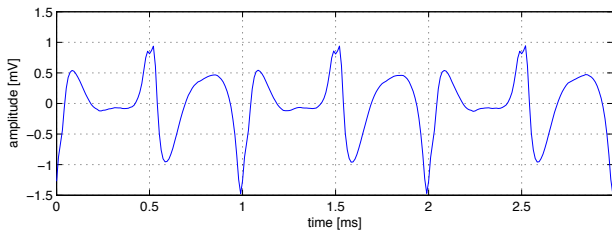
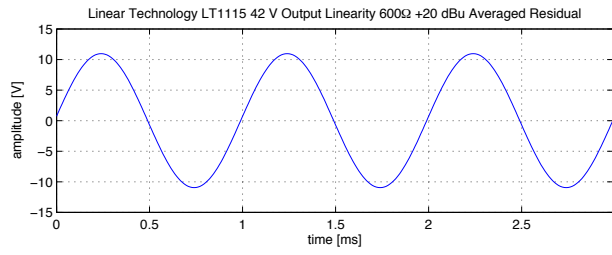


Graph Not Available









### 3.7 Linear Technology LT1124

<b>Number of Channels</b>	2
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	1.75 US\$ at 1k units (August 2008)

Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		25	100	$\mu\text{V}$
Input Bias Current		8	30	nA
Input Offset Current		6	20	nA
Gain Bandwidth Product	8	12.5		MHz
Slew-Rate	2.7	4.5		$\text{V}/\mu\text{S}$
Input Voltage Noise (f = 1 kHz)		2.7	4.5	$\text{nV}/\sqrt{\text{Hz}}$
Input Current Noise (f = 1 kHz)		0.3		$\text{pA}/\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 12$	$\pm 12.8$		V
Output Voltage Swing ( $R_L = 2 \text{ k}\Omega$ )	$\pm 12.5$	$\pm 13.8$		V
Power Supply Voltage			$\pm 22$	V
Quiescent Current per Amplifier		2.3	2.75	mA

Table 3.7: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 15 \text{V}$ .

This operational amplifier is based on a three-stage architecture with BJT inputs and offers very good DC precision. Both voltage and current noise are low.

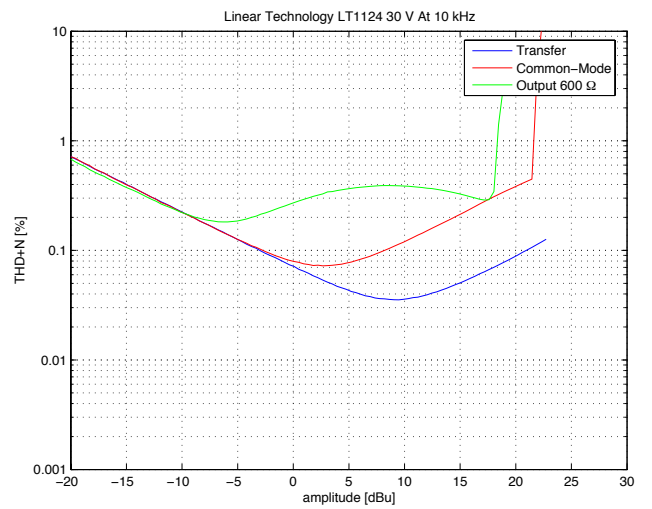
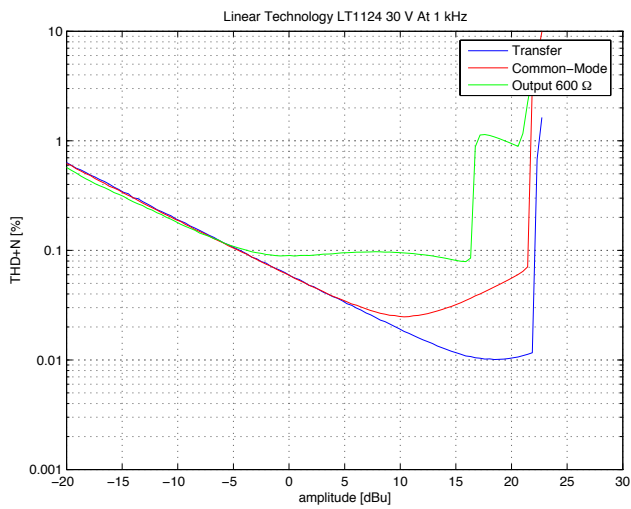
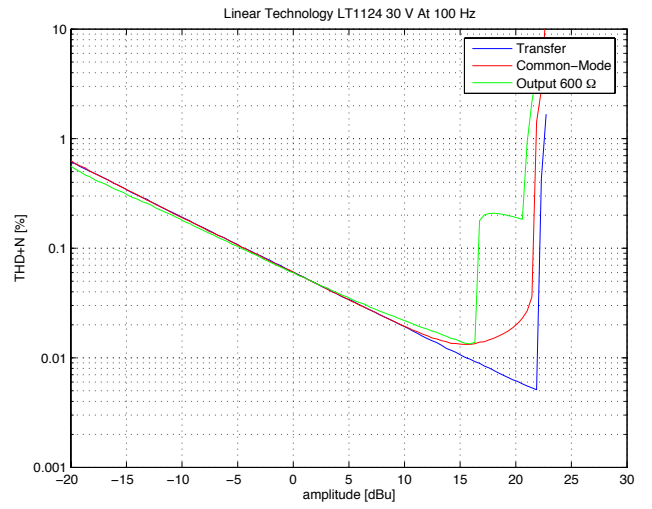
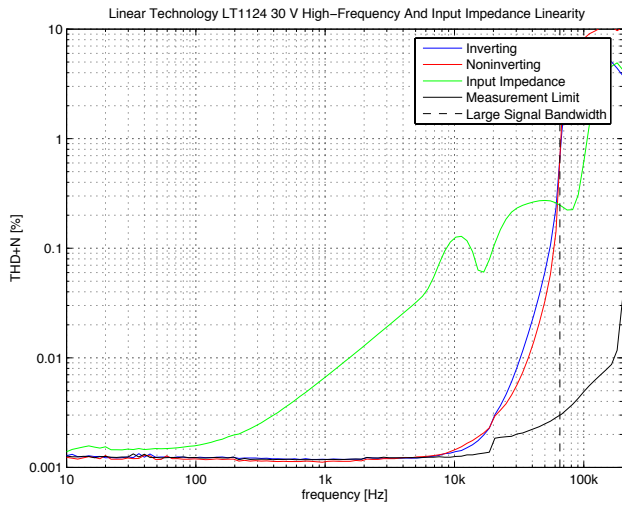
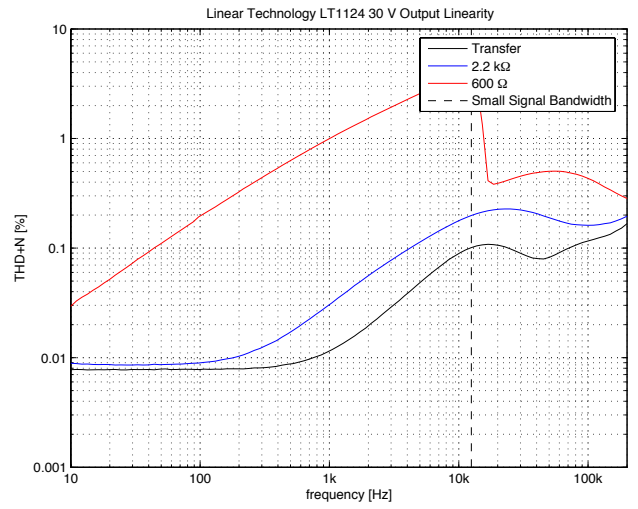
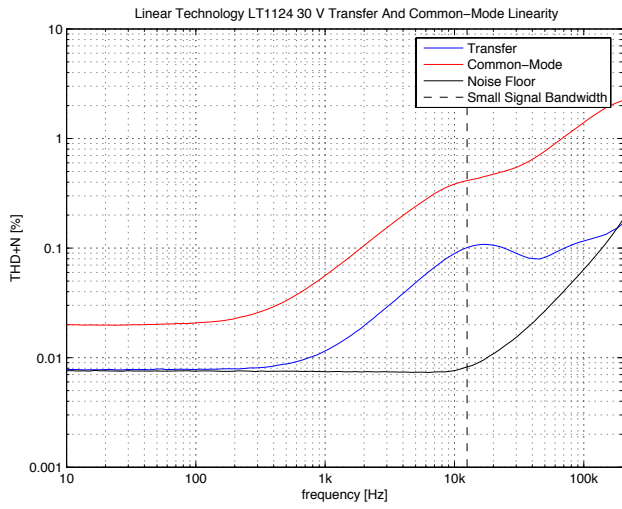
The basic transfer linearity is excellent at low frequencies but quickly degrades at higher frequencies due to the limited speed of the amplifier. Common-mode distortion causes a substantial decrease in linearity; the input impedance linearity shows for IC amplifiers typical values. The output stage suffers from some sudden distortion increase at a specific level (about +16.5 dBu), which is probably caused by an internal stage running out of current while driving the output transistors.<sup>5</sup> However even at lower levels there is significant distortion from output loading. Higher supply voltages do not considerably improve observed distortion. Unfortunately there has been some substantial interference of unknown origin during the measurement time of some of the FFT plots which makes reading the according graphs somewhat cumbersome.

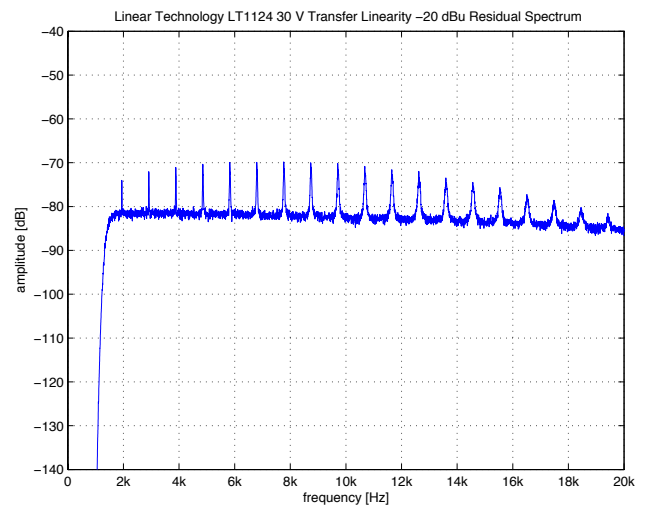
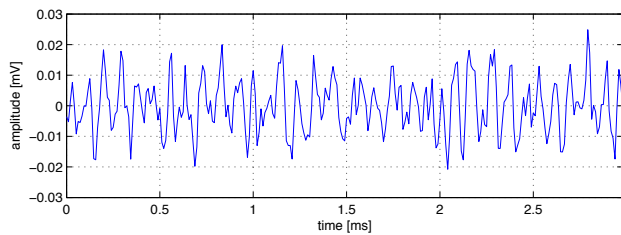
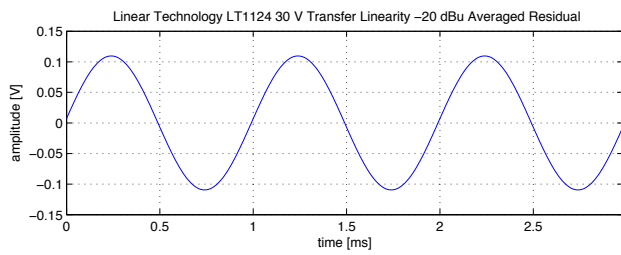
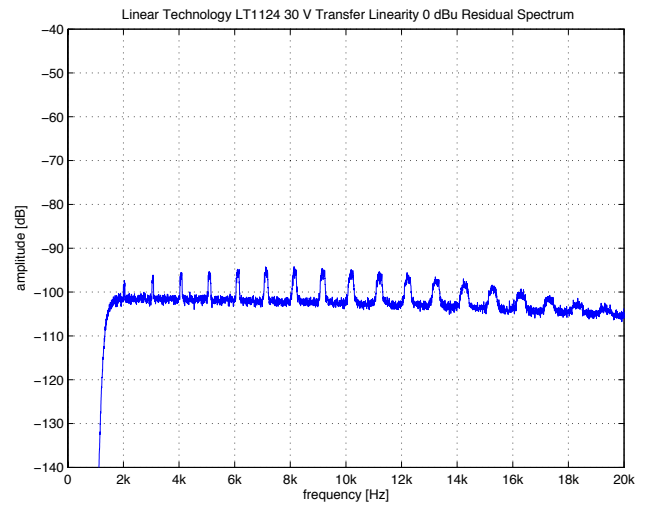
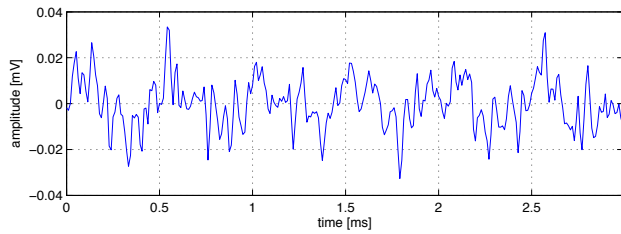
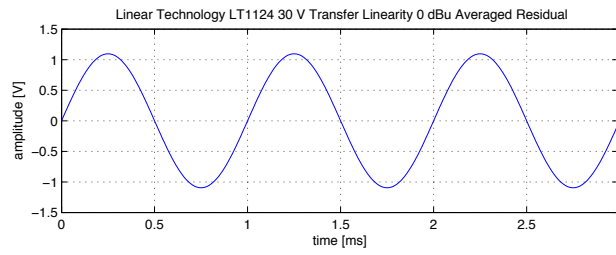
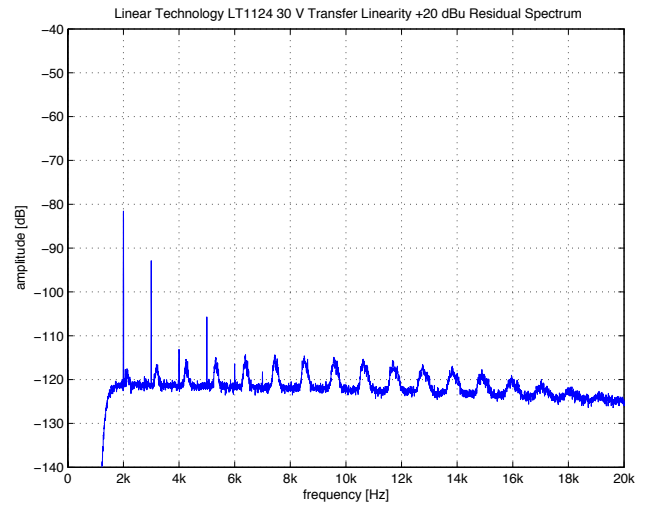
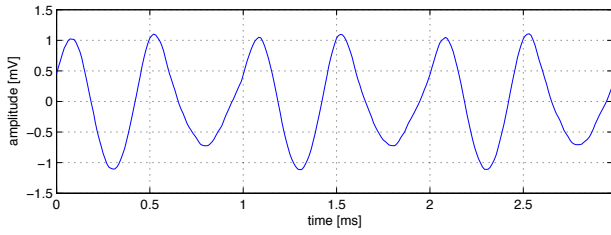
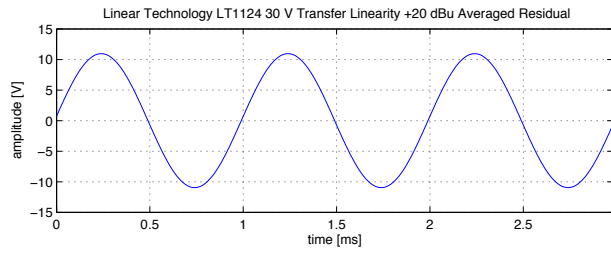
Perhaps usefull for its DC precision at lower supply voltages where slew-induced distortion is less troublesome and the output can be operated below the mysterious “distortion step” or preferably even at light loading only.

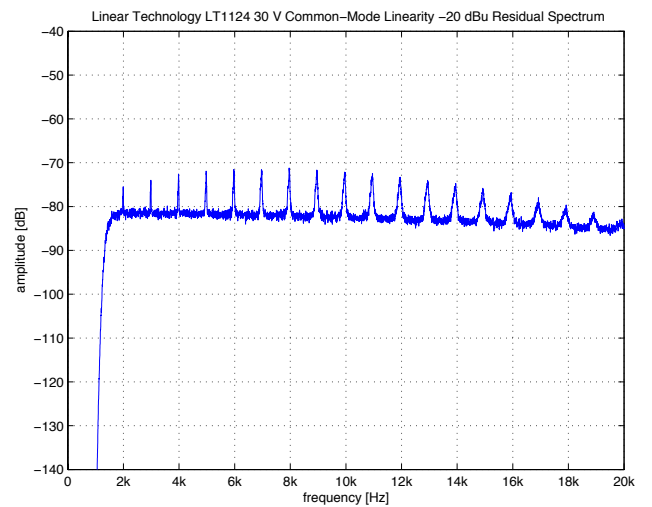
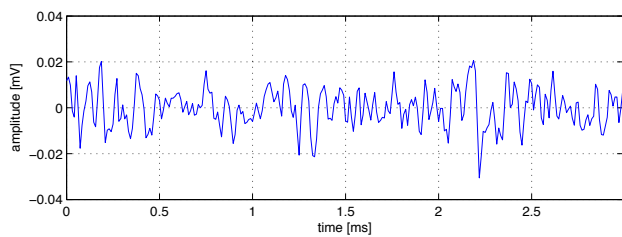
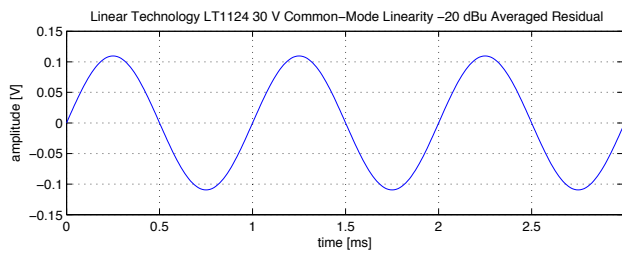
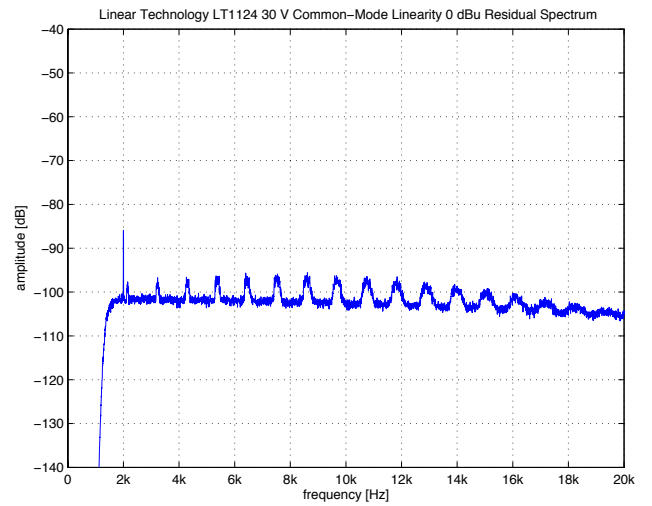
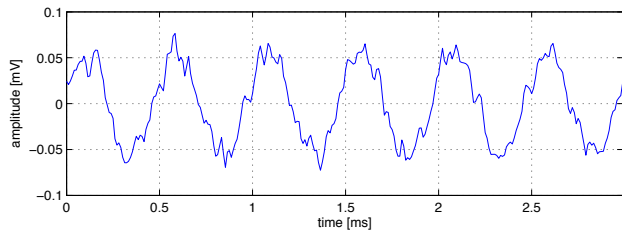
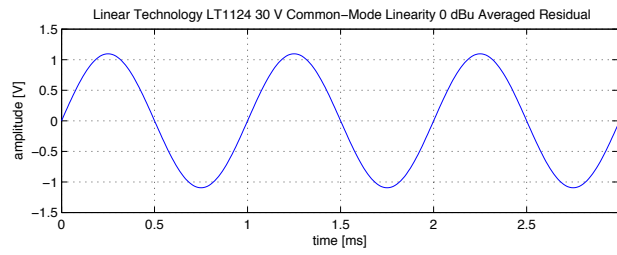
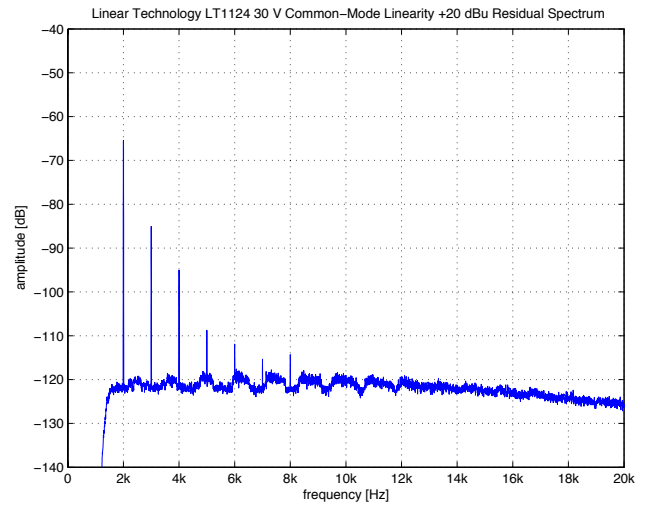
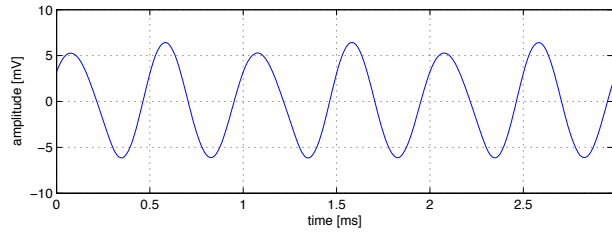
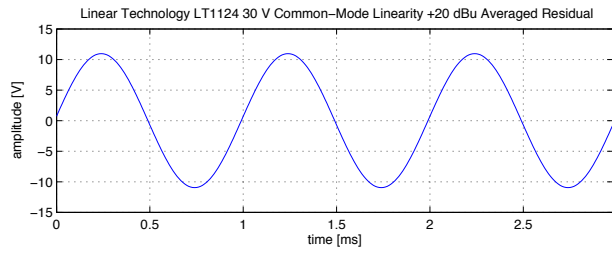
<sup>5</sup>Q25/Q26 as shown in the manufacturer’s datasheet look suspicious—their  $100 \mu\text{A}/200 \mu\text{A}$  collector current seems not to be enough to reliably drive the output transistors (Q28/Q29) at higher output currents.

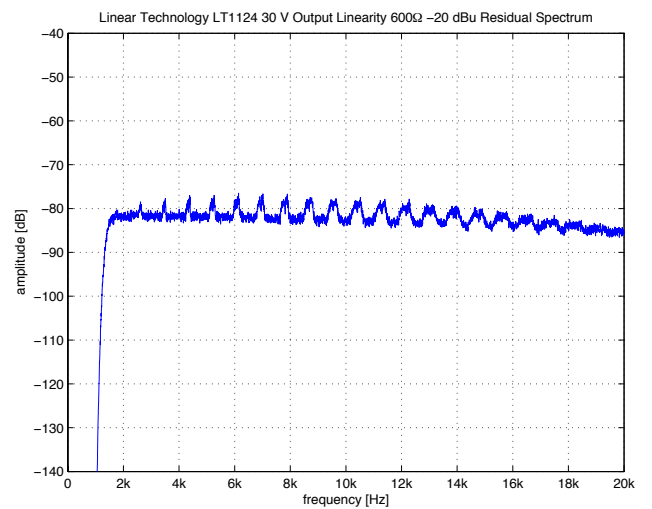
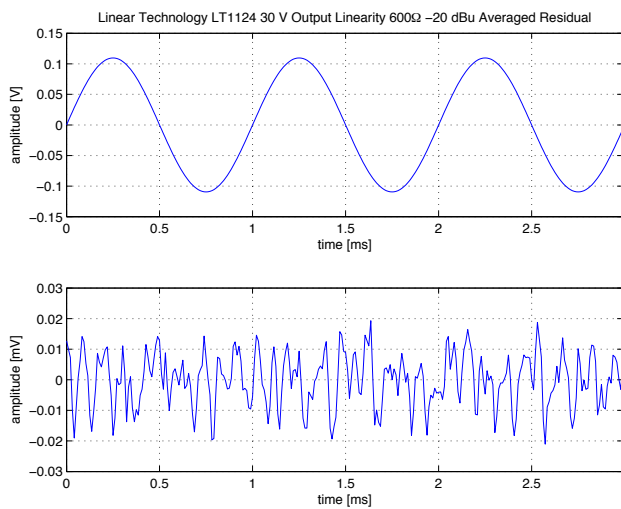
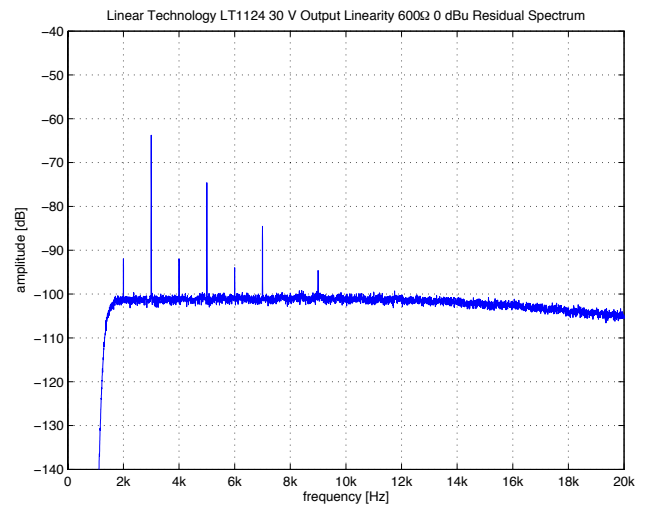
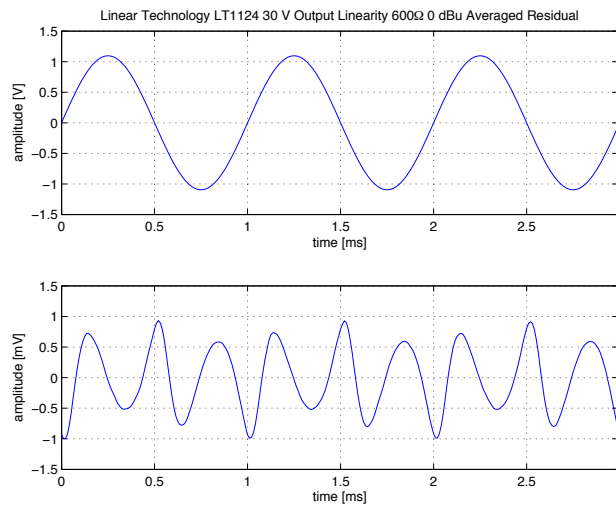
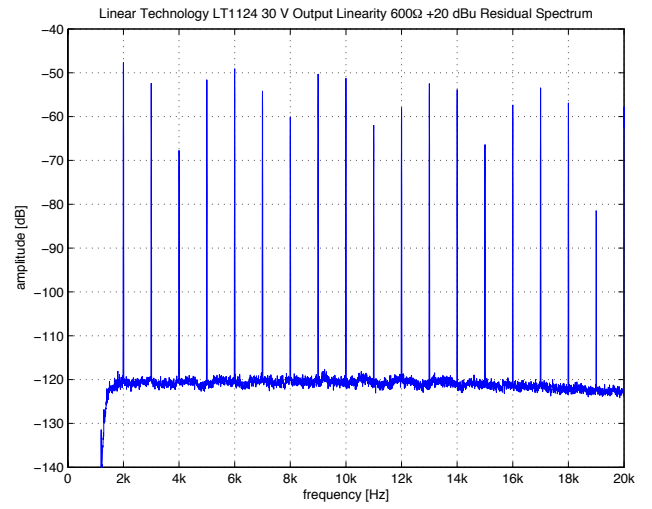
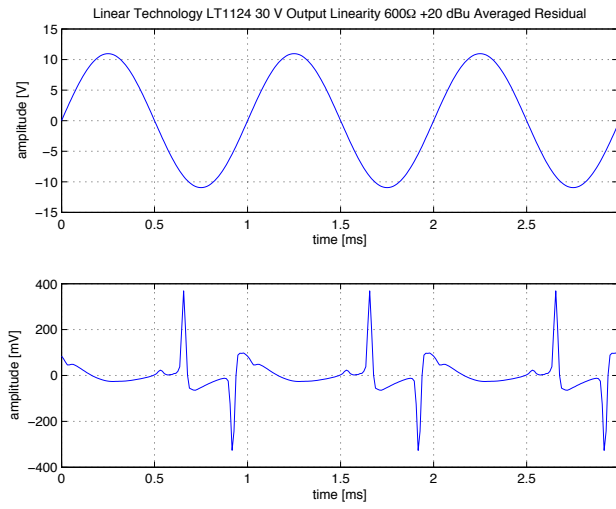
Otherwise there are lower distortion opamps out there at similar or even lower price tag.

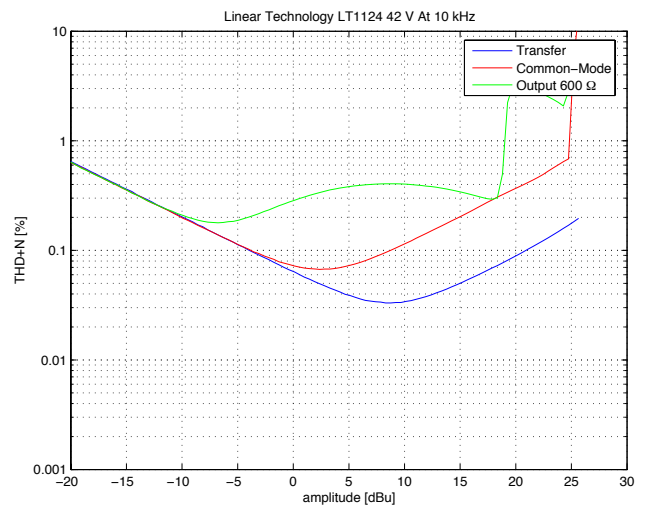
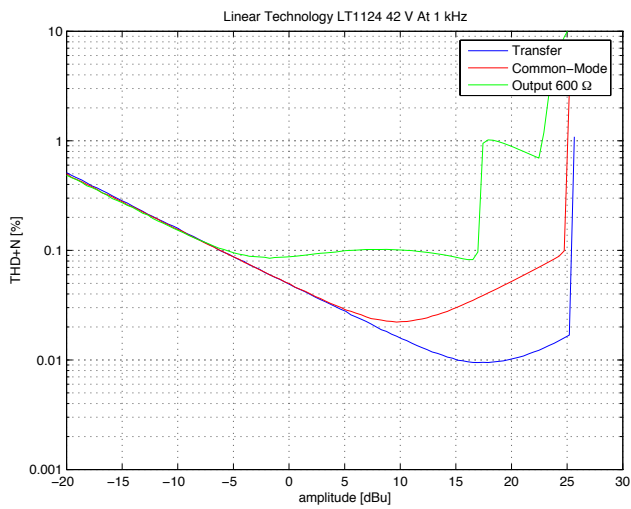
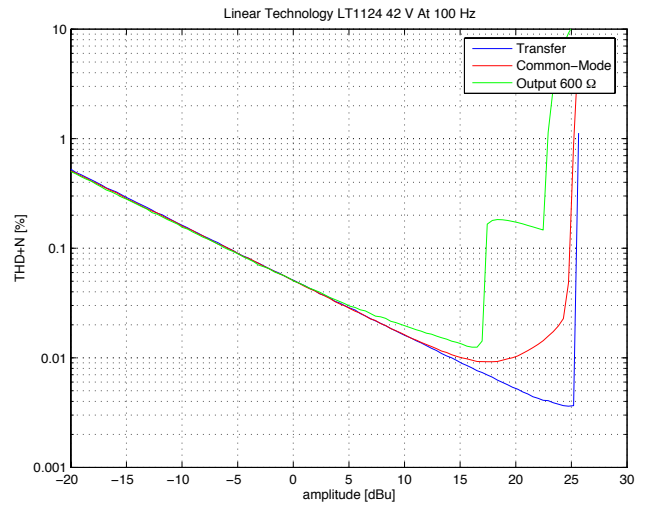
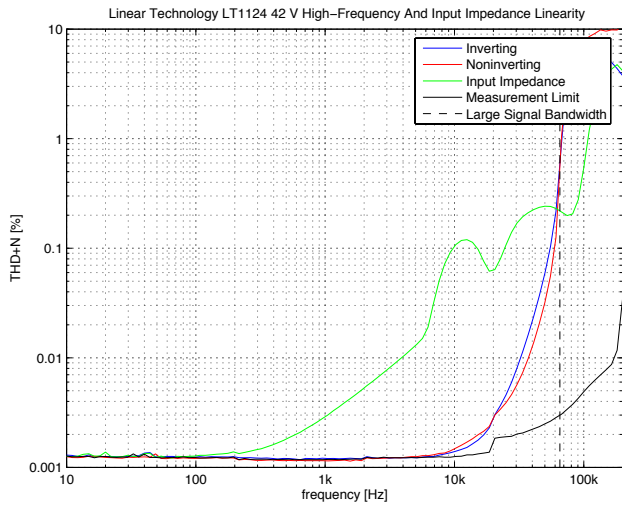
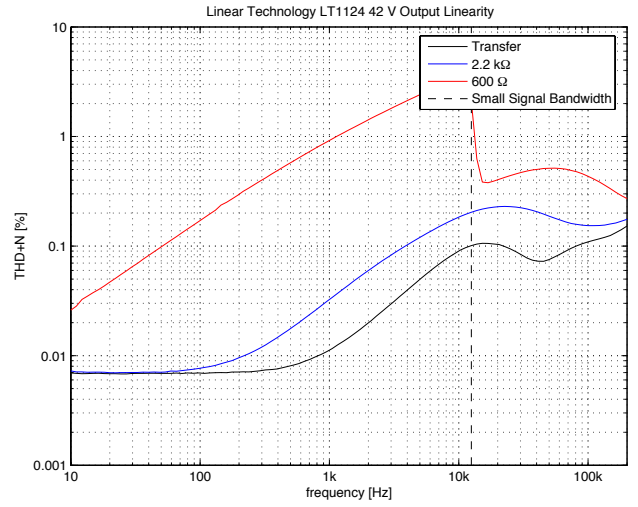
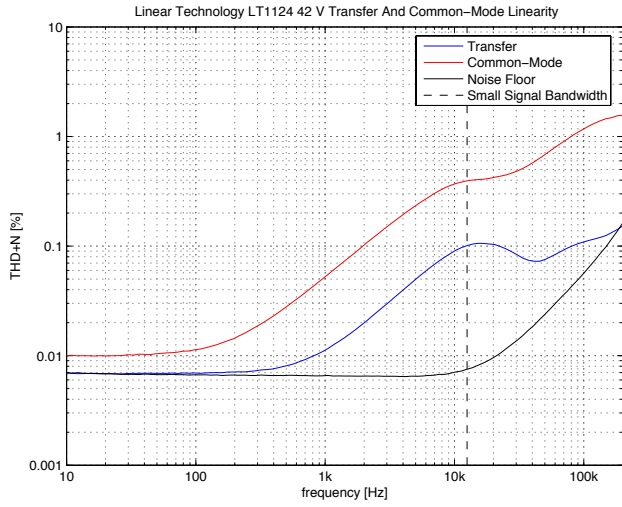


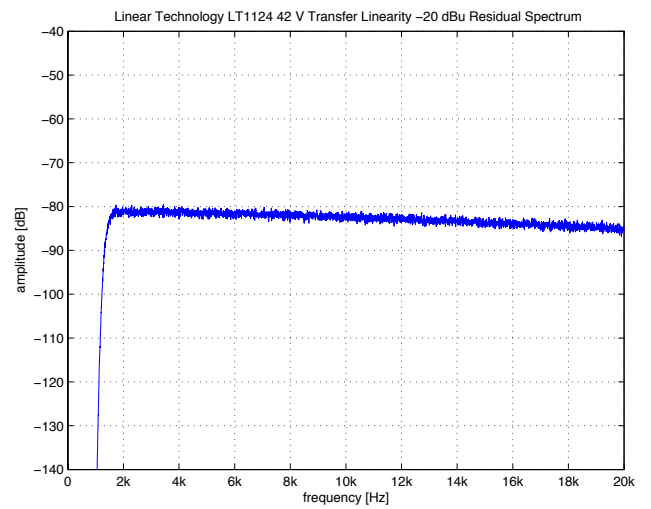
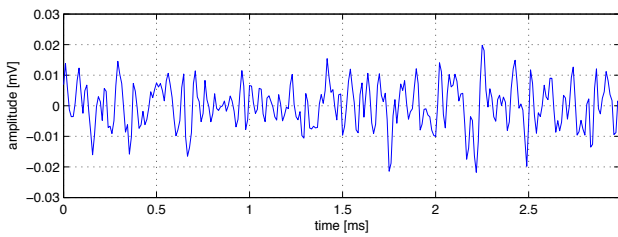
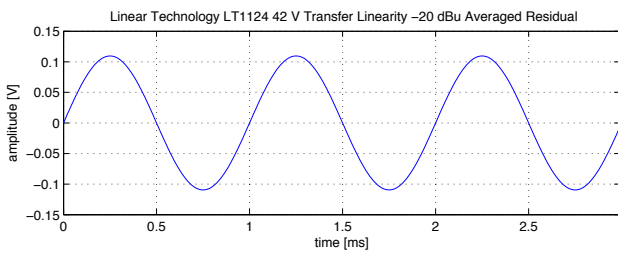
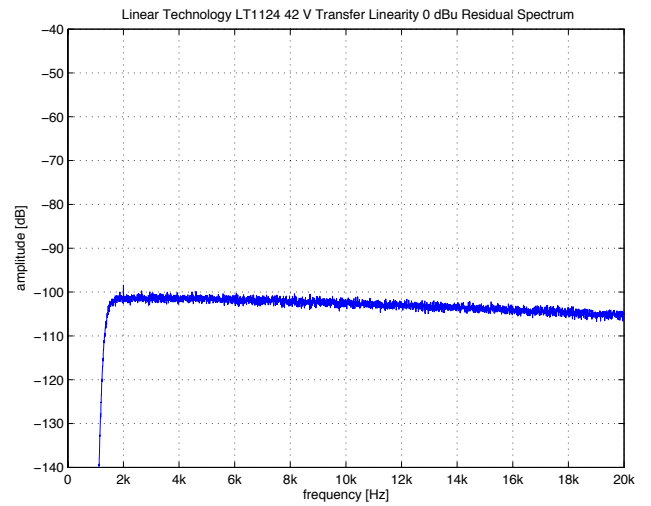
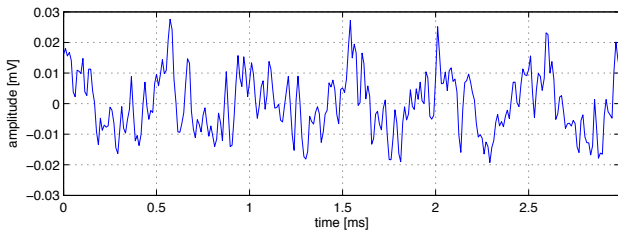
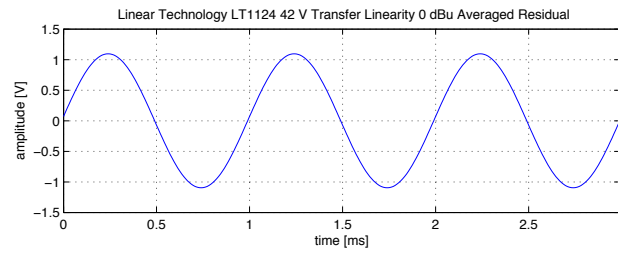
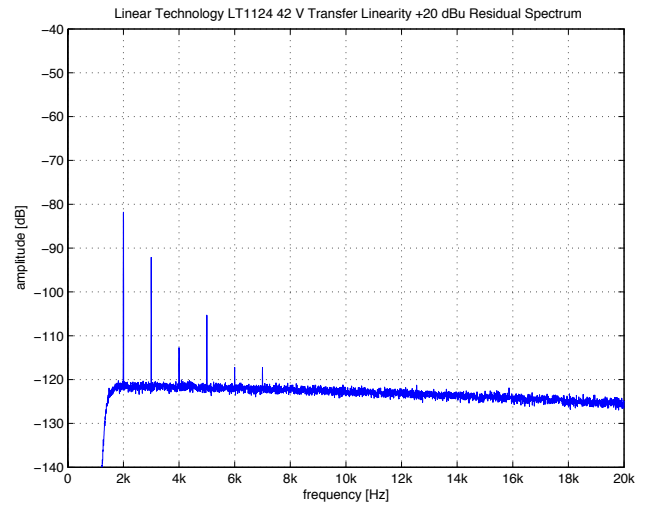
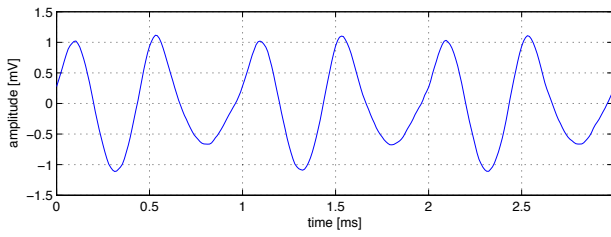
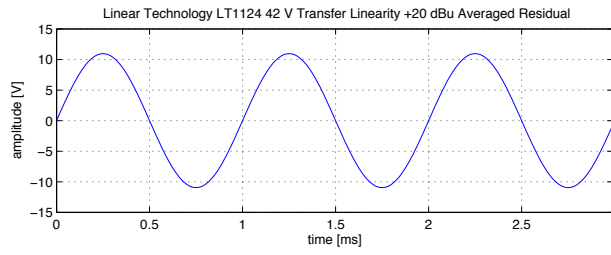


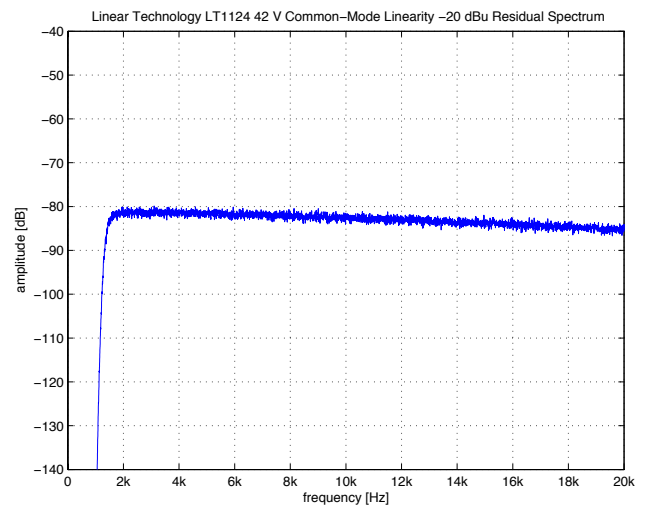
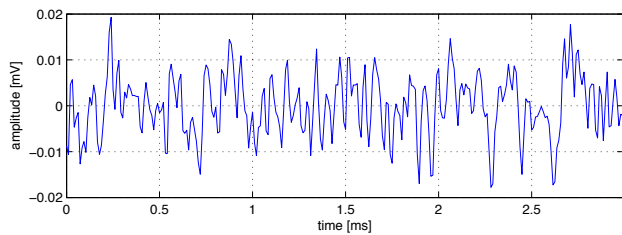
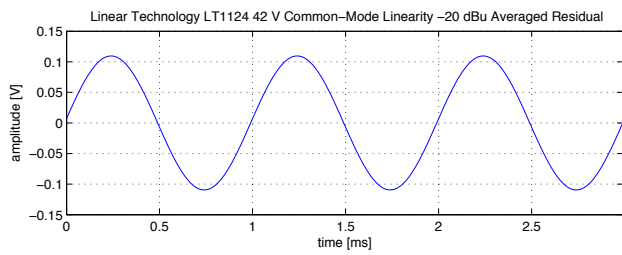
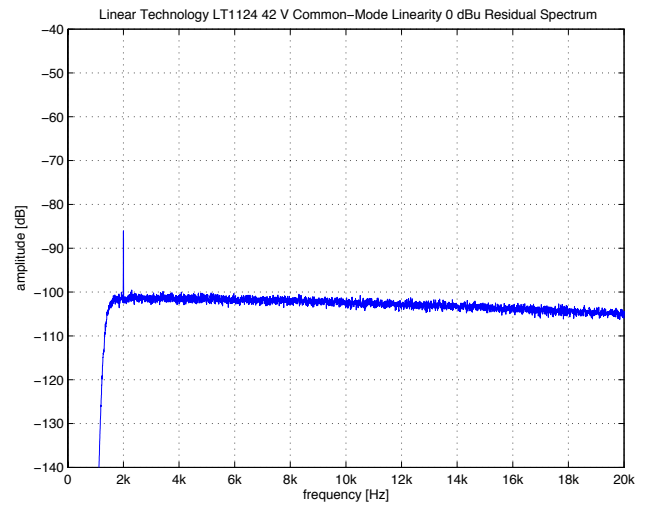
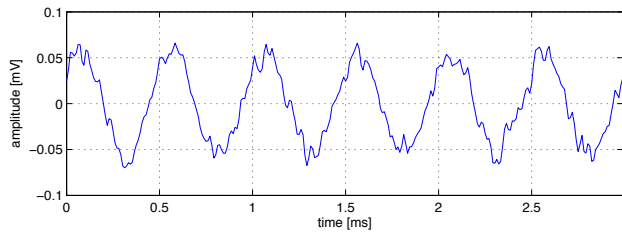
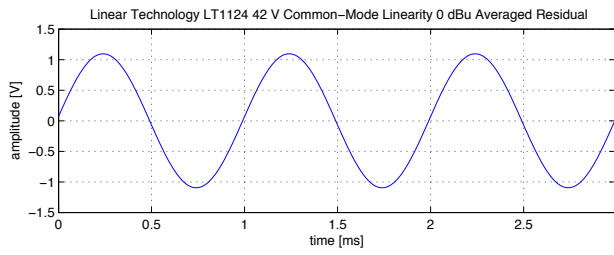
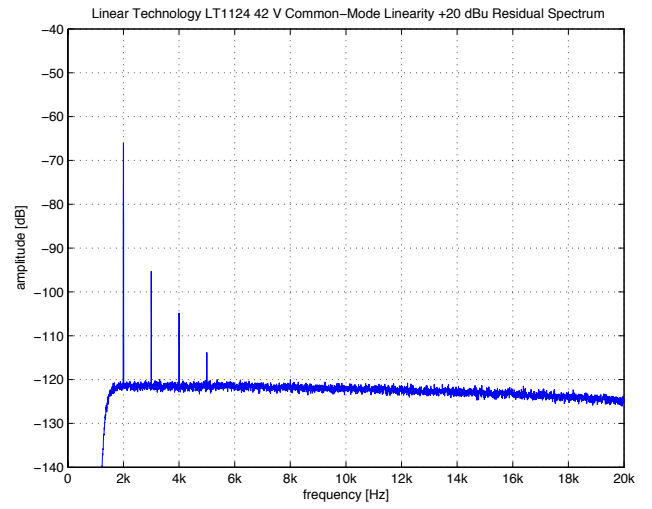
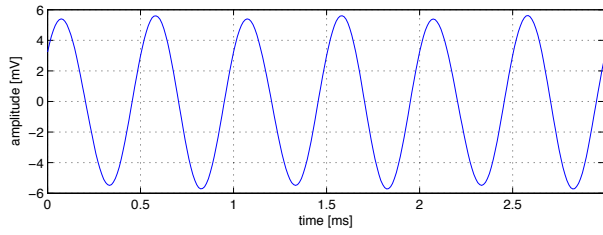
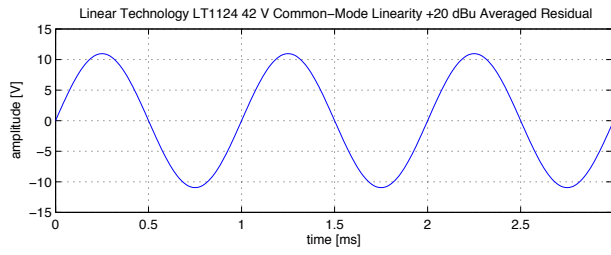


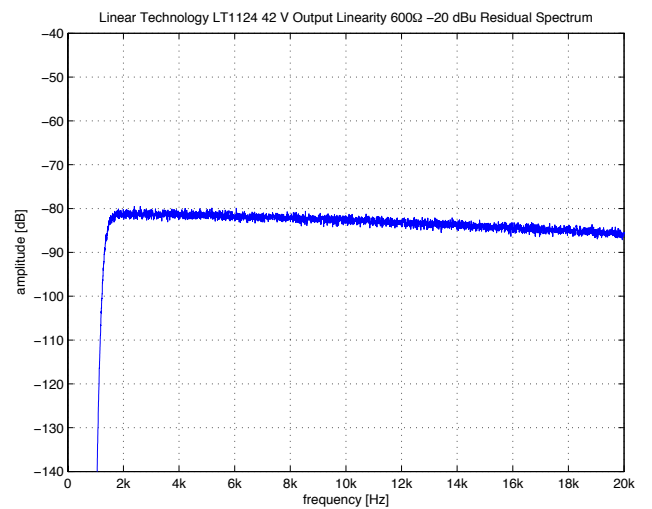
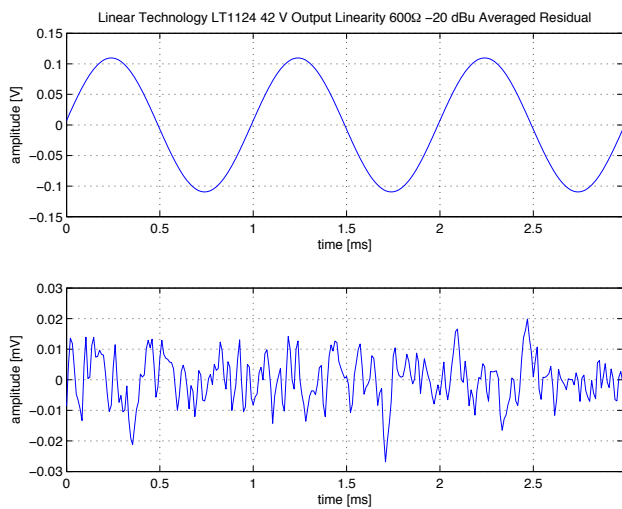
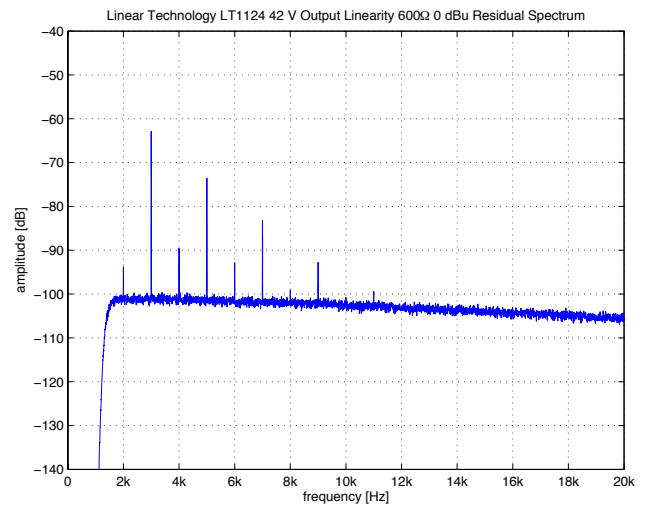
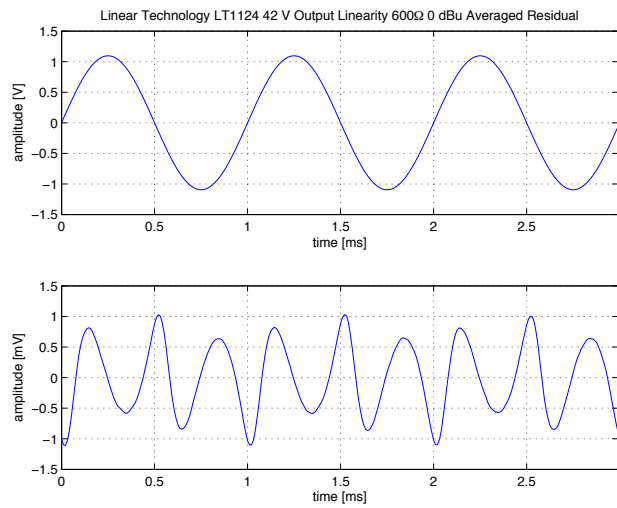
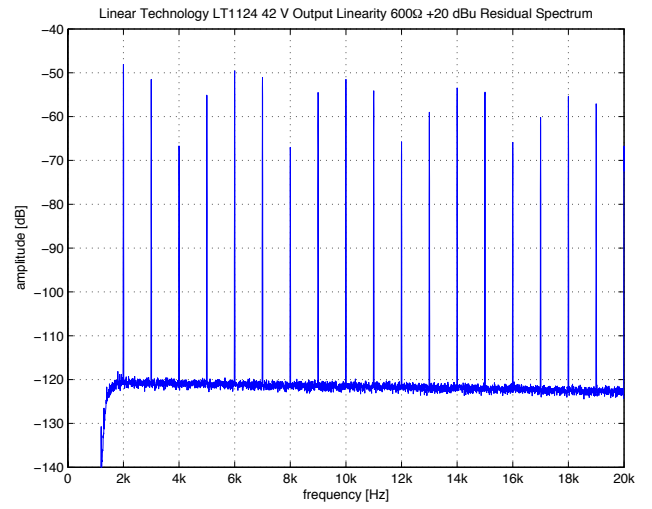
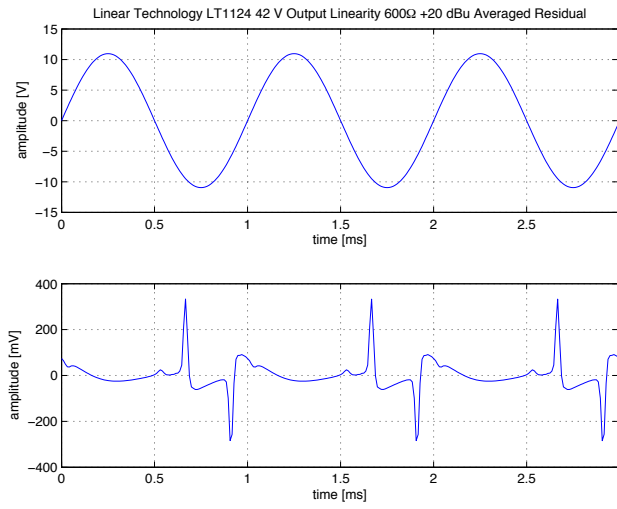














### 3.8 Linear Technology LT1122

<b>Number of Channels</b>	1
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	2.45 US\$ at 1k units (July 2008)

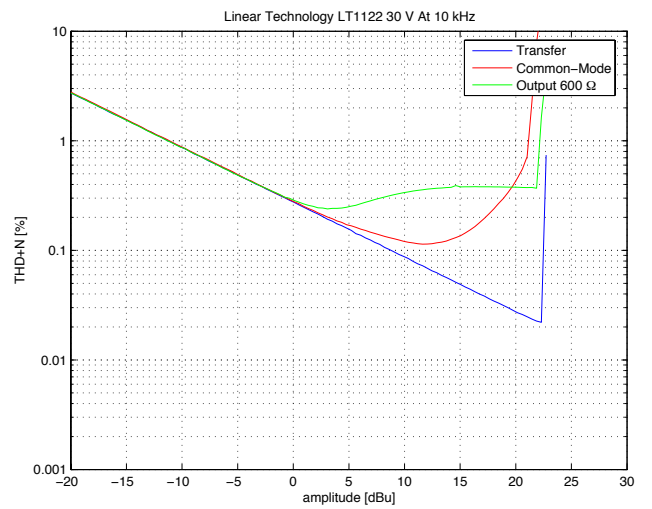
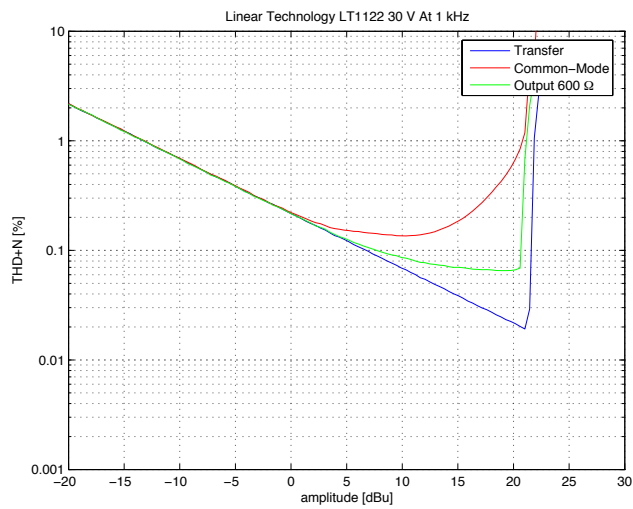
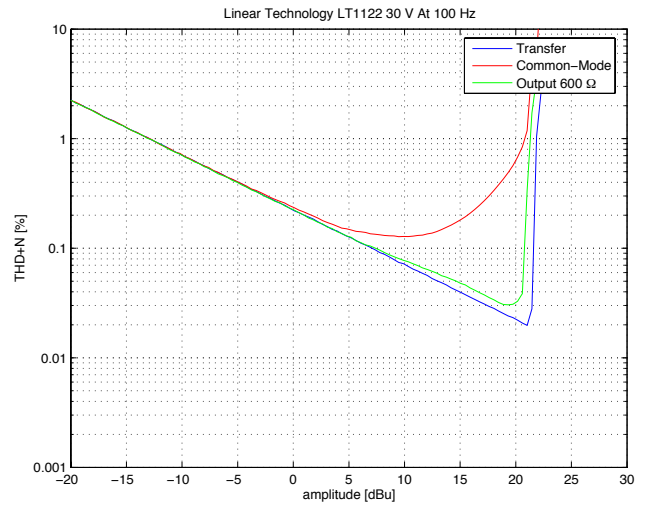
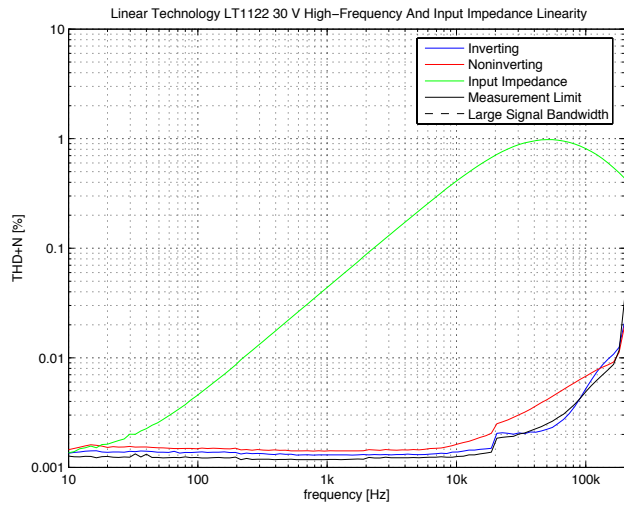
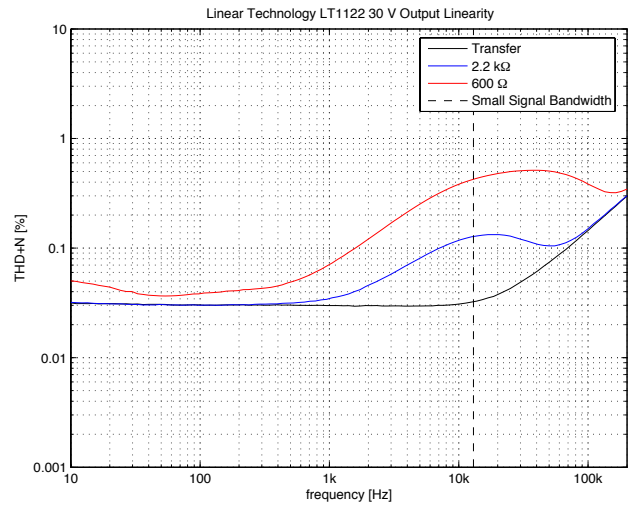
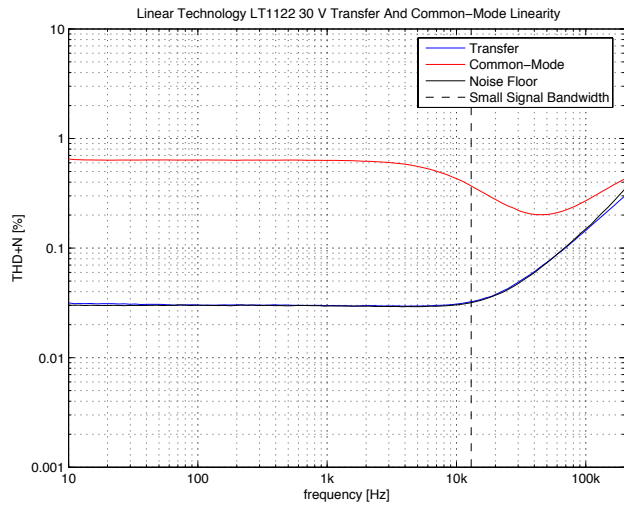
Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		130	900	$\mu\text{V}$
Input Bias Current		12	100	pA
Input Offset Current		5	50	pA
Gain Bandwidth Product		13		MHz
Slew-Rate	50	75		V/ $\mu\text{S}$
Input Voltage Noise (f = 10 kHz)		15		nV/ $\sqrt{\text{Hz}}$
Input Current Noise (f = 1 kHz)		2		fA/ $\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 10.5$	$\pm 11$		V
Output Voltage Swing ( $R_L = 2 \text{ k}\Omega$ )	$\pm 12$	$\pm 12.5$		V
Output Voltage Swing ( $R_L = 600 \Omega$ )	$\pm 11.5$	$\pm 12$		V
Power Supply Voltage	$\pm 5$		$\pm 20$	V
Quiescent Current per Amplifier		7.8	11	mA

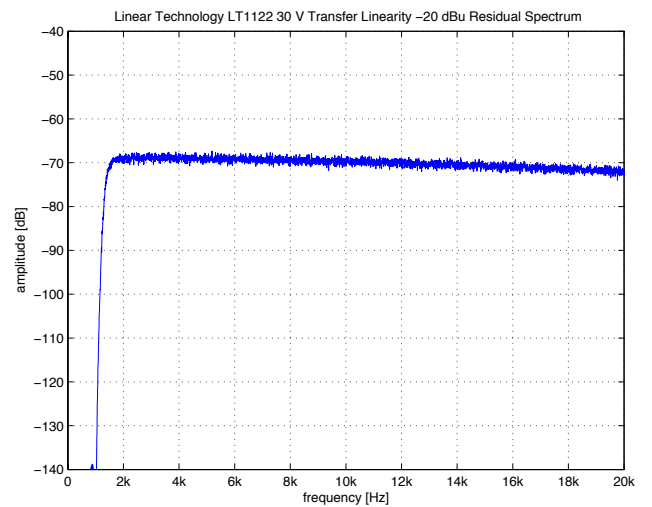
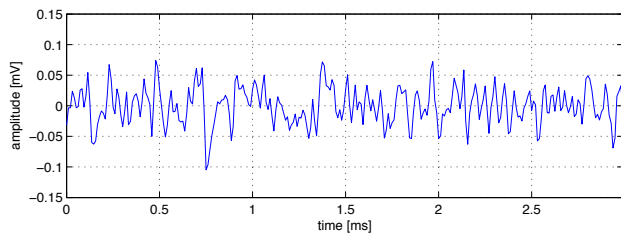
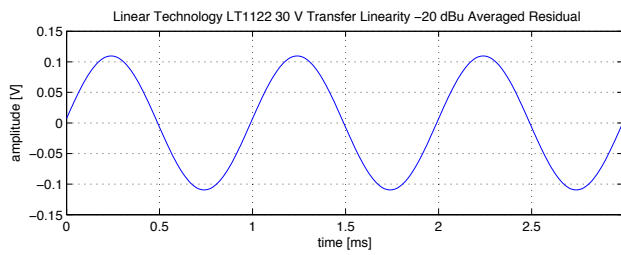
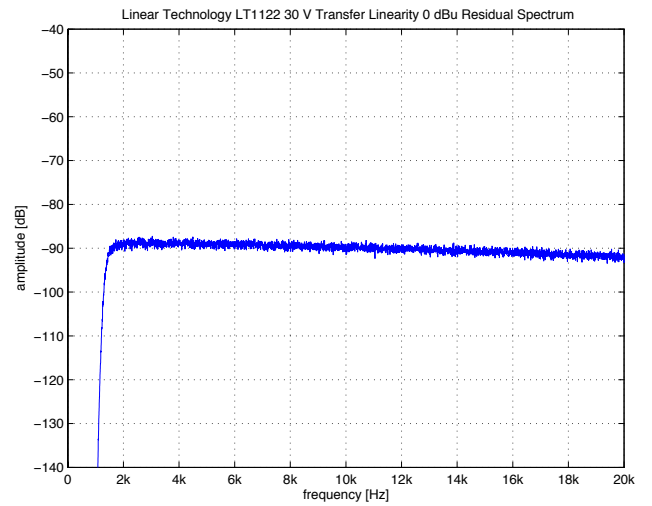
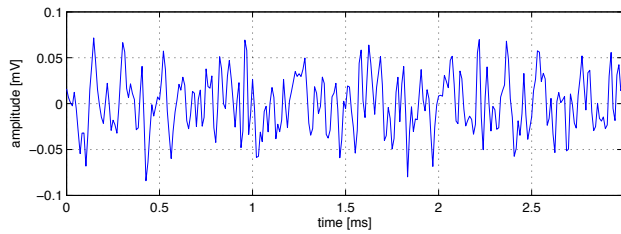
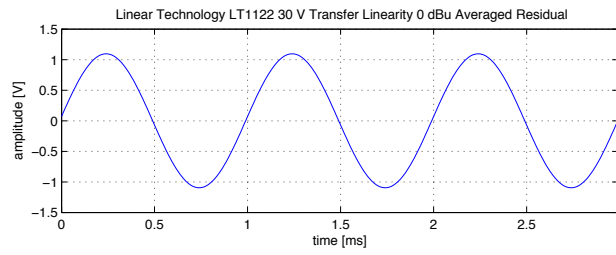
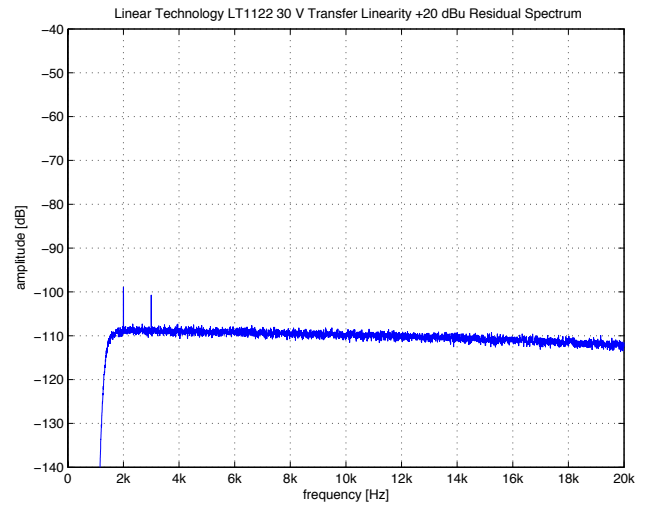
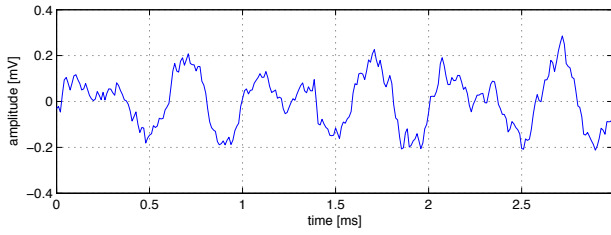
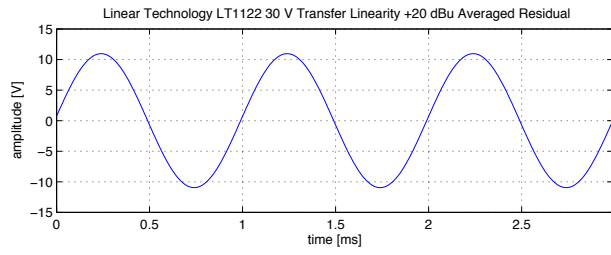
Table 3.8: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 15 \text{V}$ .

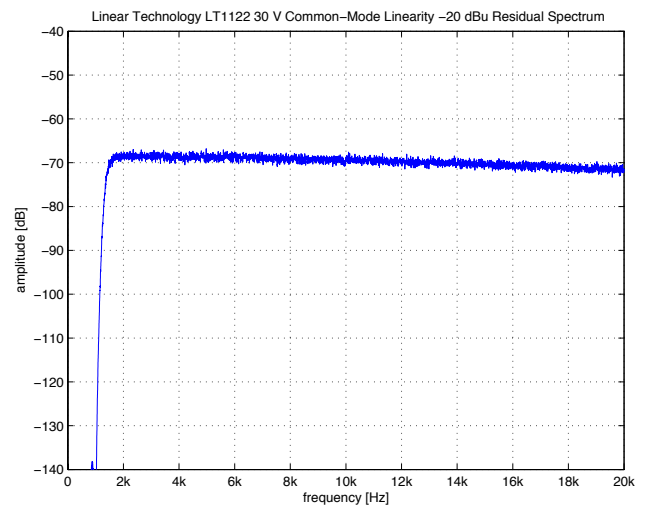
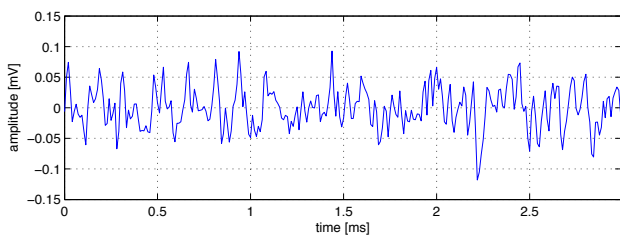
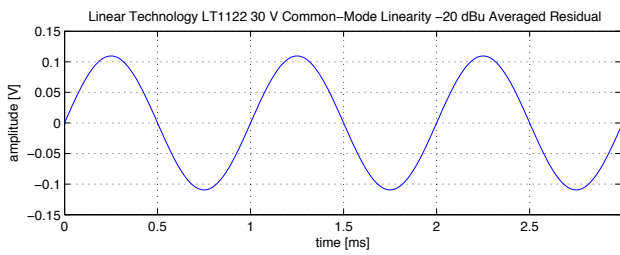
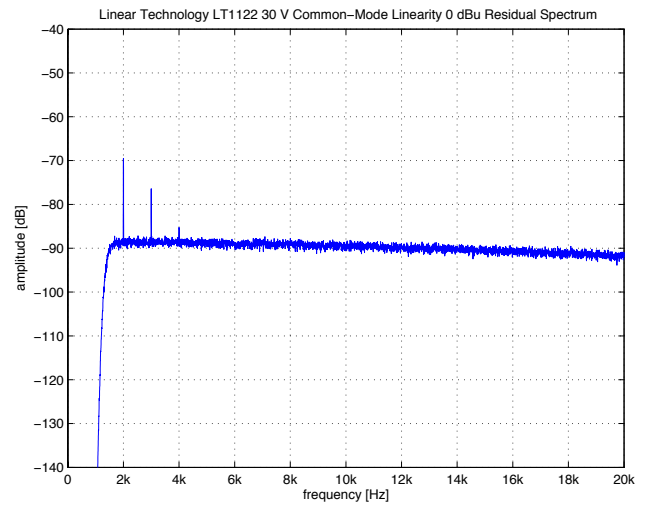
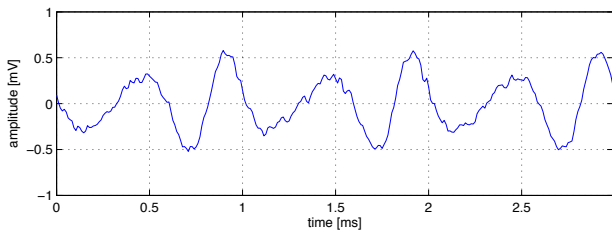
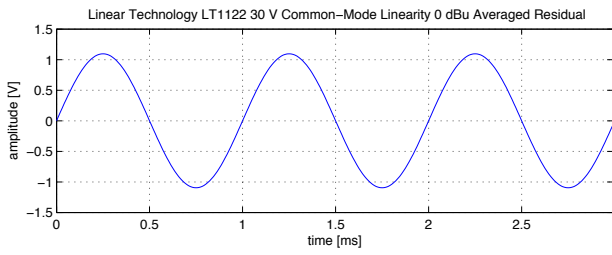
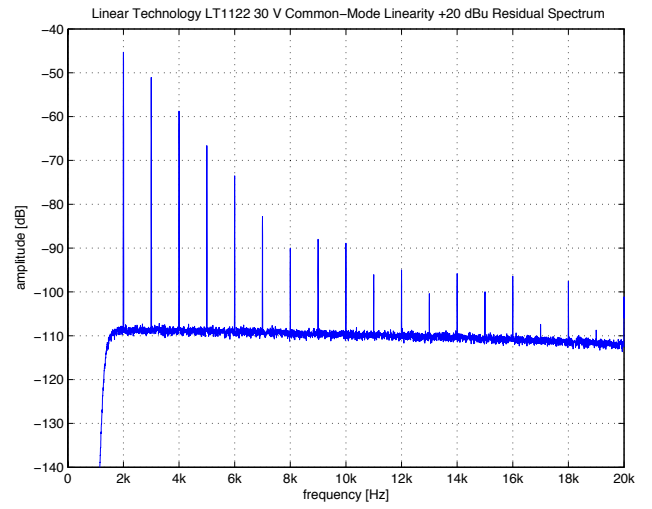
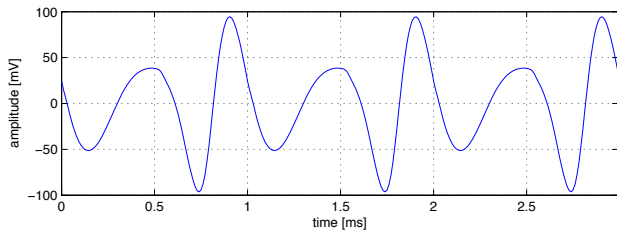
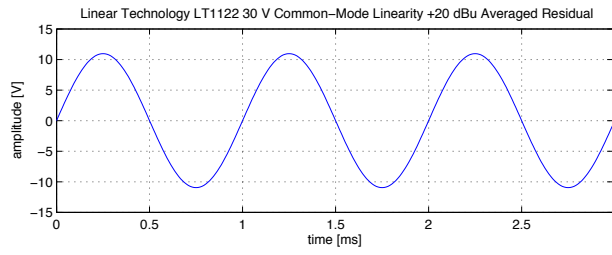
A JFET input opamp with very high slew-rate; the topology is not published according to the knowledge of the author. Voltage noise is rather high, presumably a result of a degenerated input stage.

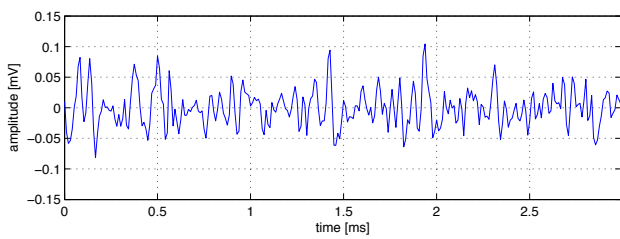
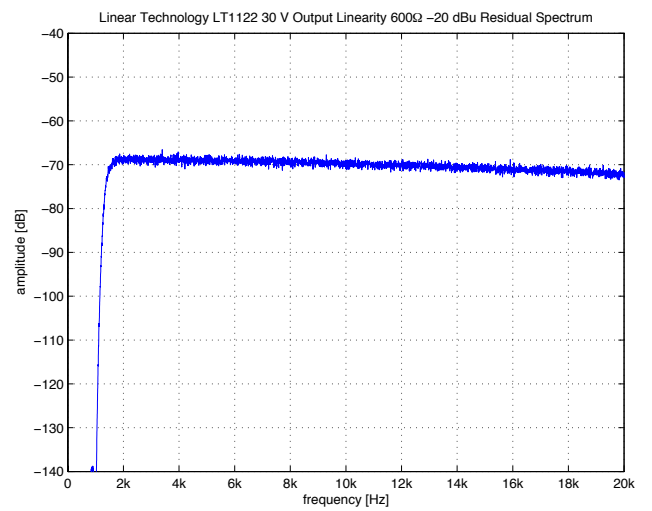
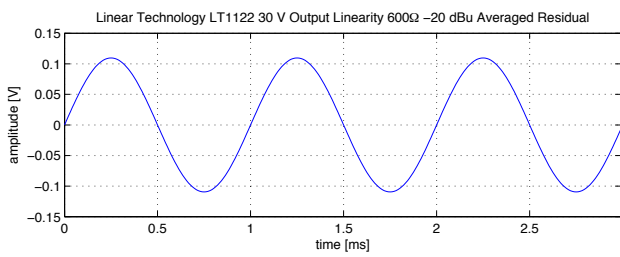
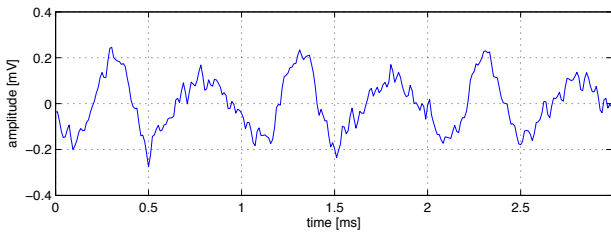
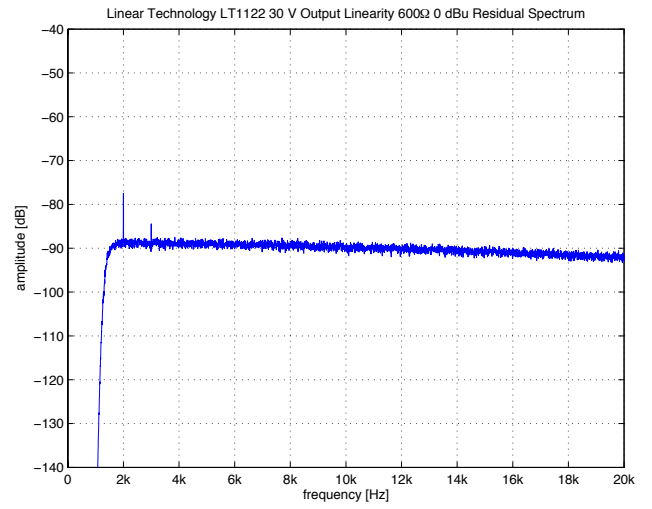
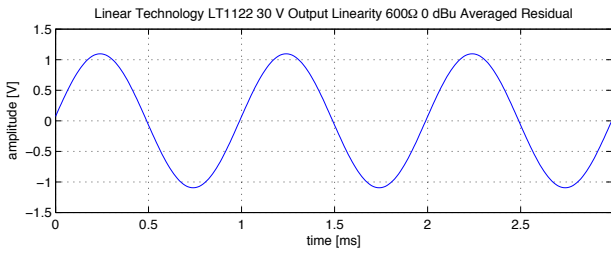
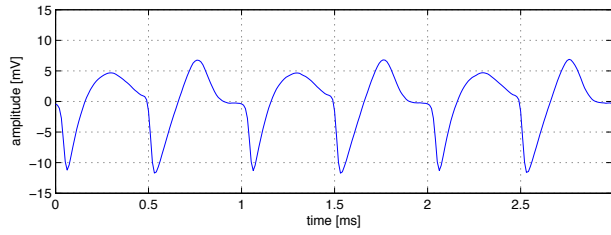
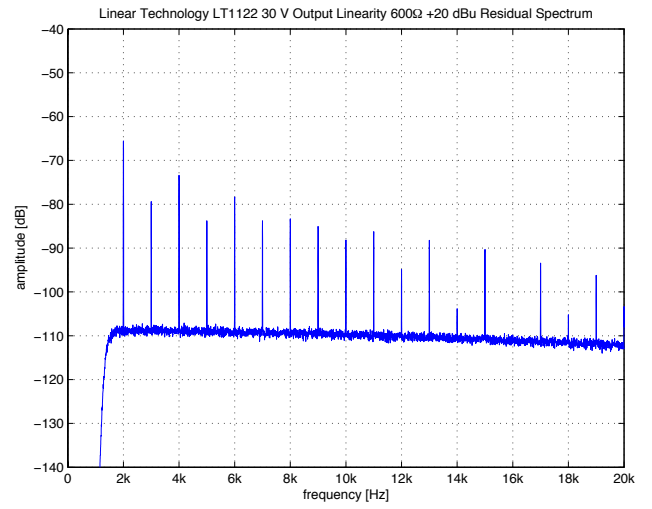
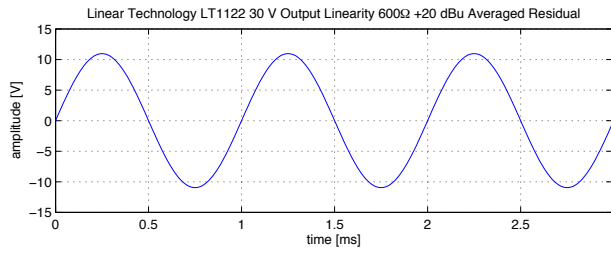
The basic transfer linearity is exceptionally good, up to high frequencies. Unfortunately the common-mode and input impedance linearity is very modest; output loading distortion is better controlled but still degrades the transfer linearity considerably. Note the thermal effects with  $600 \Omega$  load. Higher supply voltages reduce common-mode distortion, but highlight low-frequency distortion from output loading.

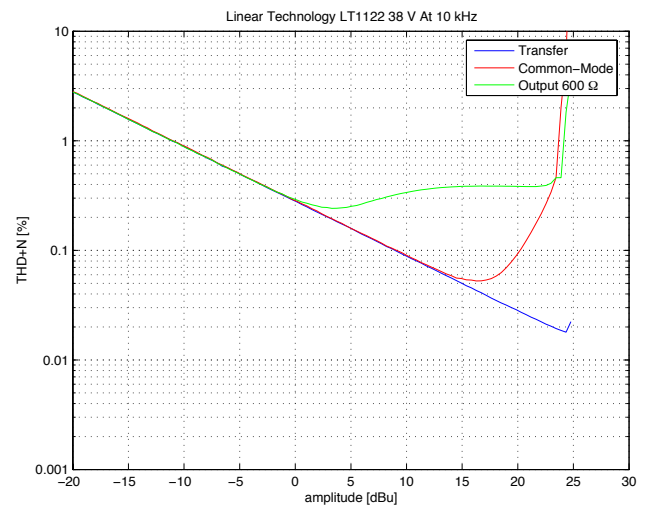
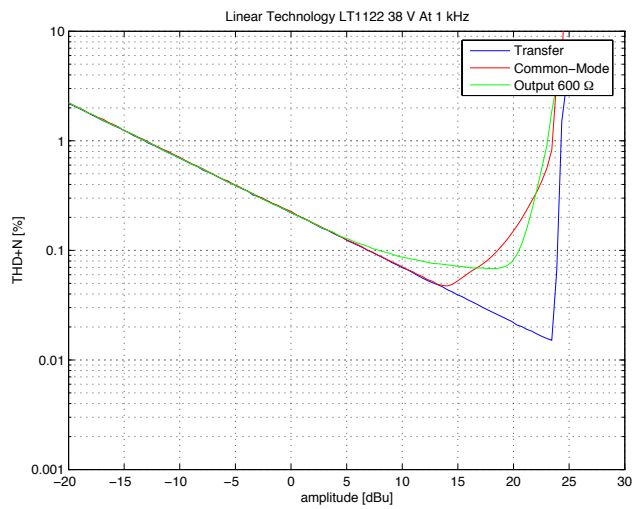
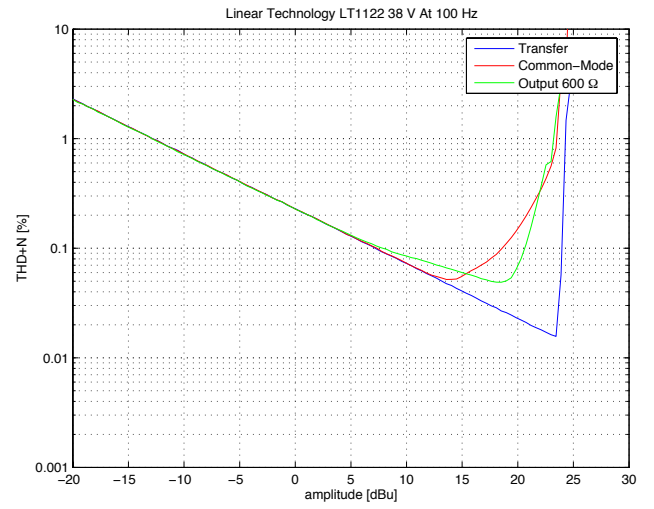
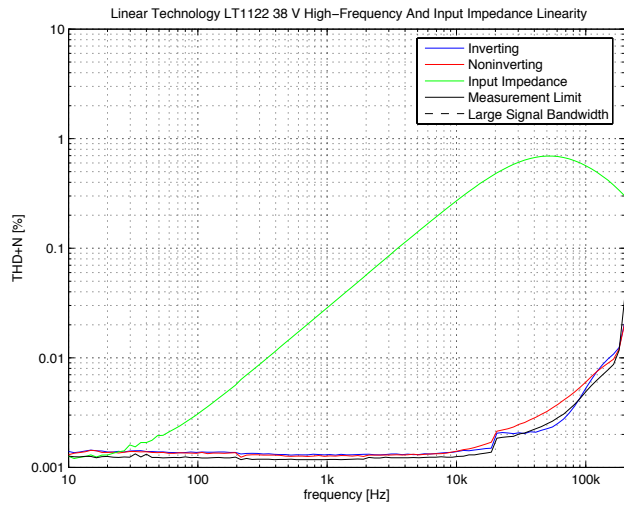
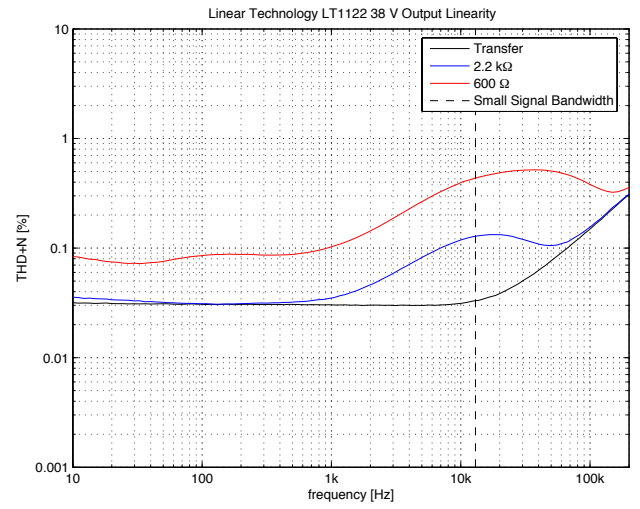
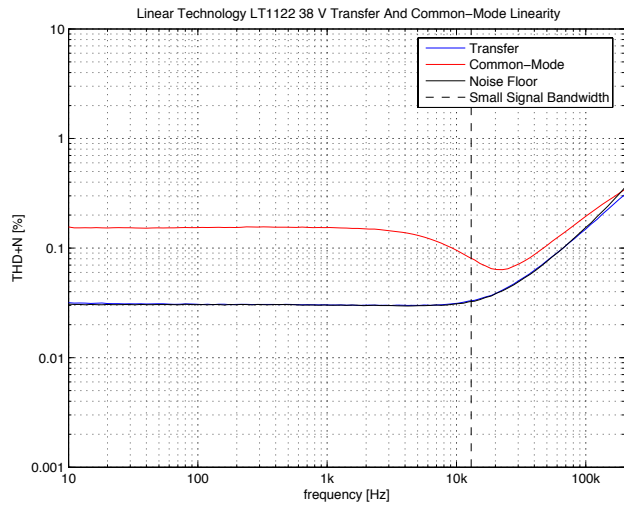
A good choice for applications where common-mode and output loading effects can be controlled, especially if linearity at high frequencies is a primary concern. Medium-high cost.

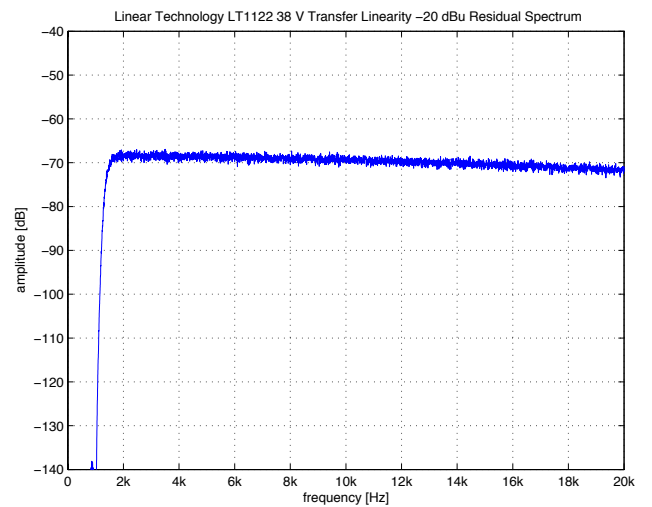
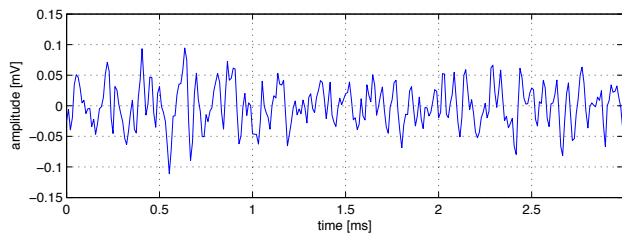
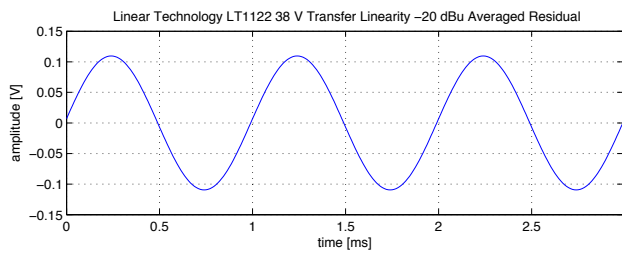
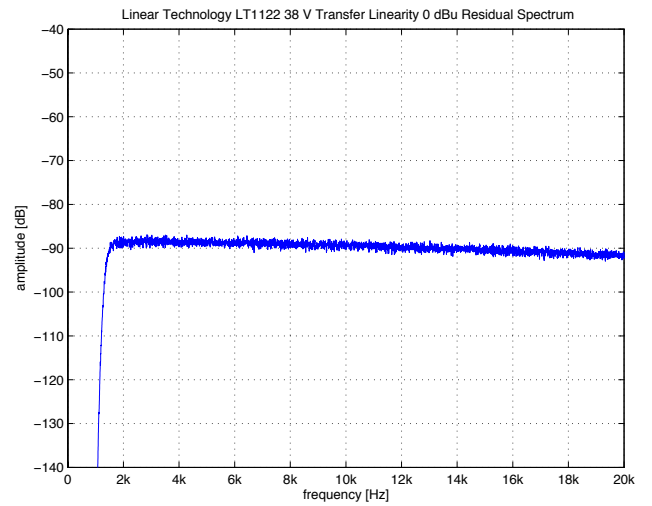
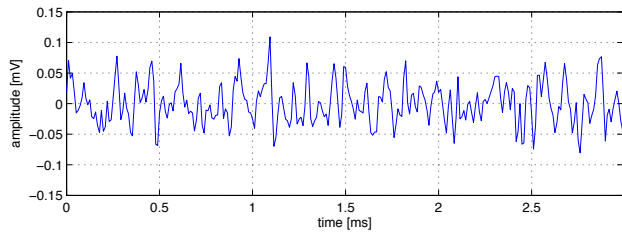
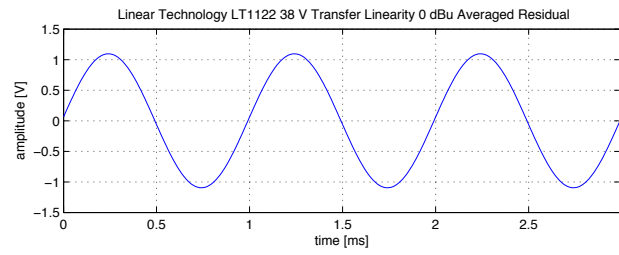
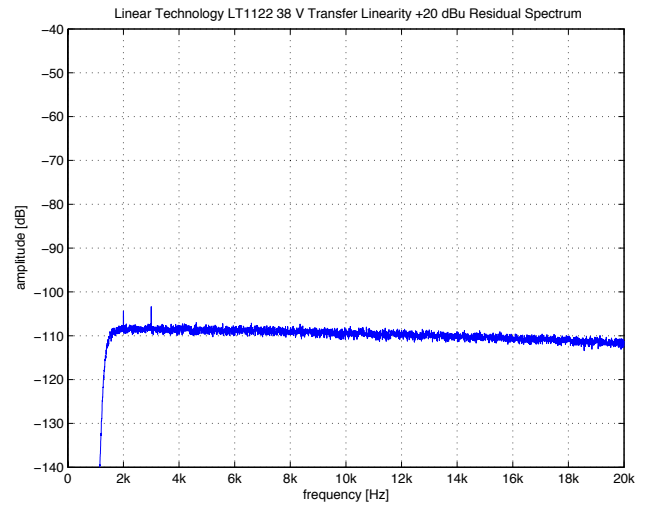
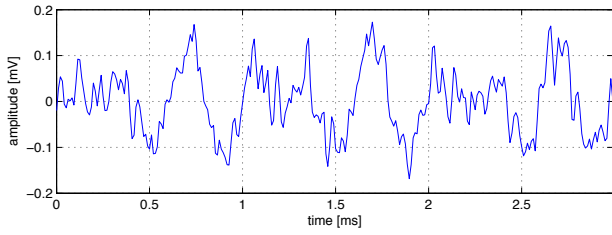
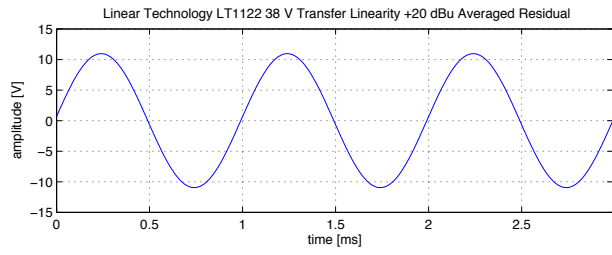


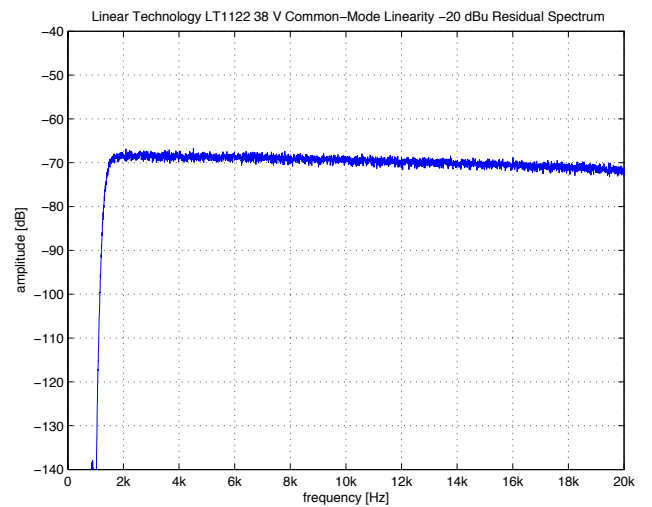
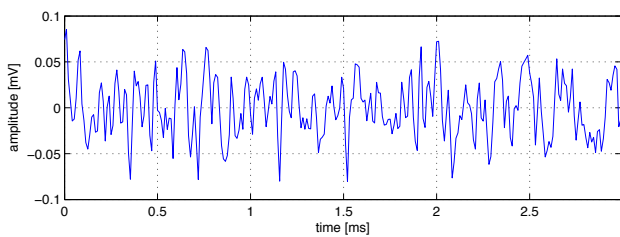
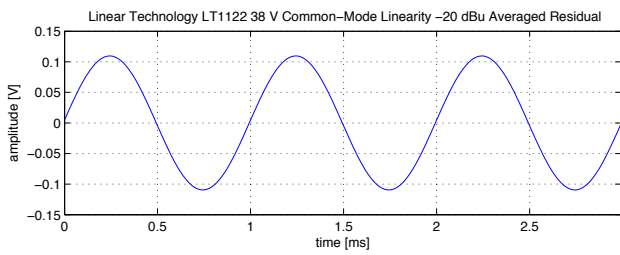
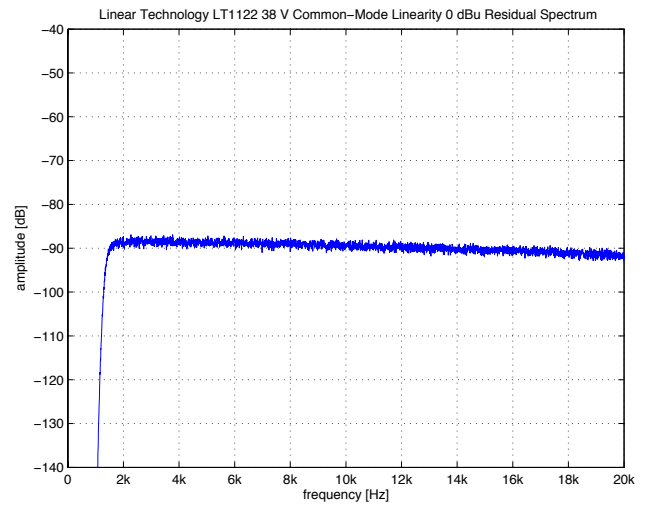
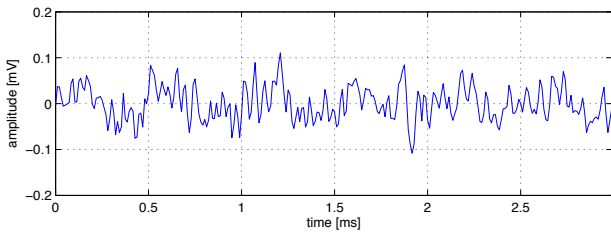
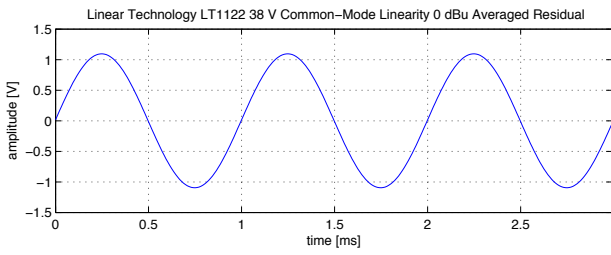
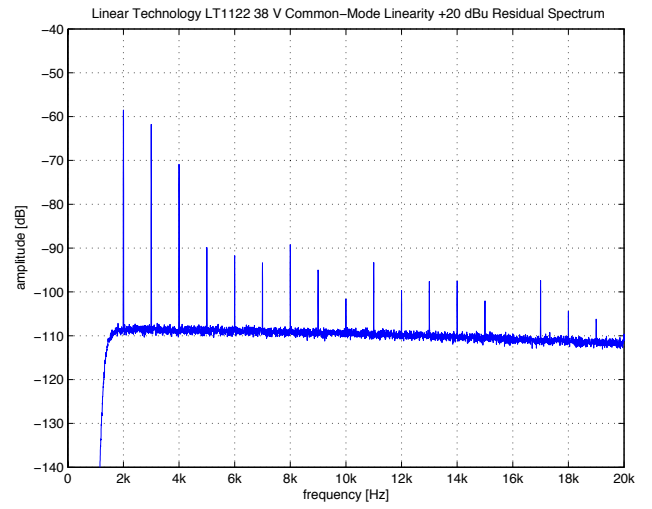
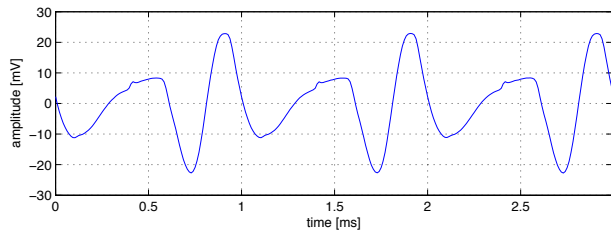
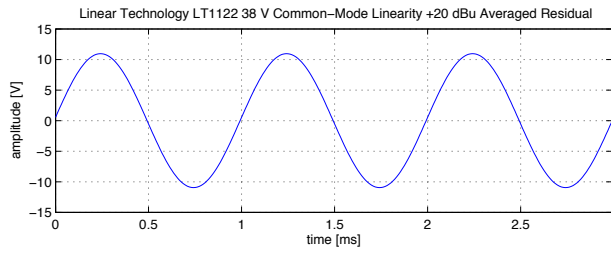




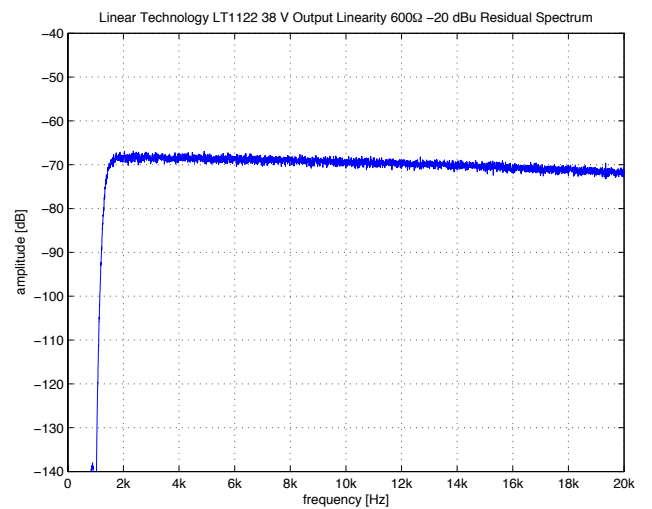
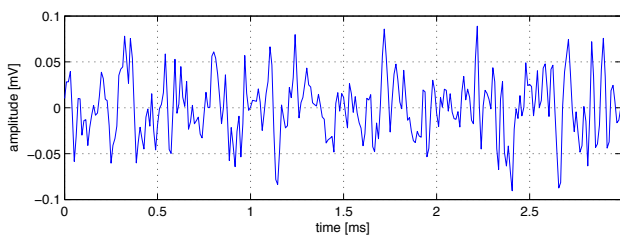
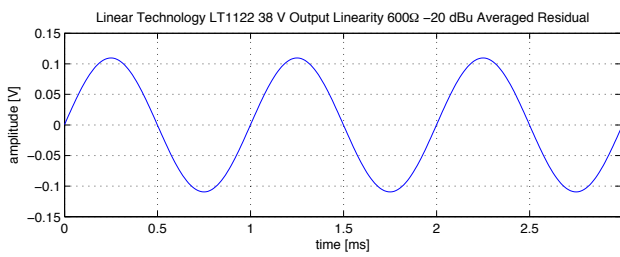
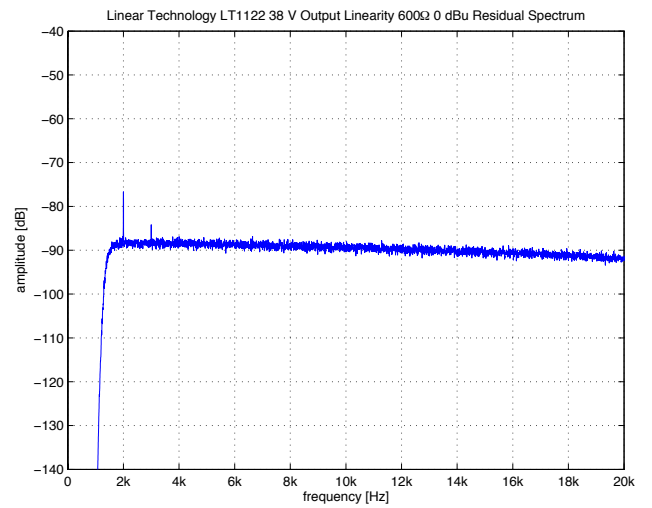
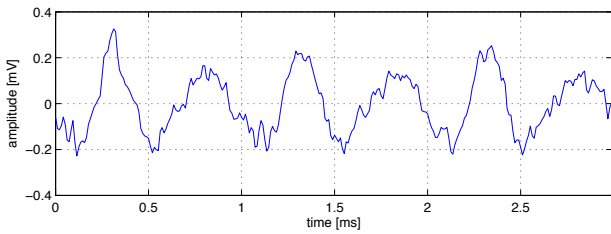
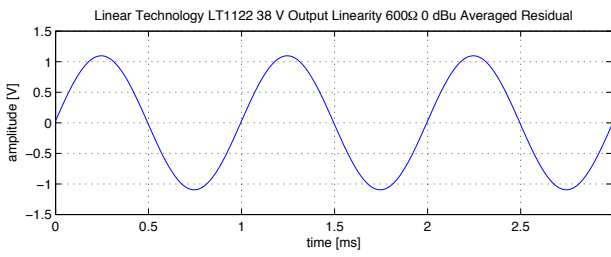
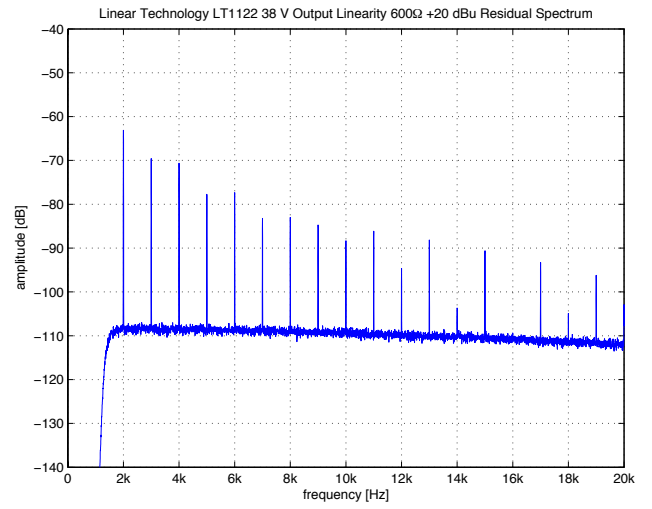
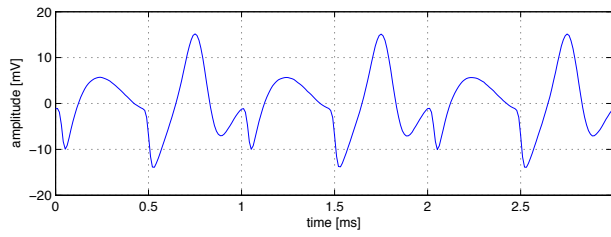
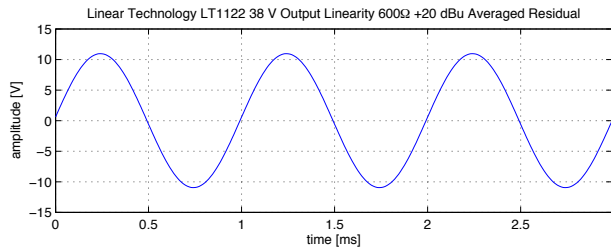












### 3.9 Linear Technology LT1128

<b>Number of Channels</b>	1
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	4.75 US\$ at 1k units (July 2008)

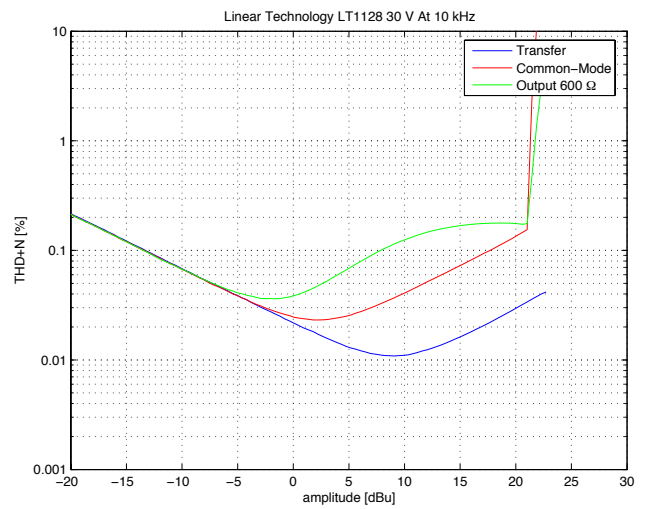
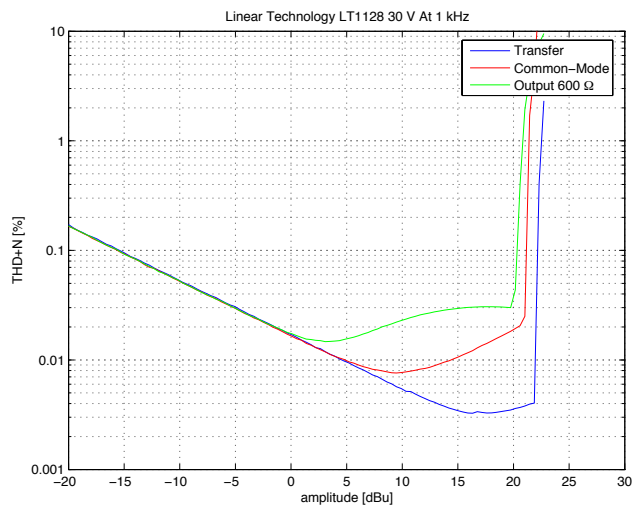
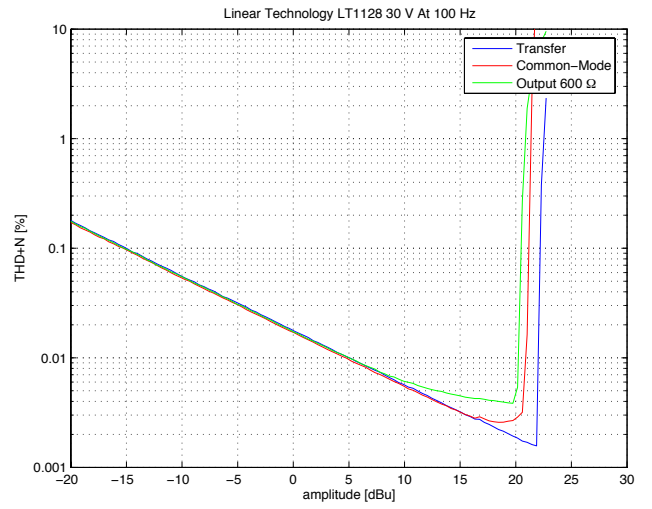
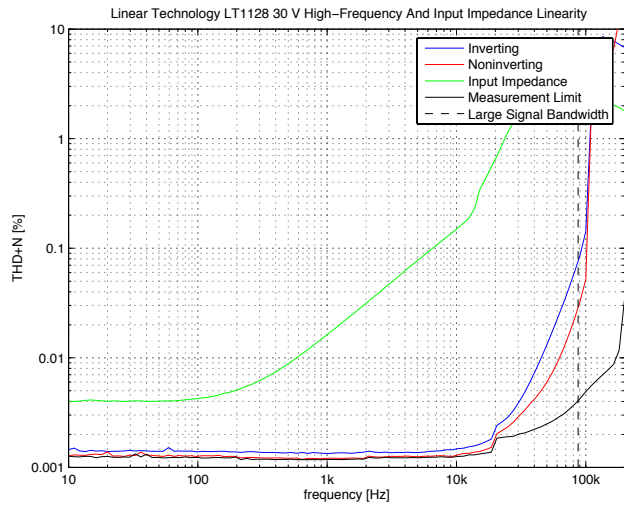
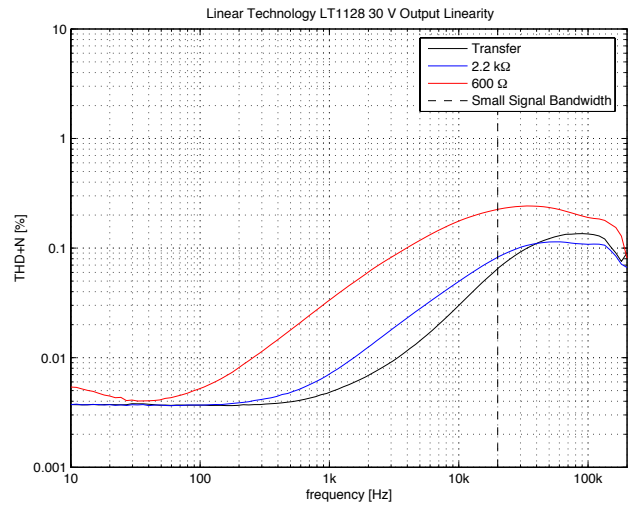
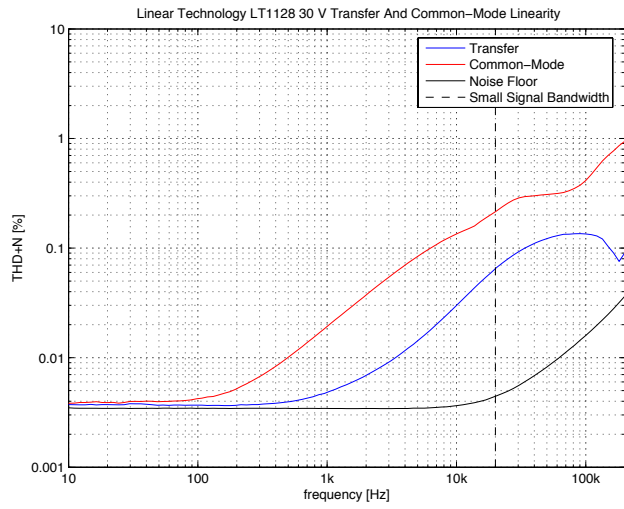
Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		20	80	$\mu\text{V}$
Input Bias Current		30	80	nA
Input Offset Current		18	100	nA
Gain Bandwidth Product	11	20		MHz
Slew-Rate	4.5	6		$\text{V}/\mu\text{S}$
Input Voltage Noise ( $f = 1 \text{ kHz}$ )		0.9	1.2	$\text{nV}/\sqrt{\text{Hz}}$
Input Current Noise ( $f = 1 \text{ kHz}$ )		1	1.8	$\text{pA}/\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 11$	$\pm 12.2$		V
Output Voltage Swing ( $R_L = 2 \text{ k}\Omega$ )	$\pm 12$	$\pm 13$		V
Output Voltage Swing ( $R_L = 600 \Omega$ )	$\pm 10.5$	$\pm 12.2$		V
Output Current	$\pm 15$	$\pm 22$		mA
Power Supply Voltage	$\pm 2.5$		$\pm 22$	V
Quiescent Current per Amplifier		7.6	10.5	mA

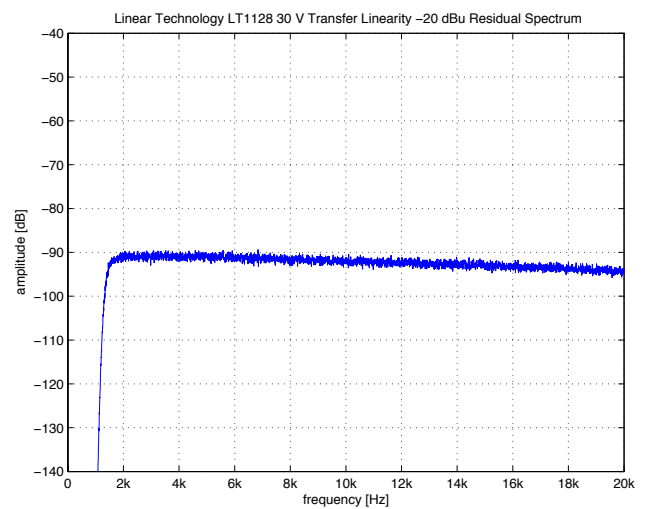
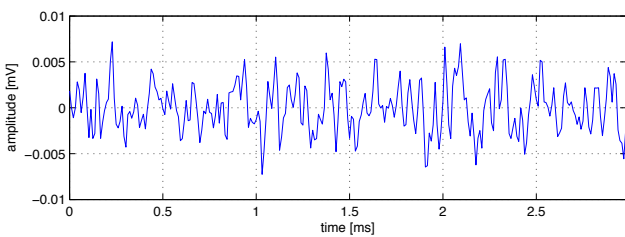
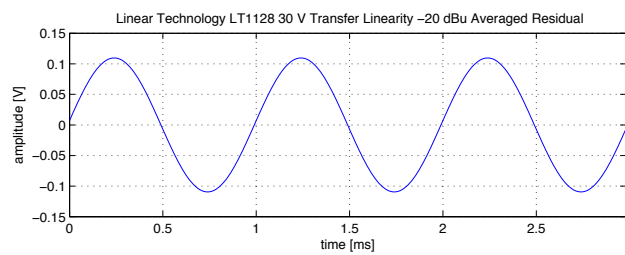
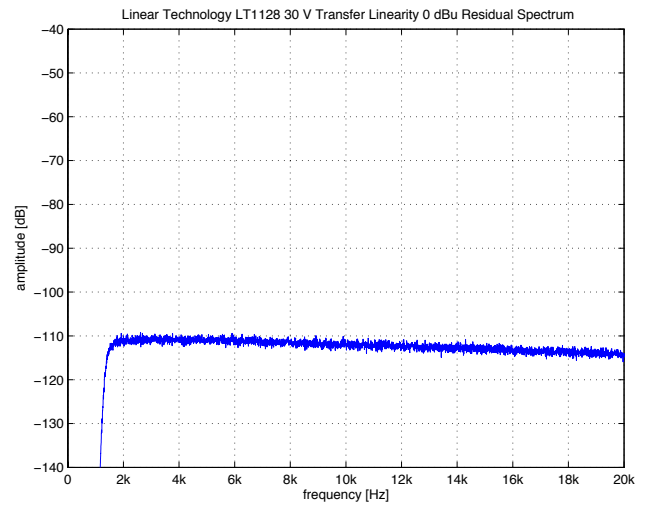
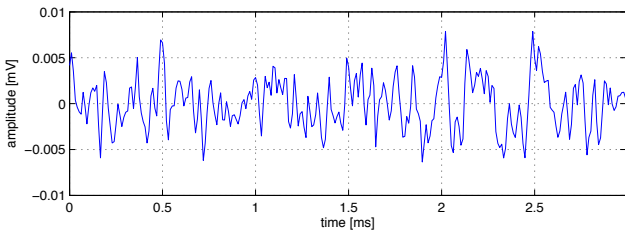
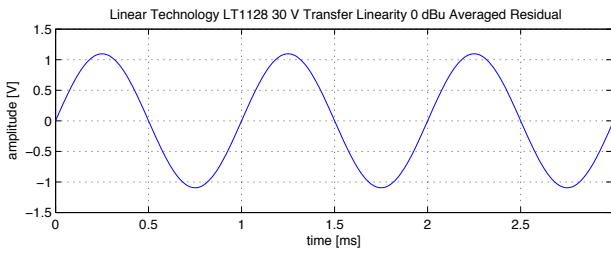
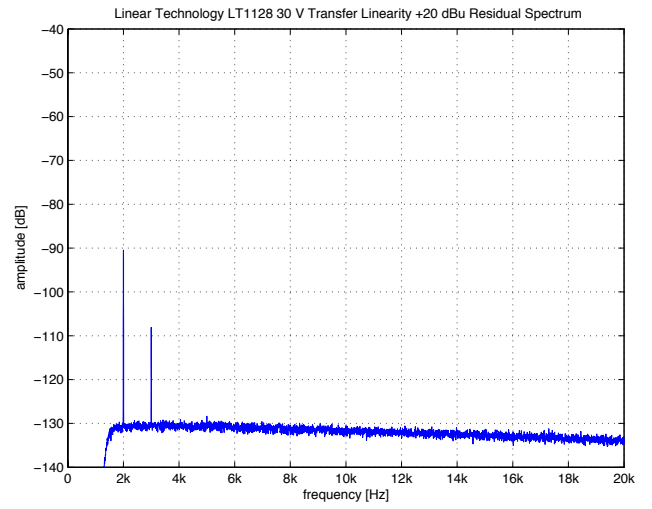
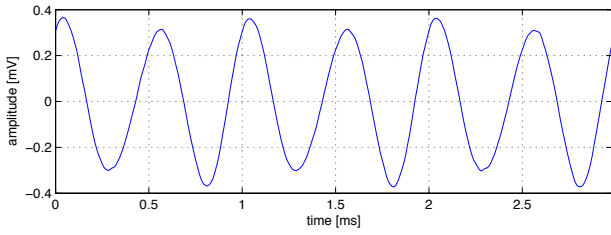
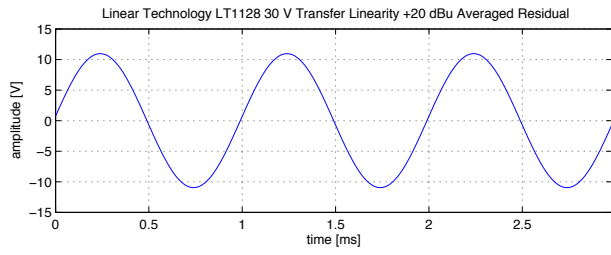
Table 3.9: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 15 \text{ V}$ .

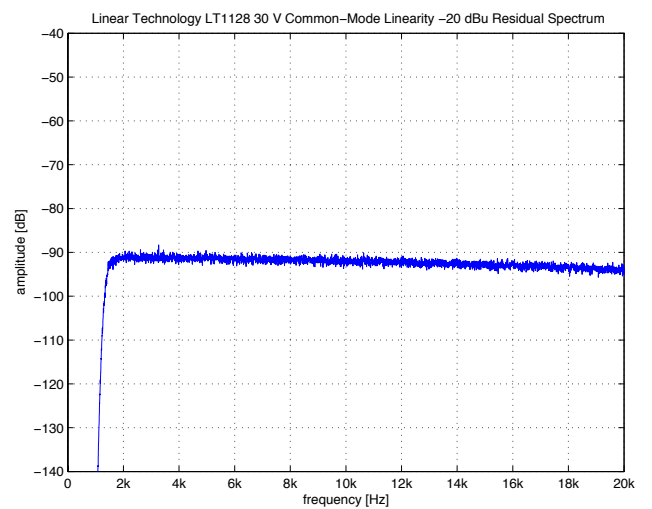
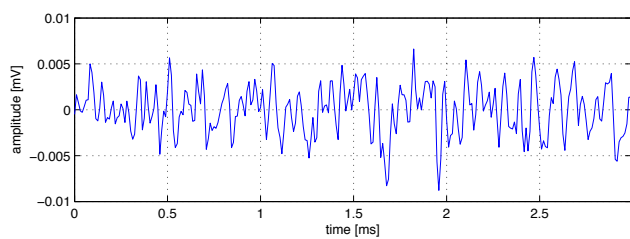
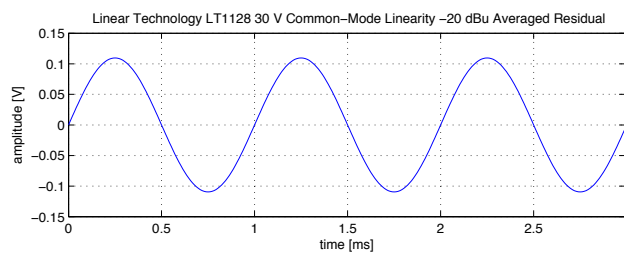
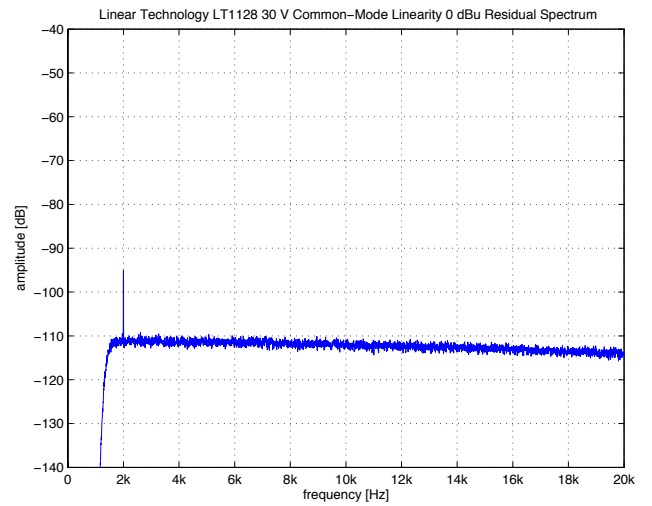
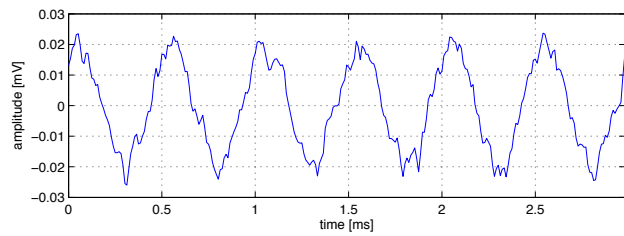
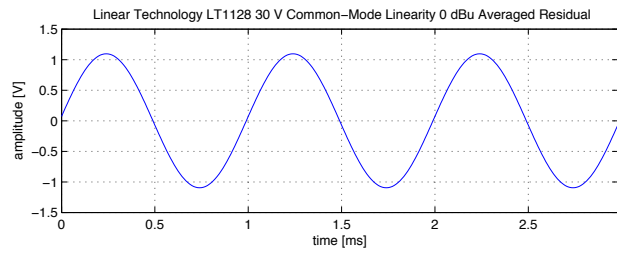
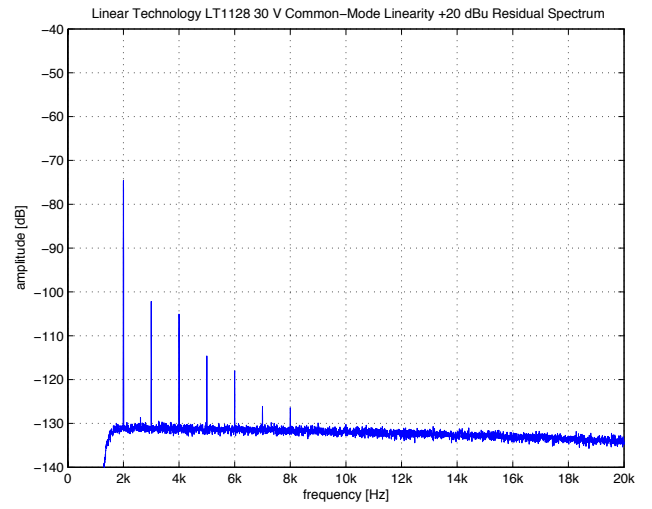
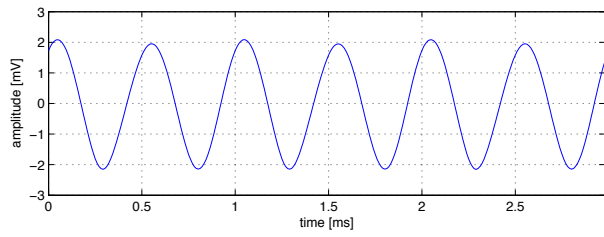
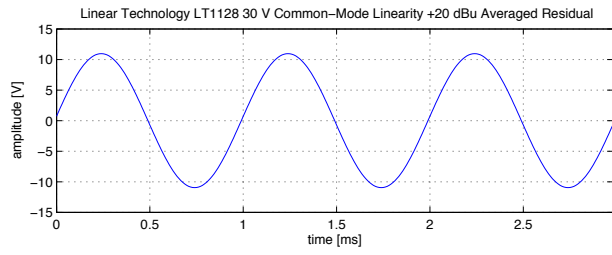
An operational amplifier with a bipolar input stage and a three-stage architecture. Note very low voltage noise combined with reasonably low current noise and pretty low input bias currents. A decompensated version stable at noise gains of two (LT1028) is available.

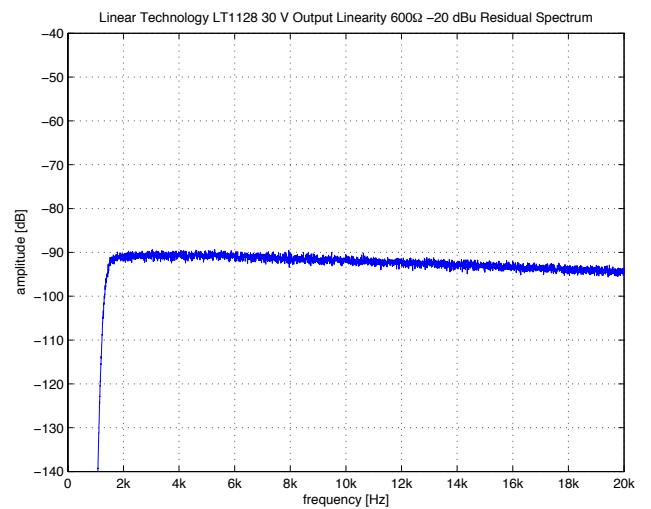
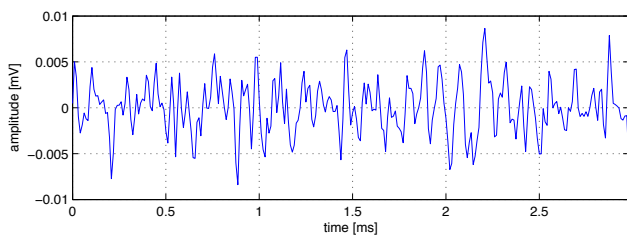
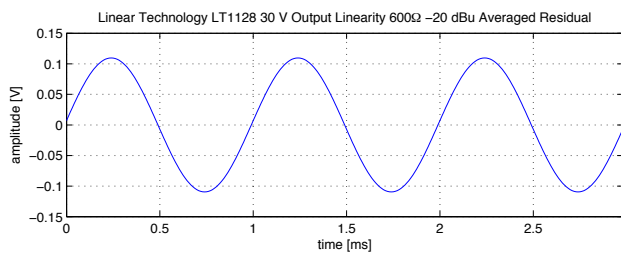
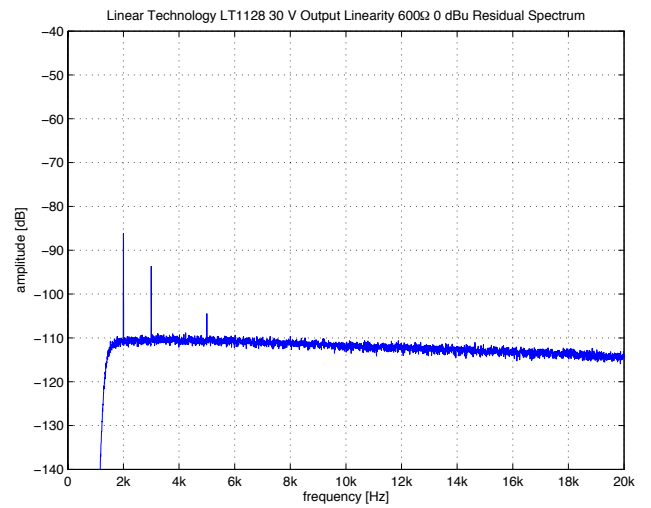
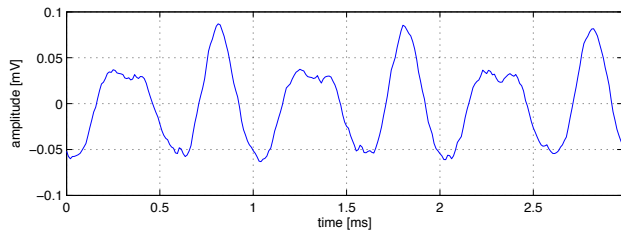
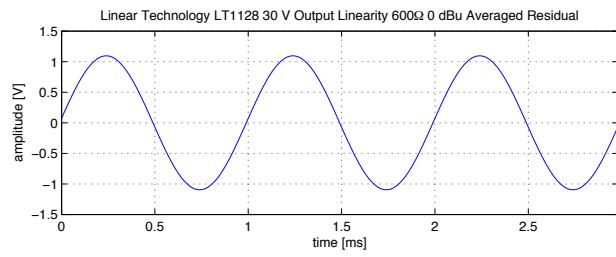
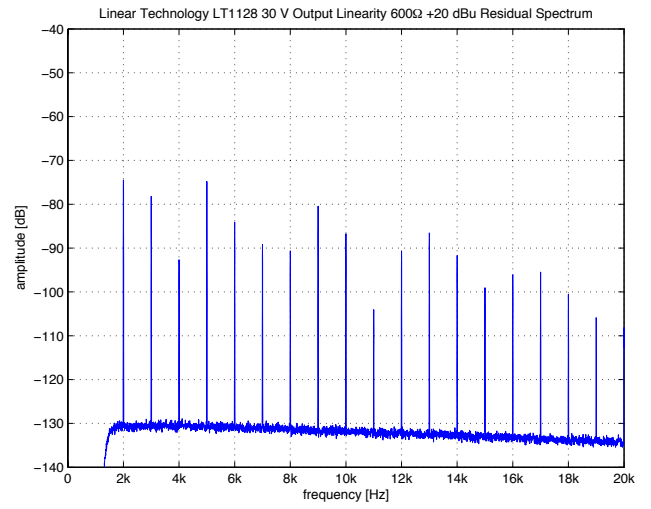
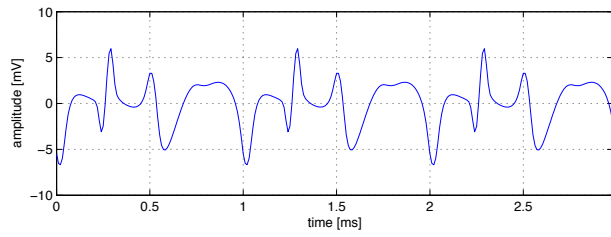
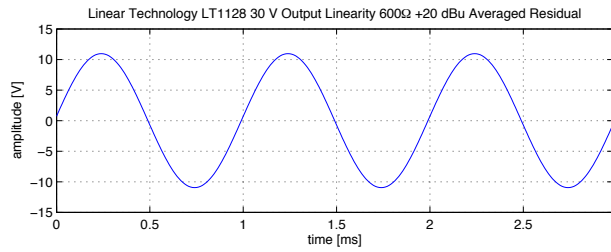
At low frequencies the transfer and common-mode linearity is very good; unfortunately the performance degrades relatively fast towards higher frequencies. Input impedance shows severe nonlinearity with an unusually rapid increase above 10 kHz. With a 600  $\Omega$  load distortion is severely increased, and thermal effects become measurable. Higher supply voltages do not help performance significantly.

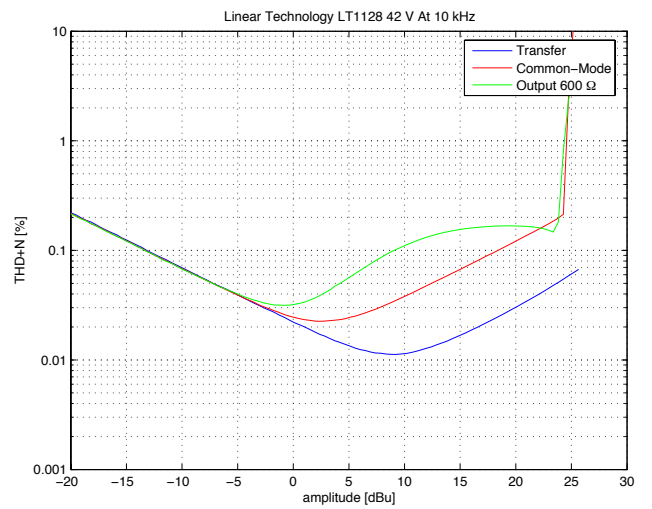
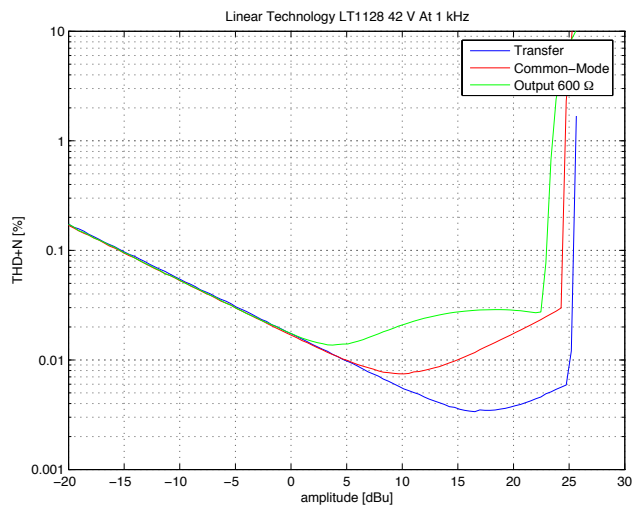
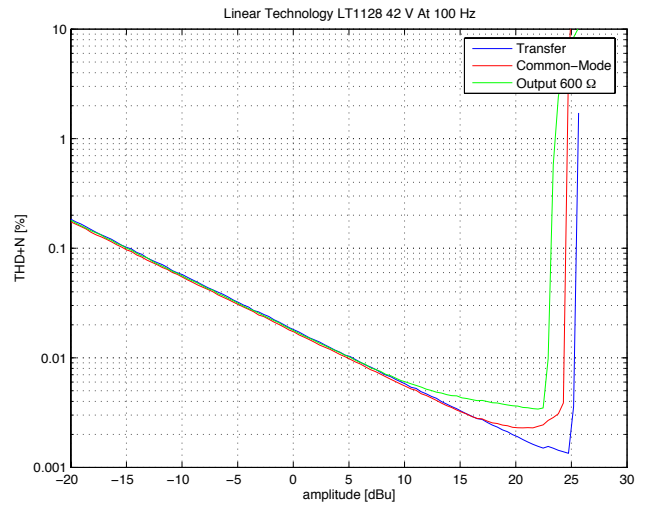
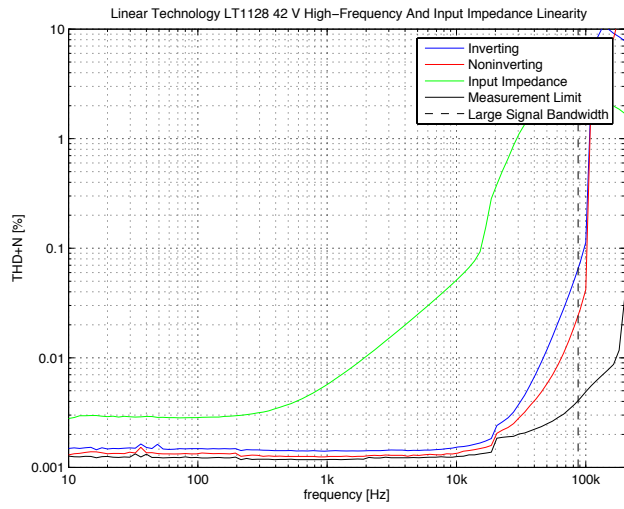
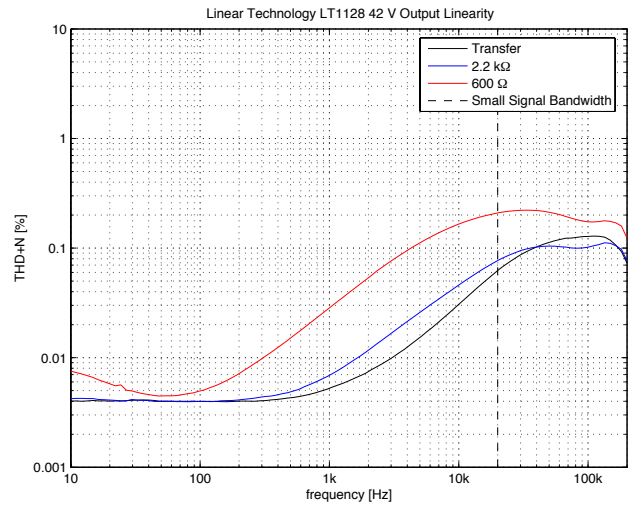
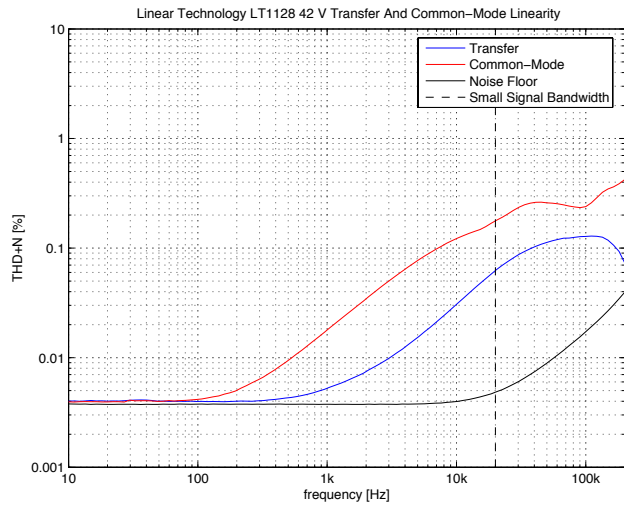
Only a medium performer with respect to distortion unless lower frequencies are of main interest—and expensive.

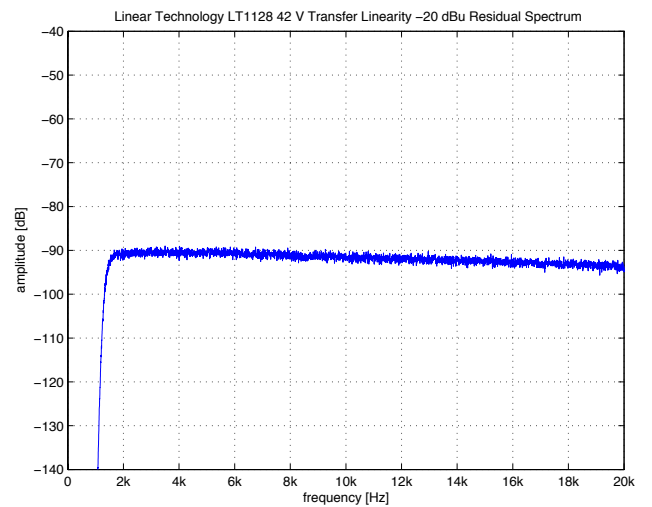
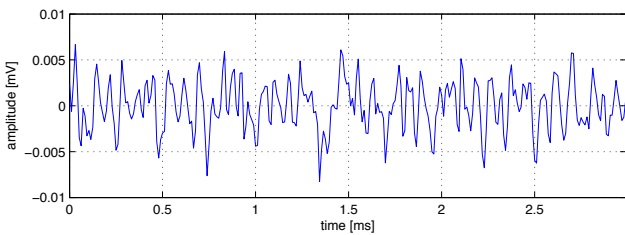
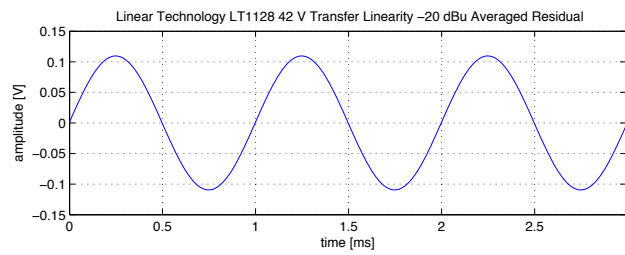
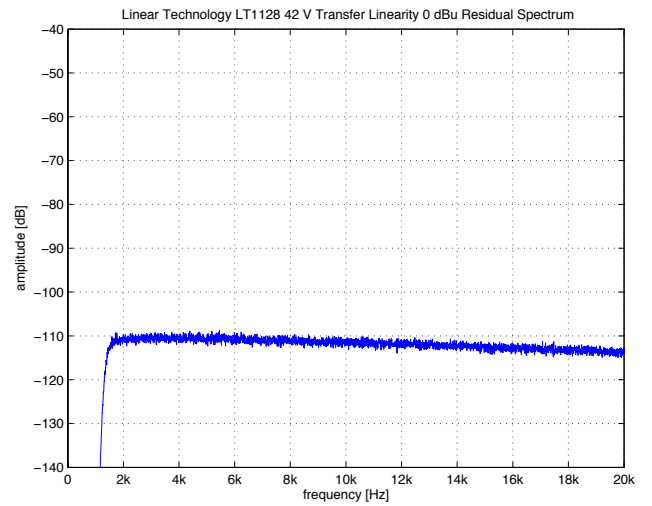
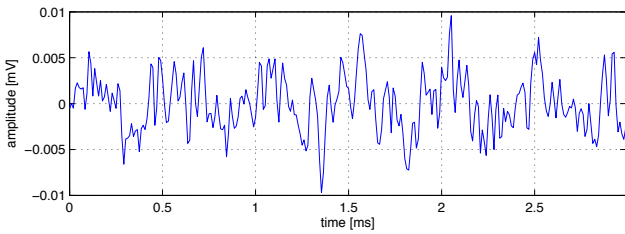
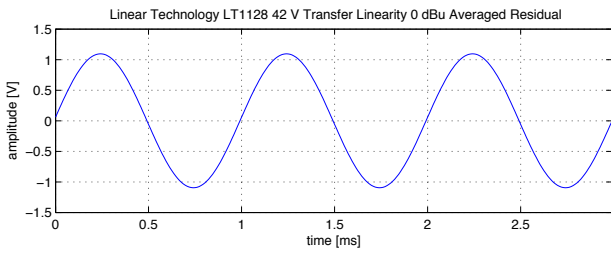
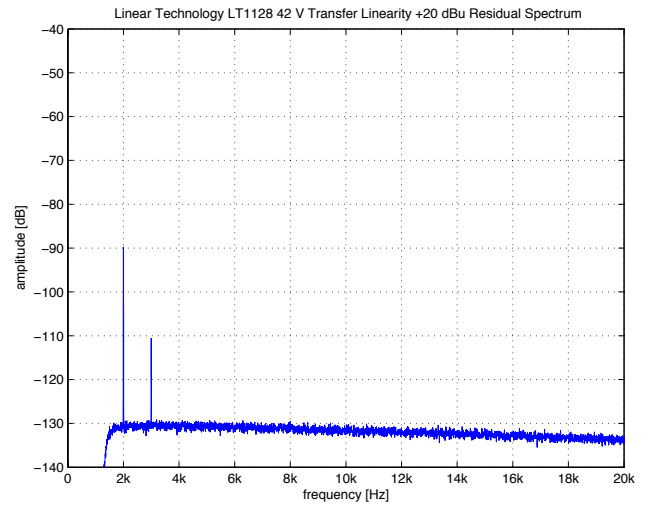
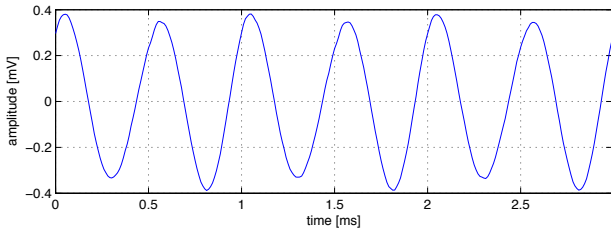
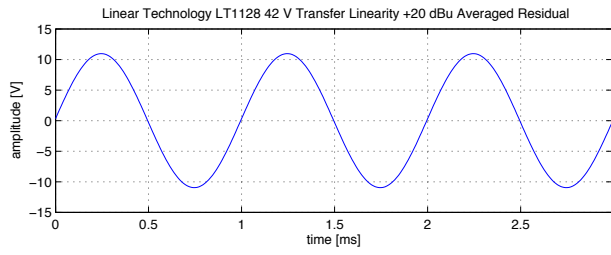




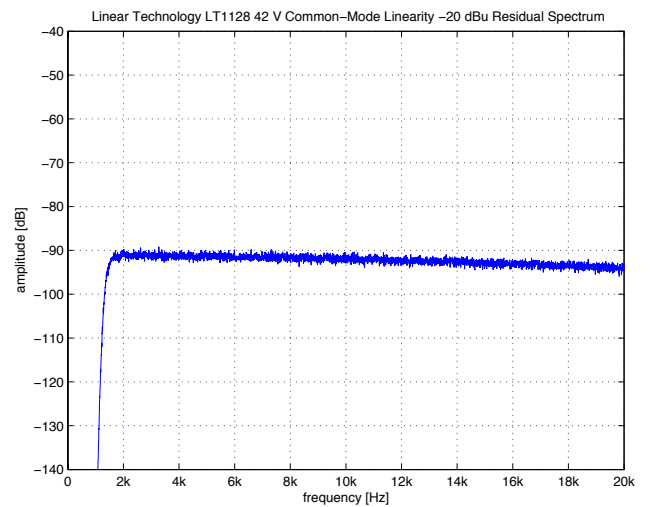
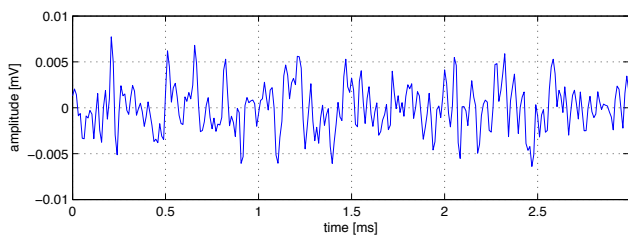
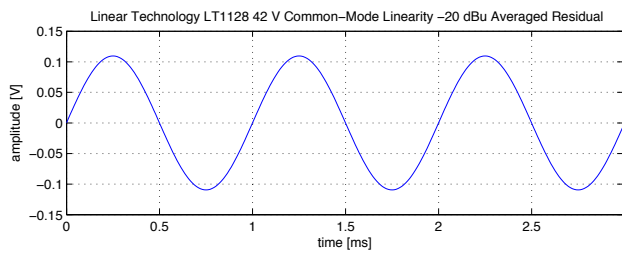
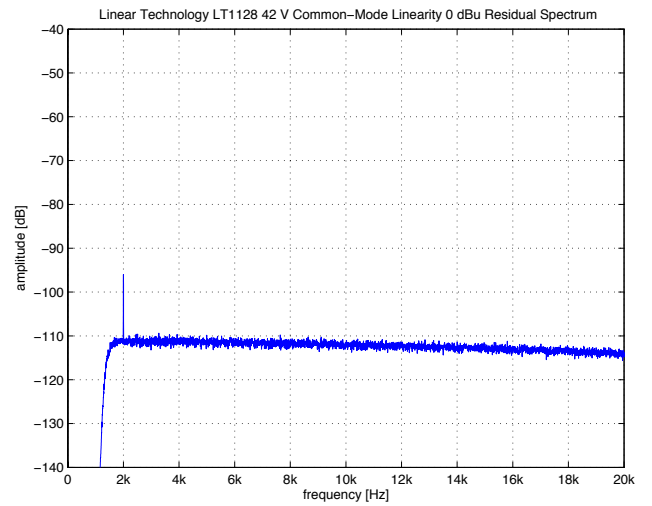
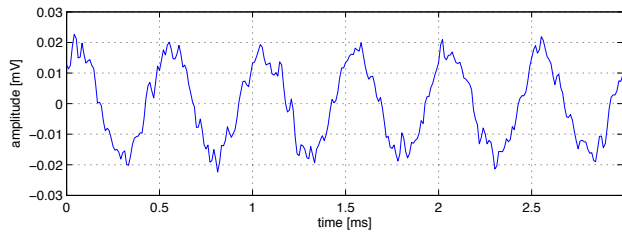
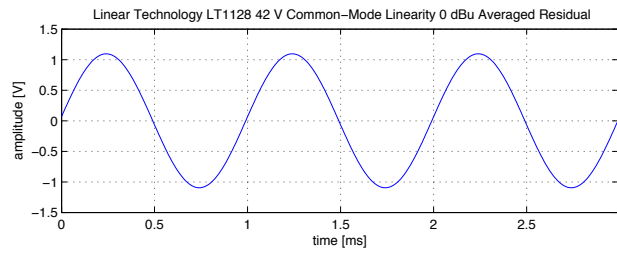
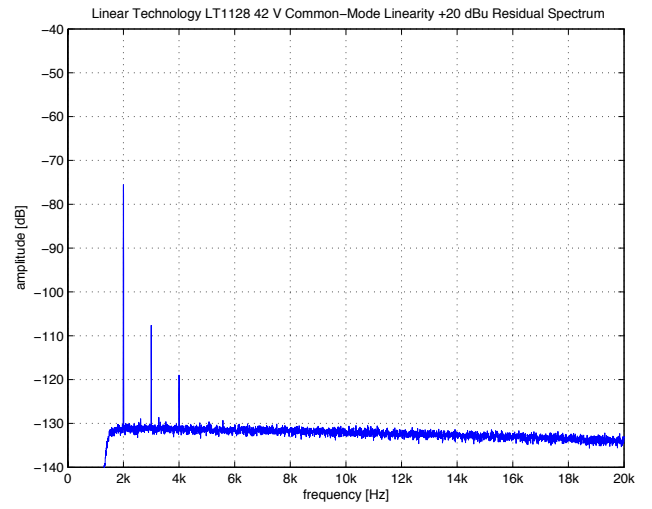
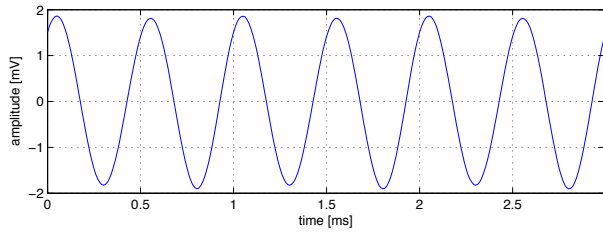
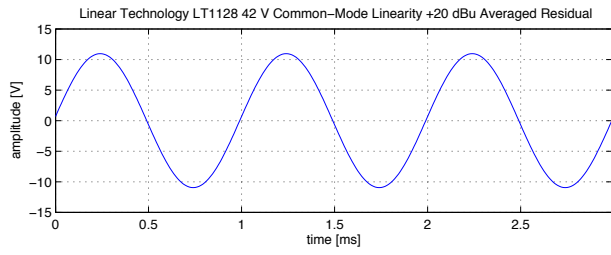


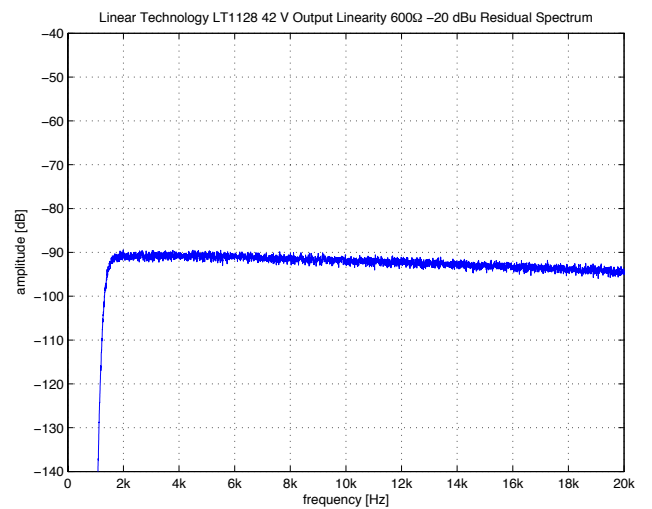
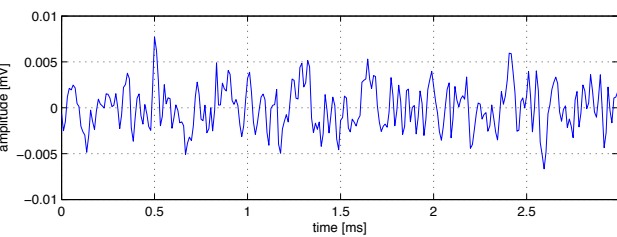
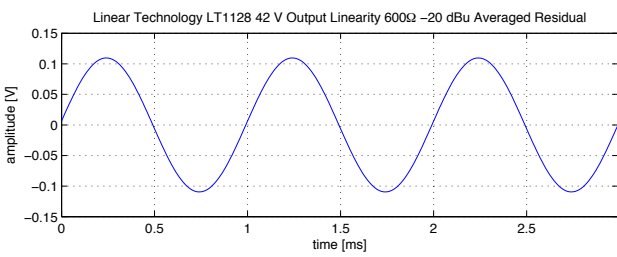
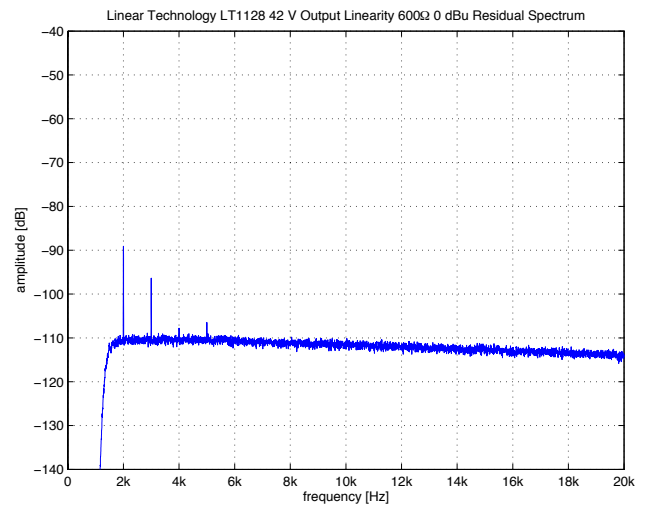
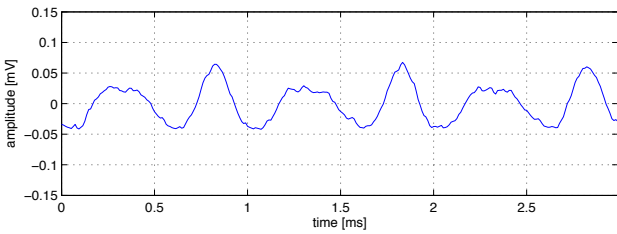
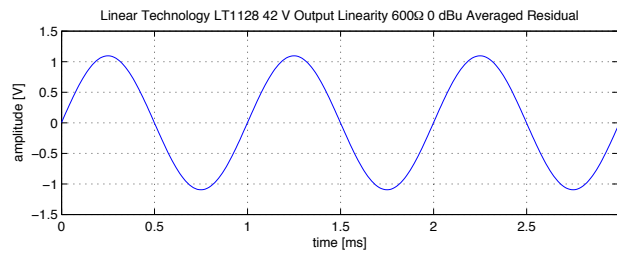
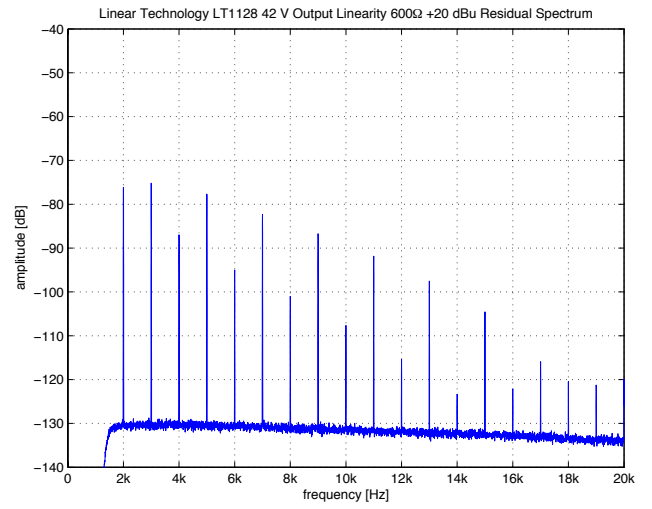
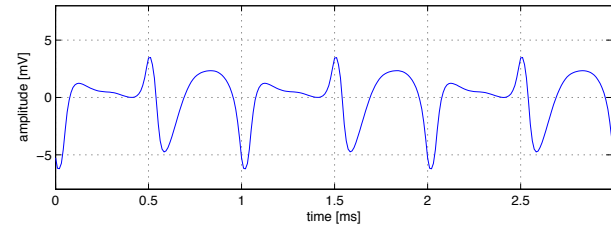
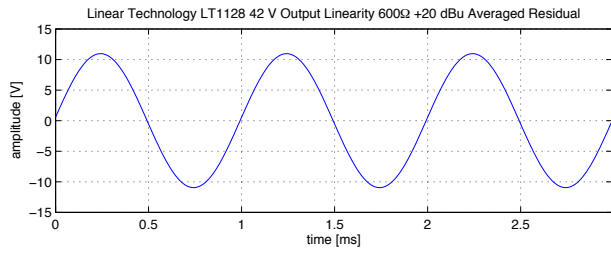












### 3.10 Linear Technology LT1213

<b>Number of Channels</b>	2
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	1.43 US\$ at 1k units (July 2008)

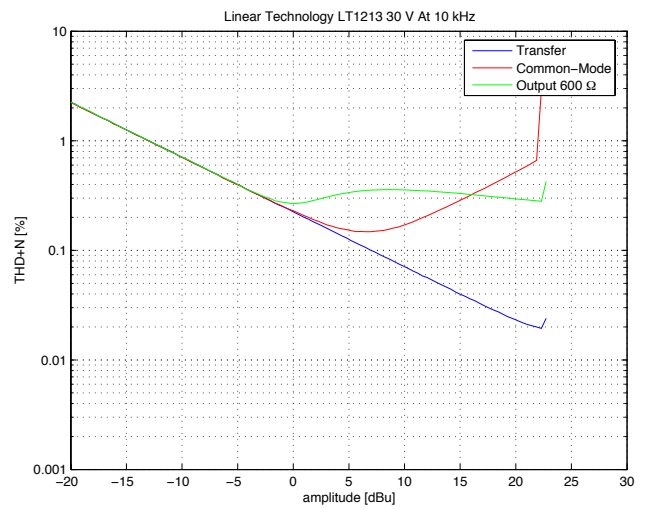
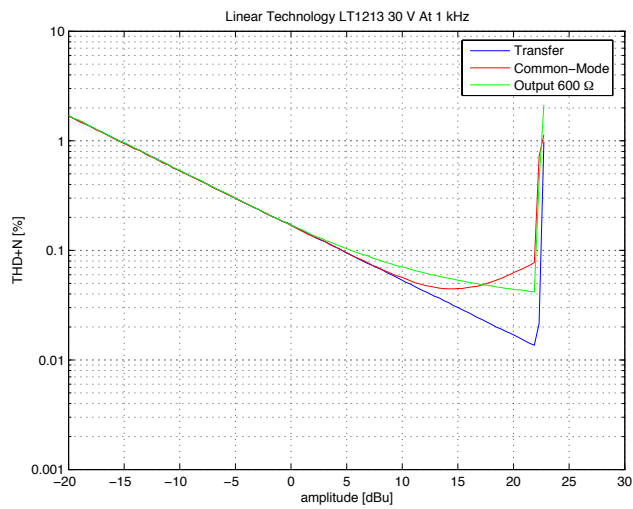
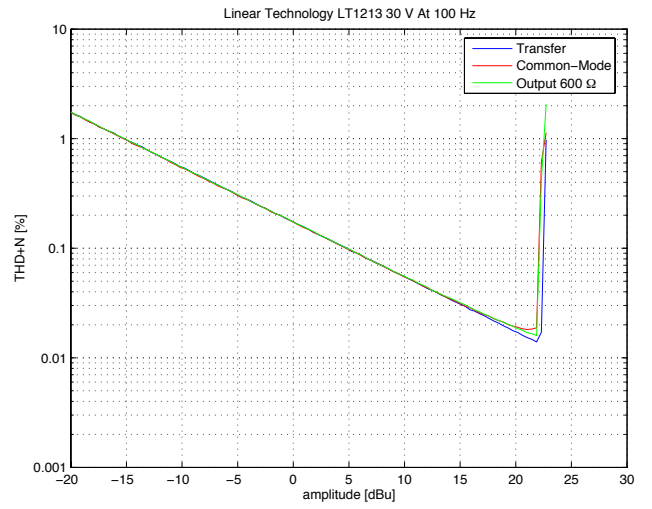
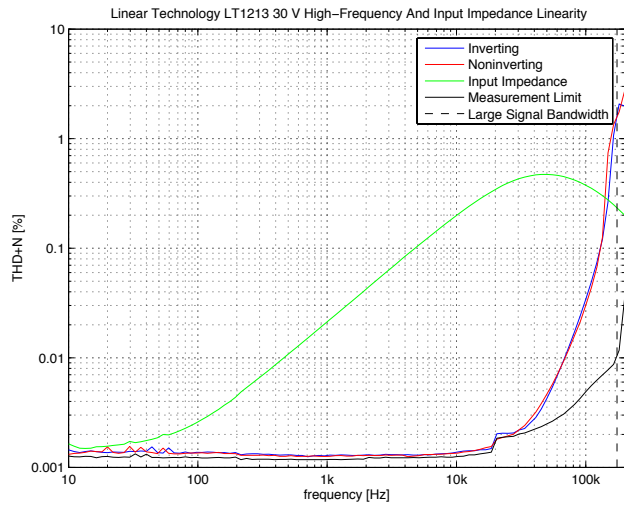
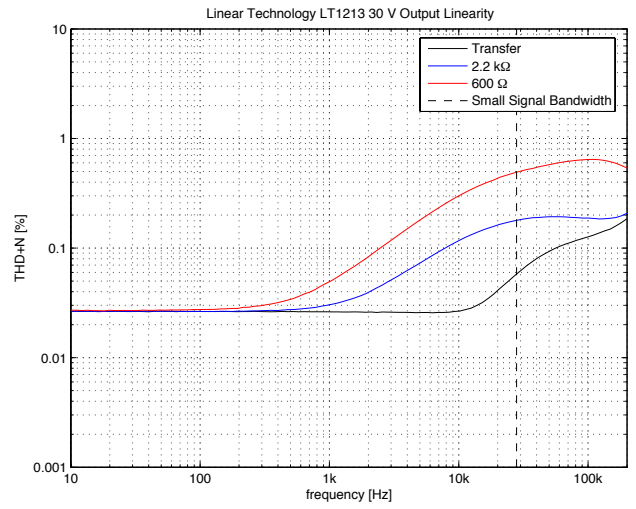
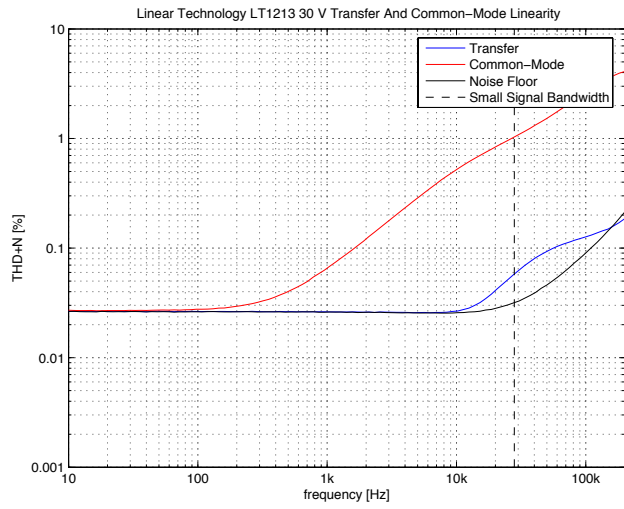
Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		150	550	$\mu\text{V}$
Input Bias Current		90	190	nA
Input Offset Current		5	40	nA
Gain Bandwidth Product	15	28		MHz
Slew-Rate	10	12		$\text{V}/\mu\text{S}$
Input Voltage Noise (f = 1 kHz)		10		$\text{nV}/\sqrt{\text{Hz}}$
Input Current Noise (f = 1 kHz)		0.2		$\text{pA}/\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	+13.5/−15	+13.8/−15.3		V
Output Voltage Swing ( $I_{\text{OUT}} = 20 \text{ mA}$ )	+13.7/−14.3	+13.9/−14.5		V
Output Current	$\pm 30$	$\pm 50$		mA
Power Supply Voltage	$\pm 2$		$\pm 18$	V
Quiescent Current per Amplifier	2	3.4	3.7	mA

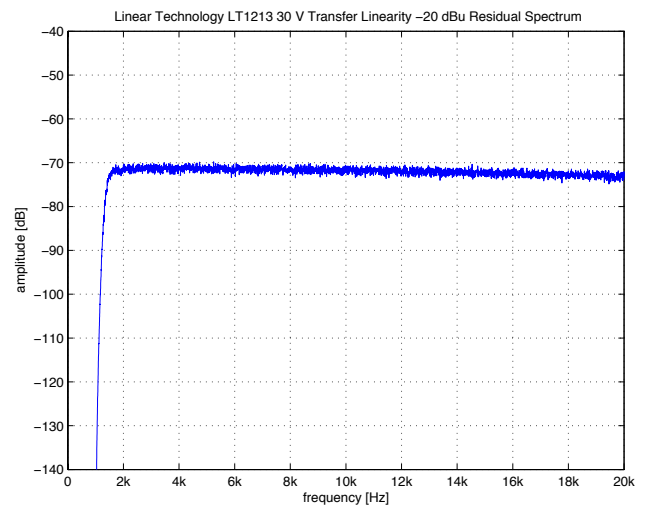
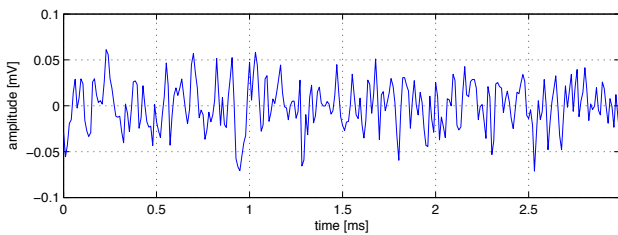
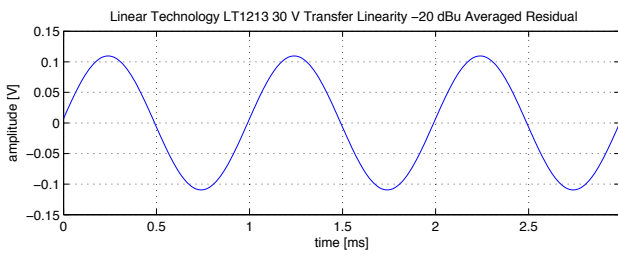
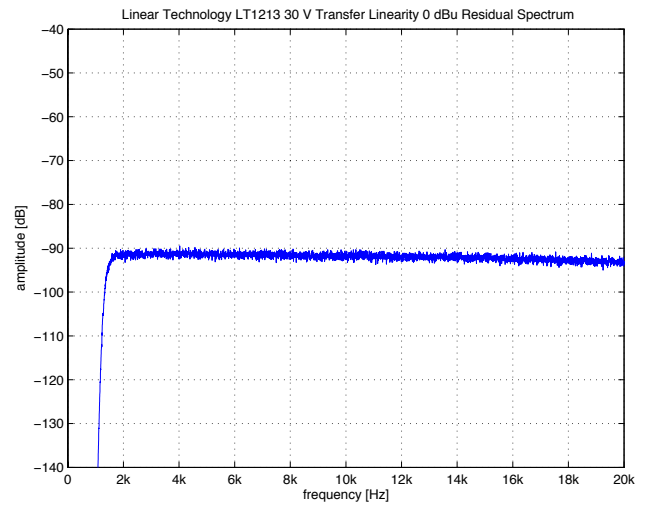
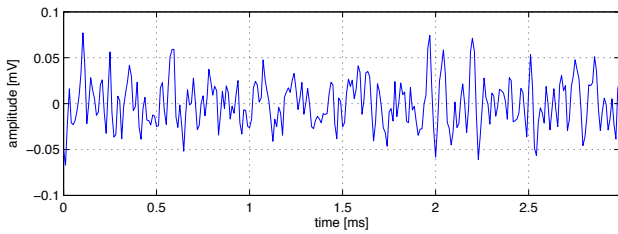
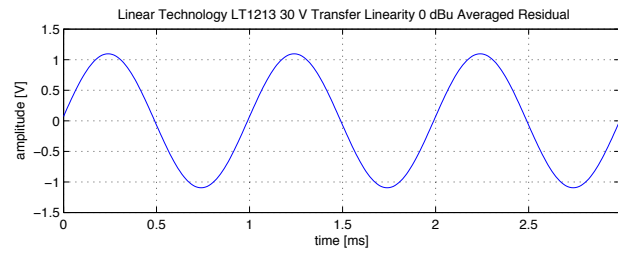
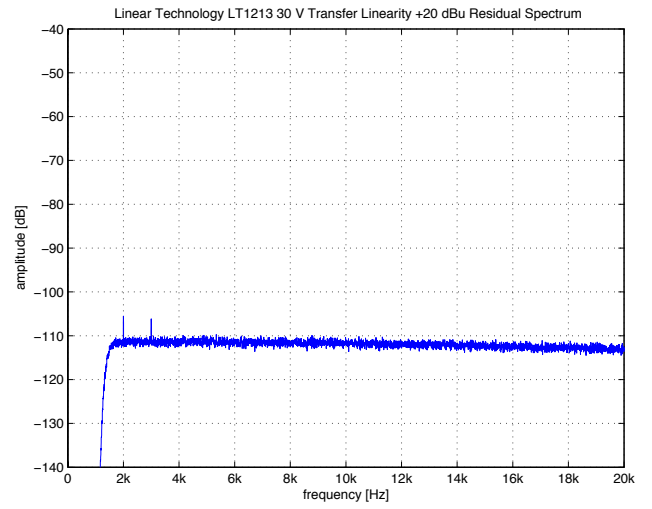
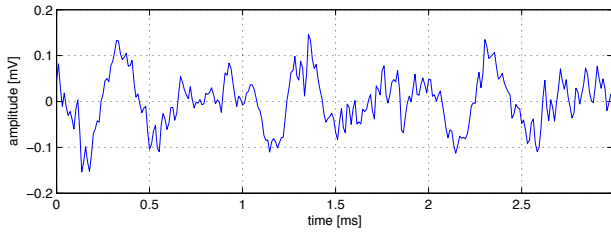
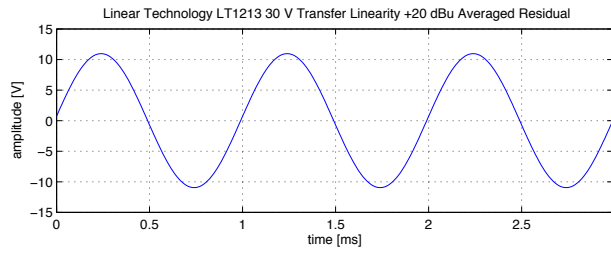
Table 3.10: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 15 \text{ V}$ .

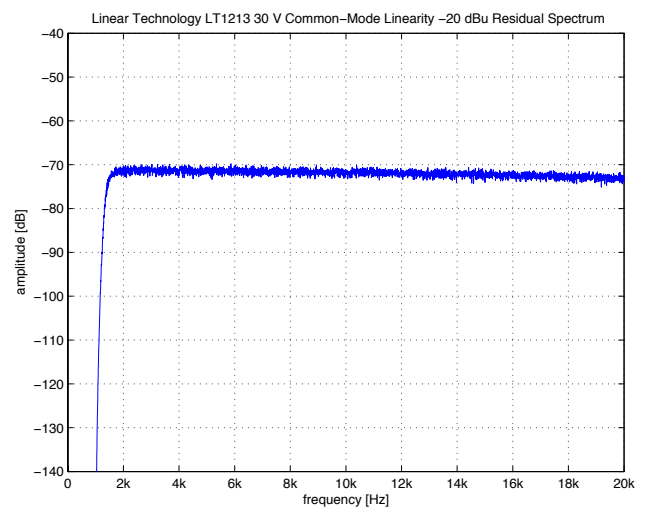
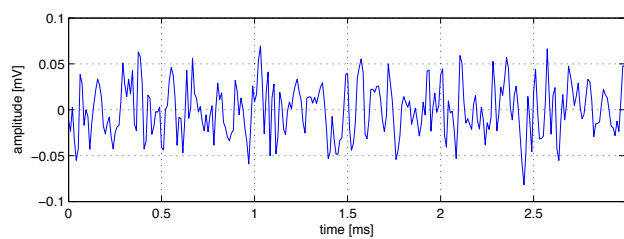
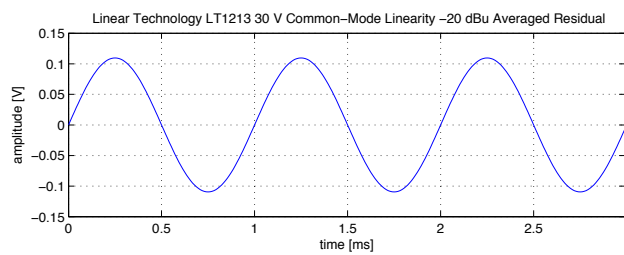
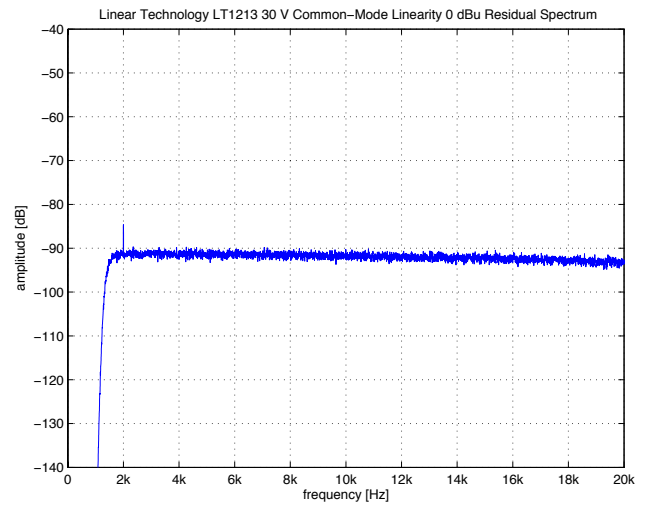
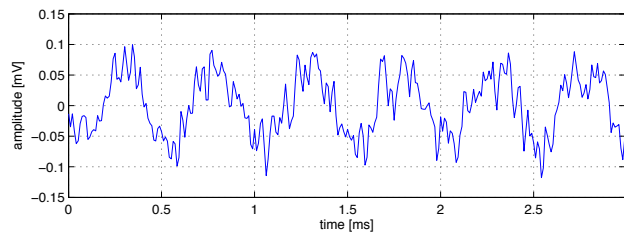
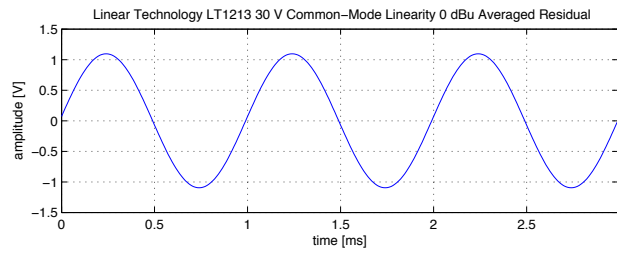
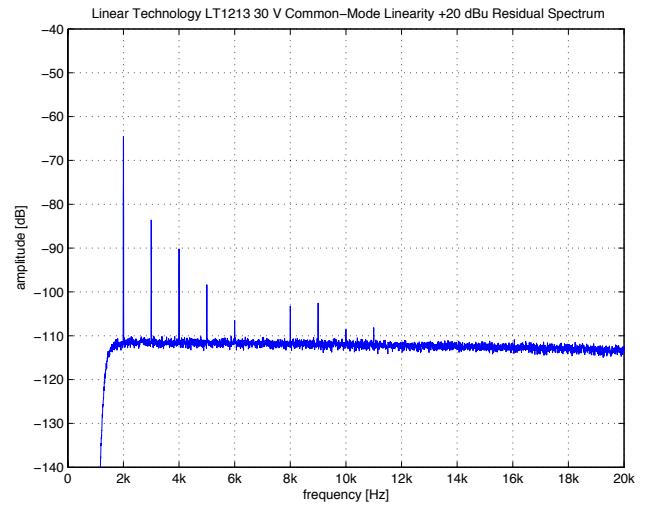
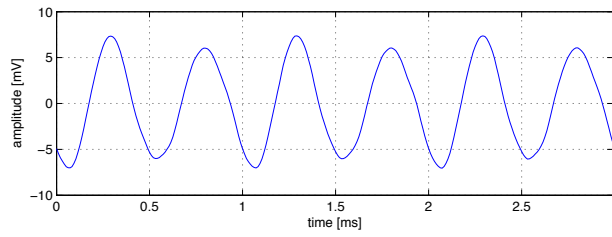
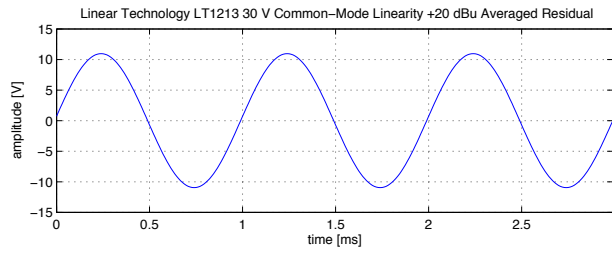
A bipolar input opamp based on a two-stage topology. Note rather wide common-mode and output swing, very low minimum power supply voltage and relatively low quiescent current. Input voltage noise is rather high, fortunately the current noise is low which makes the amplifier usable for higher source impedances nonetheless. A quad version is available as LT1214.

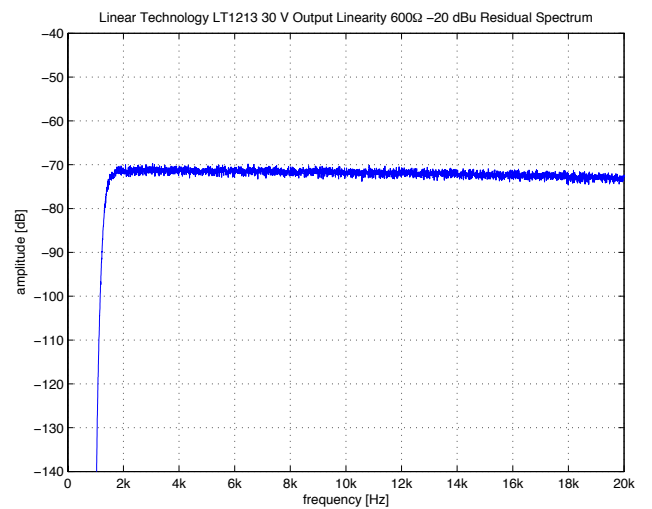
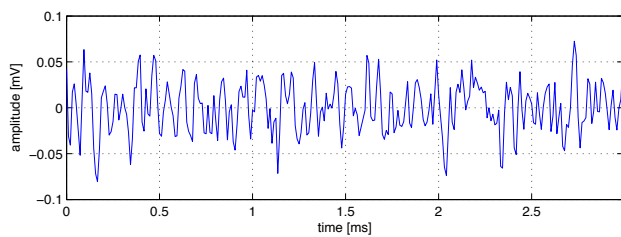
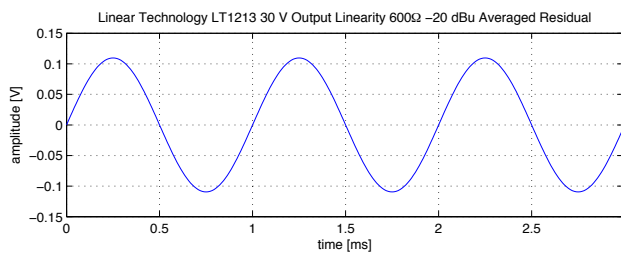
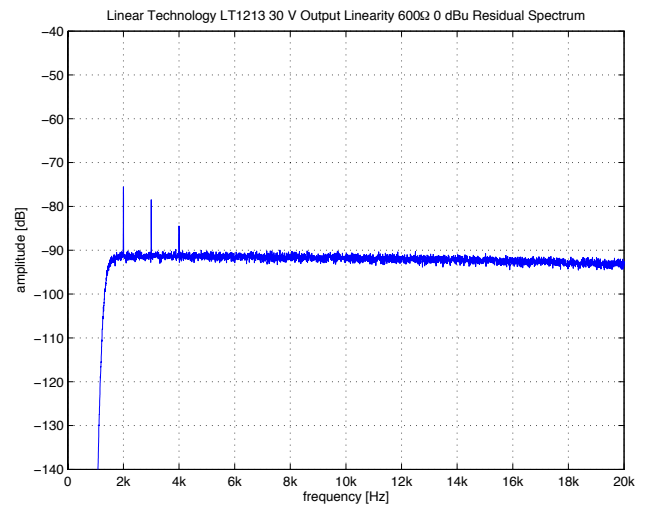
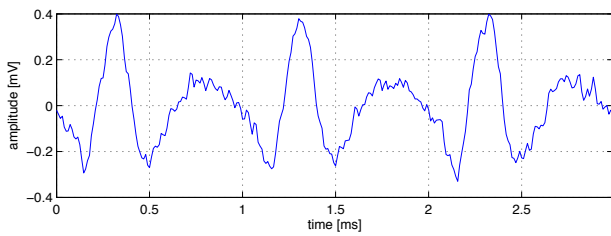
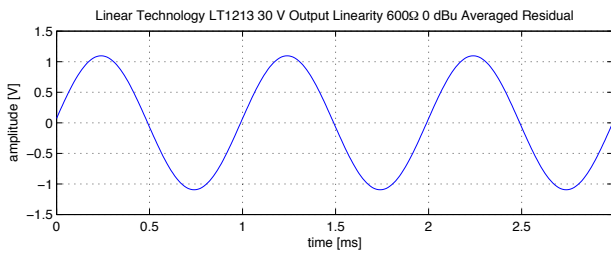
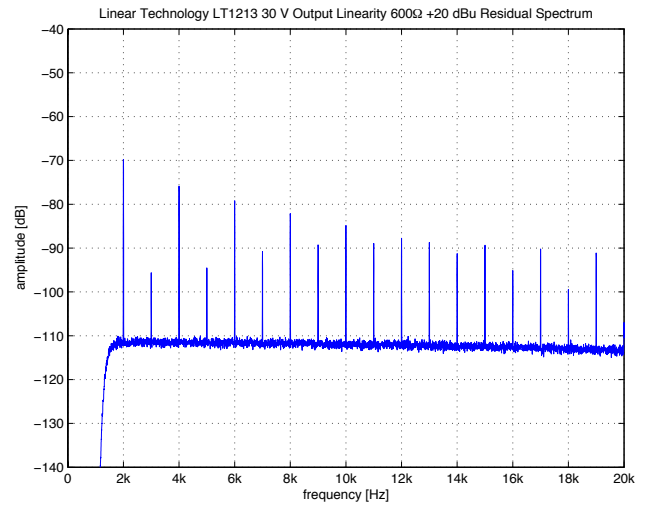
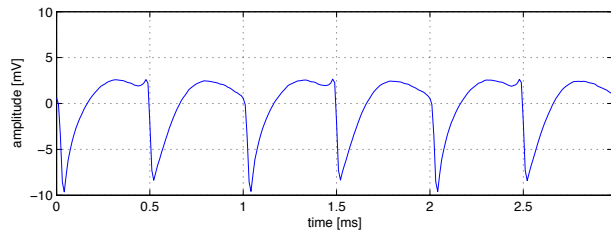
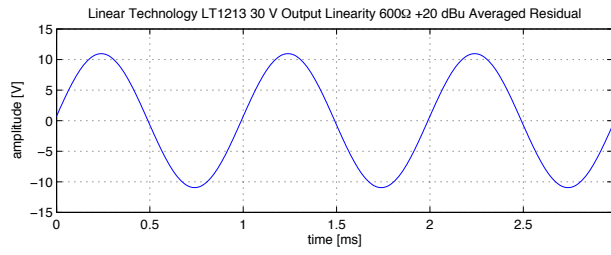
At low and medium frequencies the transfer linearity is exceptionally good, but degrades above the audio frequency band; note however the untypical behaviour in the high-frequency linearity plot where both the inverting and noninverting measurement show very similar performance. Common-mode distortion is a serious issue at higher frequencies and output loading causes a rather substantial distortion increase—the resulting distortion residual waveform is unique with its asymmetrical form. The input impedance linearity appears to be similar to JFET input amplifiers, e.g. showing mainly capacitive effects.

This part may be interesting for low-power/portable applications as most amplifiers with comparable performance have higher quiescent current and less input/output voltage range. Reasonably priced, not a bargain though.









### 3.11 Linear Technology LT1215

<b>Number of Channels</b>	2
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	1.43 US\$ at 1k units (July 2008)

Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		250	650	$\mu\text{V}$
Input Bias Current		360	550	nA
Input Offset Current		30	1100	nA
Gain Bandwidth Product	15	23		MHz
Slew-Rate	40	50		V/ $\mu\text{S}$
Input Voltage Noise (f = 1 kHz)		12.5		nV/ $\sqrt{\text{Hz}}$
Input Current Noise (f = 1 kHz)		0.5		pA/ $\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	+12.9/−14.9	+13.1/−15.1		V
Output Voltage Swing ( $I_{\text{OUT}} = 30 \text{ mA}$ )	+13.5/−14	+13.75/−14.4		V
Output Current	$\pm 30$	$\pm 50$		mA
Power Supply Voltage	$\pm 2$		$\pm 18$	V
Quiescent Current per Amplifier	3.3	6.3	9.2	mA

Table 3.11: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 15 \text{ V}$ .

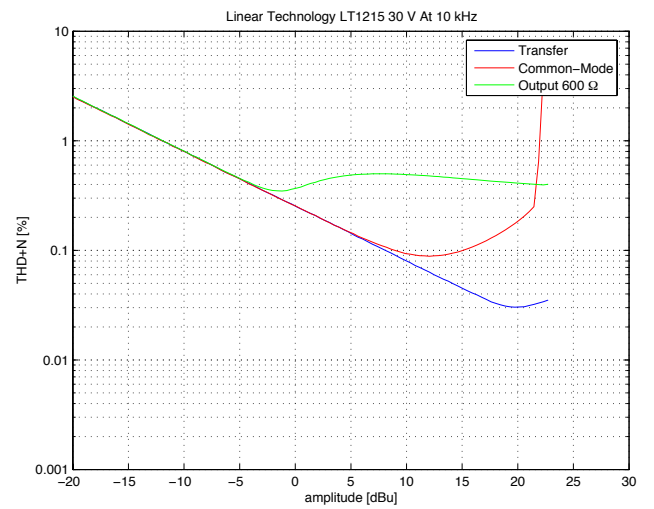
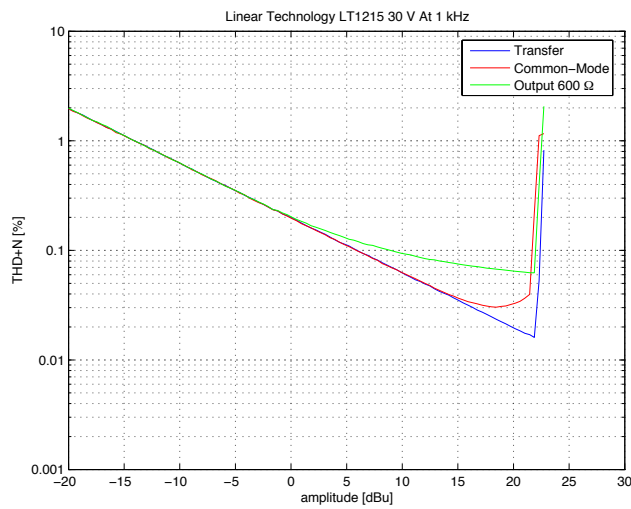
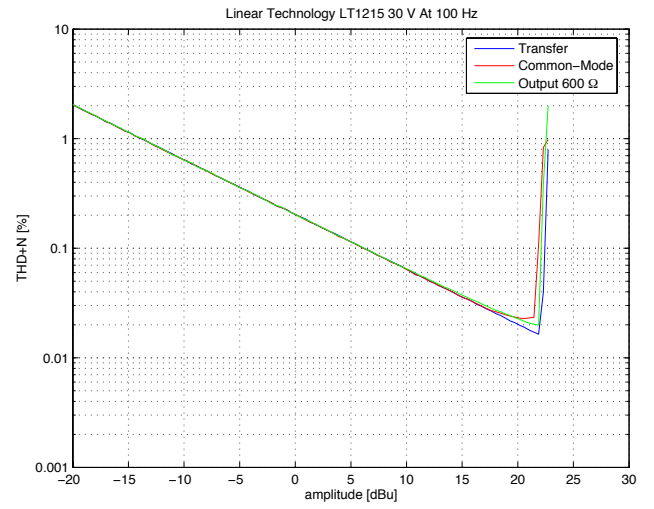
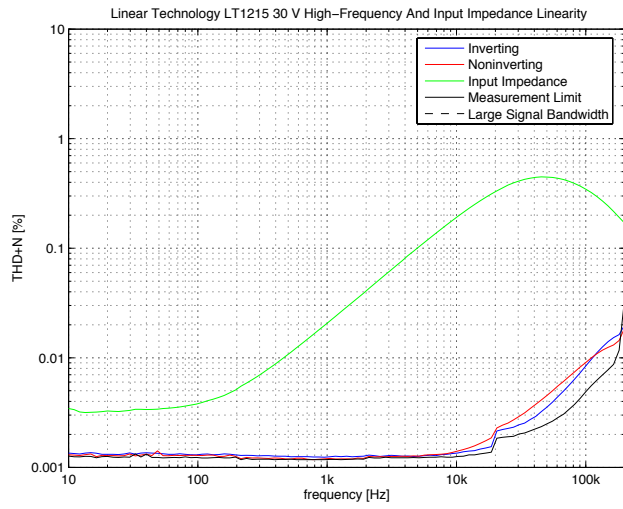
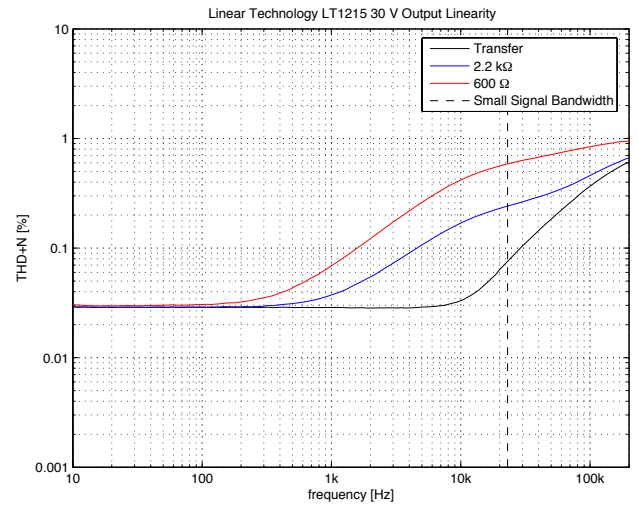
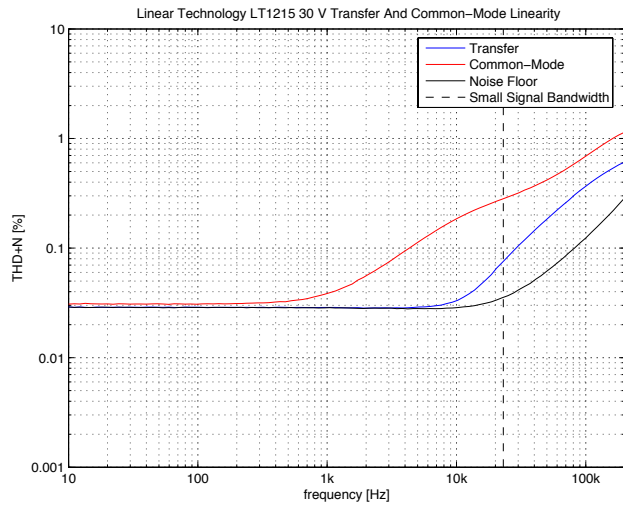
This amplifier uses the same topology as the LT1213 (i.e. a two-stage architecture); the performance differences—most noticeably with respect to slew-rate and quiescent current—are presumably a result of running a degenerated input stage at higher tail current. Voltage noise is high and current noise not particularly low either. A quad version is available with the part number LT1216.

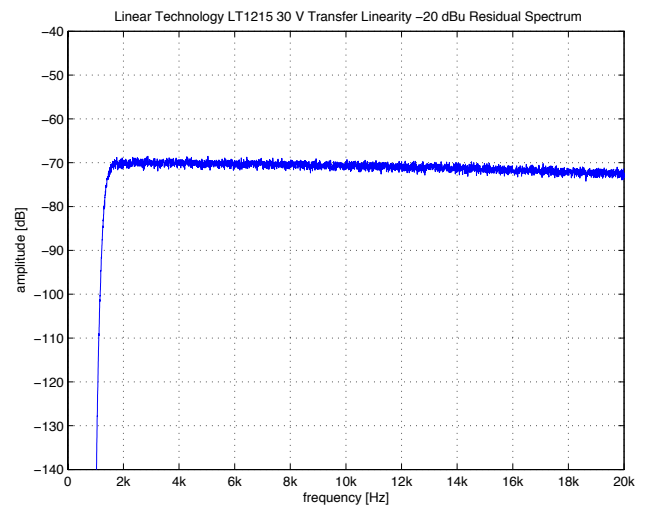
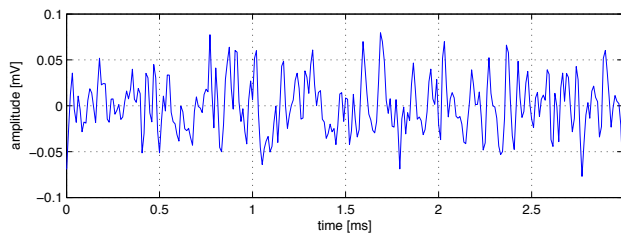
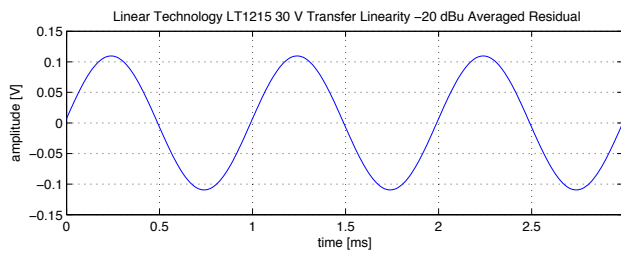
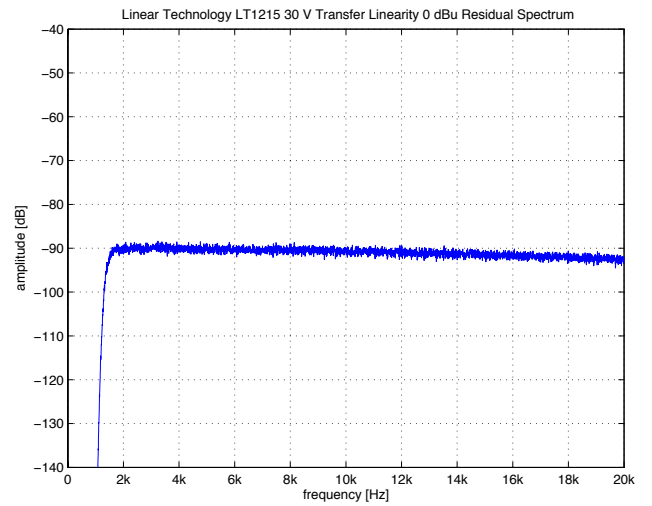
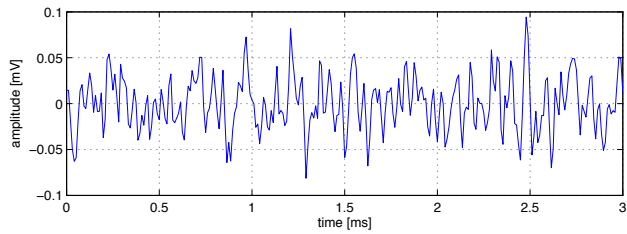
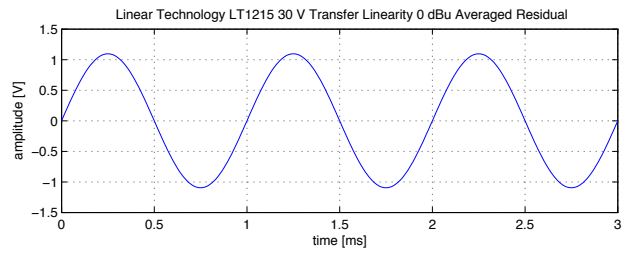
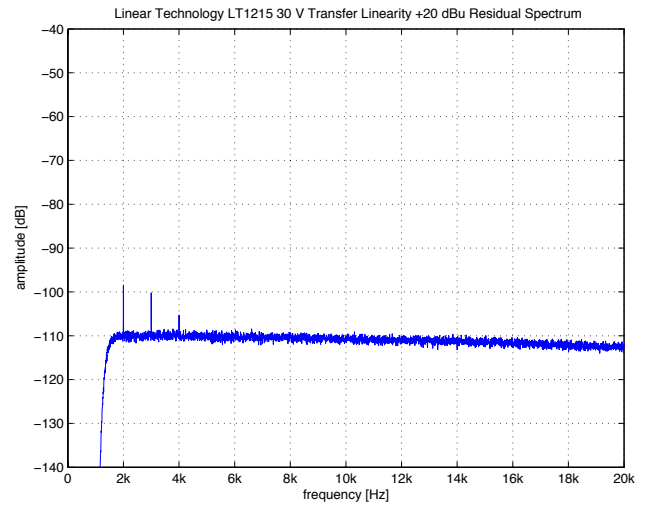
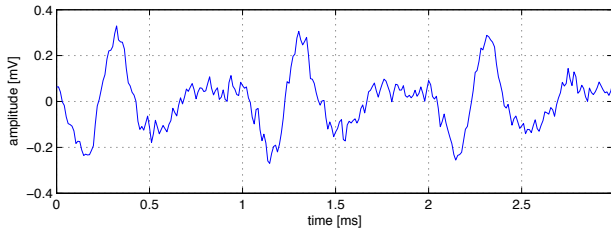
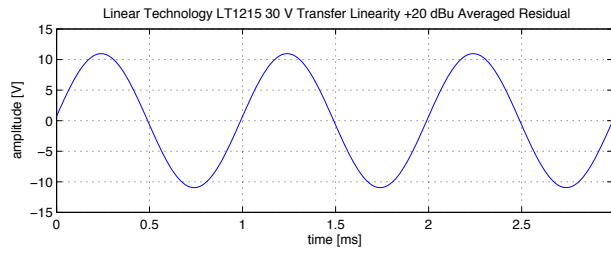
Surprisingly the transfer linearity within the audio frequency band is worse than for the LT1213.<sup>6</sup> At higher frequencies linearity is greatly increased though due to the higher slew-rate. Output distortion magnitude and residual waveform is revealingly similar to the LT1213, confirming that the two amplifiers have indeed very similar circuits. Common-mode linearity is clearly present above 1 kHz, but at least better than for the LT1213.

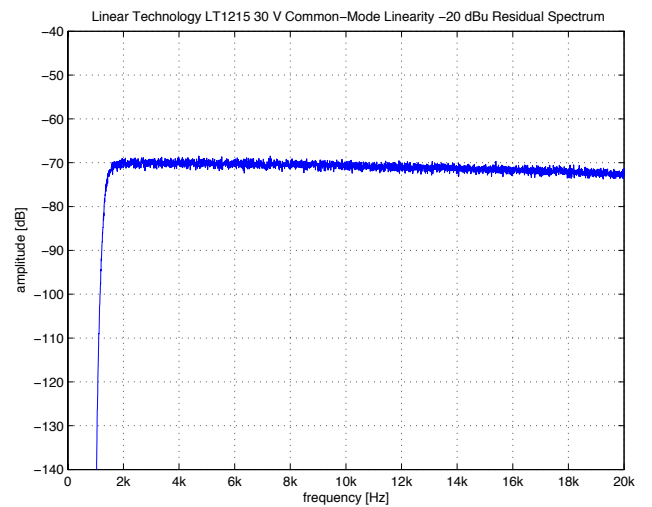
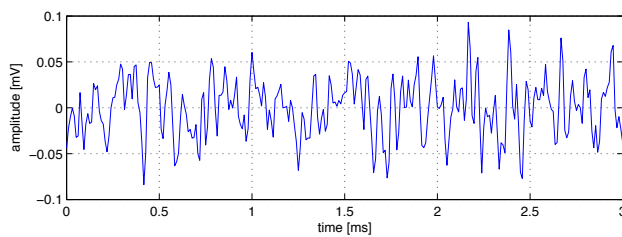
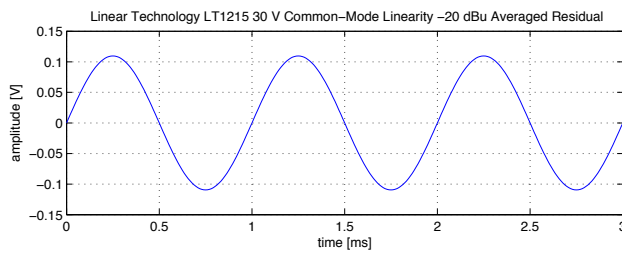
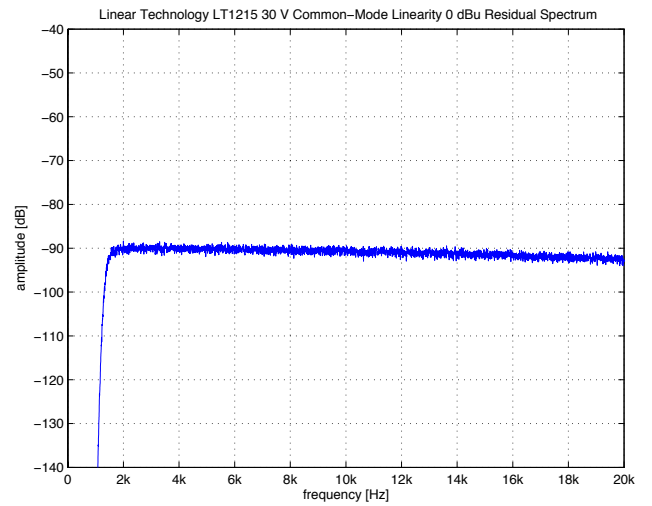
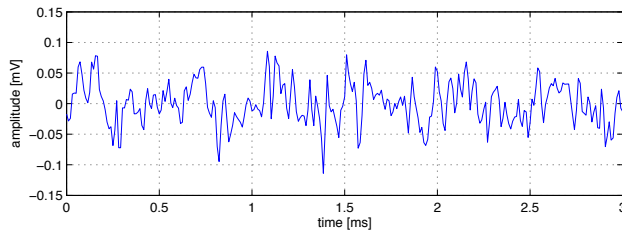
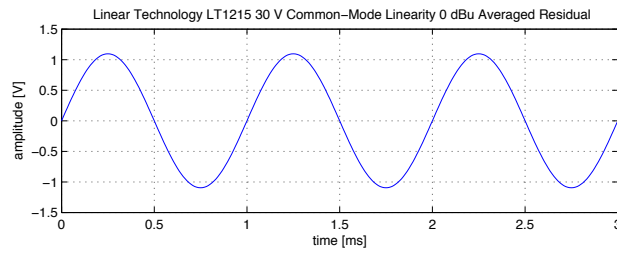
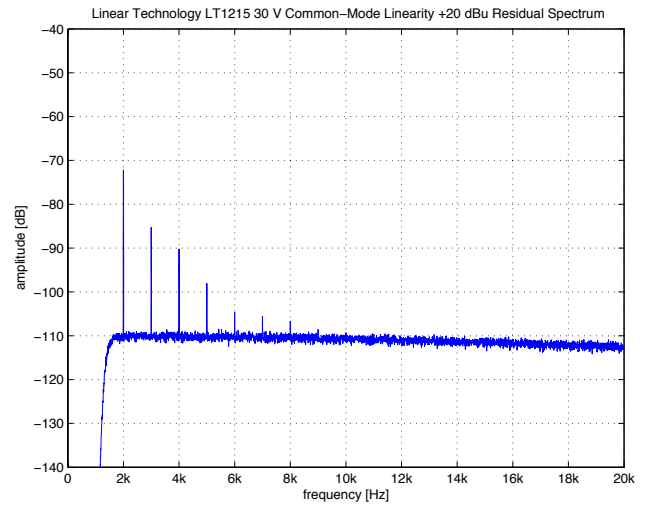
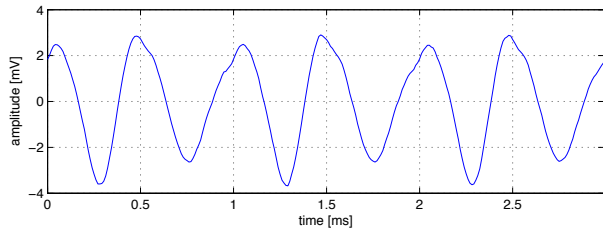
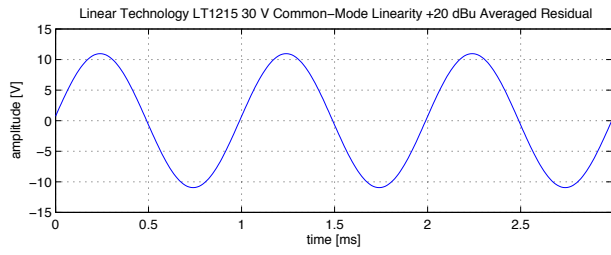
Overall distortion performance is not at all bad, but not exciting either. In most cases another amplifier will probably be more suitable, except perhaps where the large input and output voltage range of this device are needed.

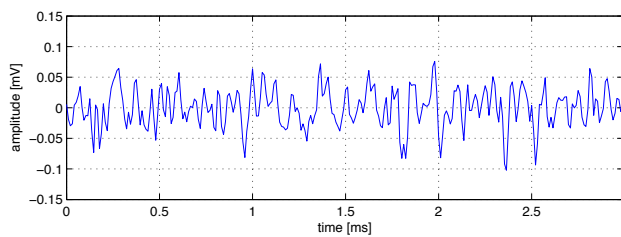
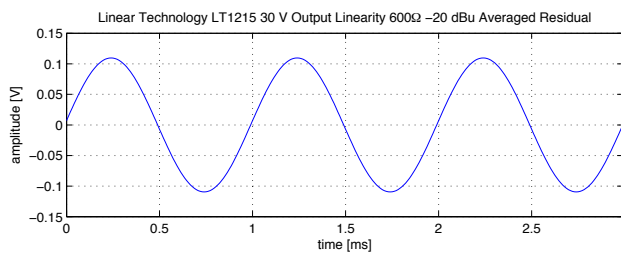
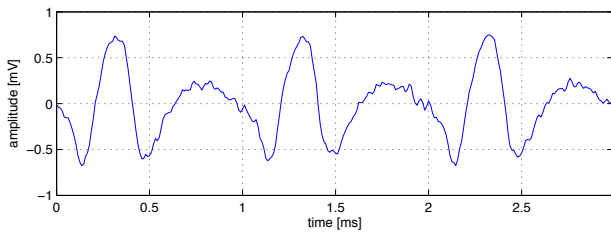
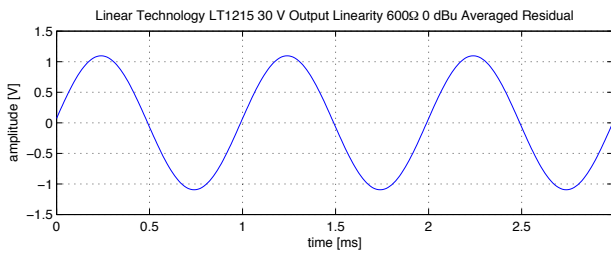
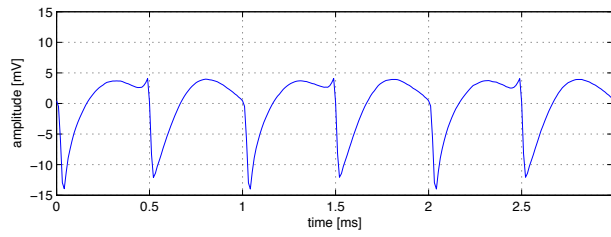
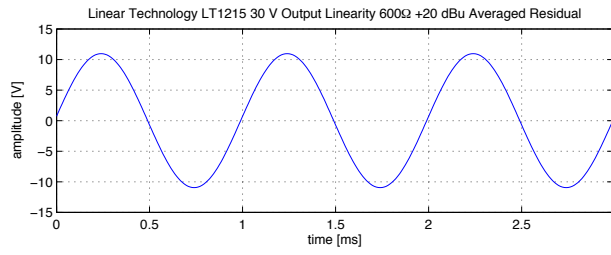
<sup>6</sup>This is probably a result of the presumably degenerated input stage. In a two-stage topology the second stage can be the dominating source for transfer distortion at lower frequencies; if the input stage is degenerated and the compensation capacitor value reduce, the total feedback for the second stage will be reduced and hence its distortion highlighted.











### 3.12 Linear Technology LT1358

<b>Number of Channels</b>	2
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	1.95 US\$ at 1k units (August 2008)

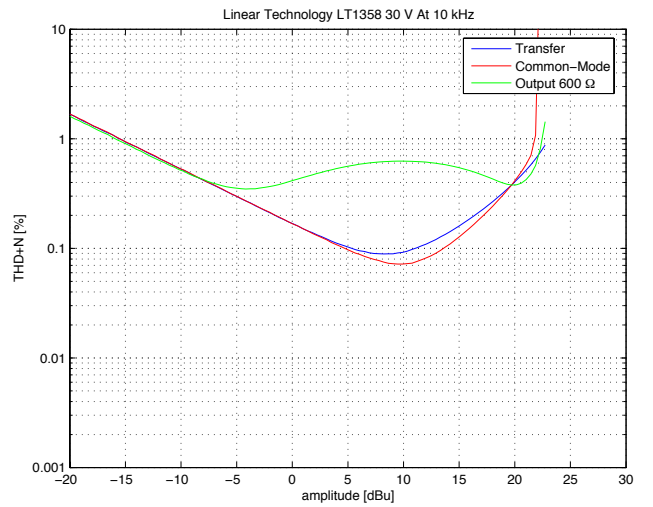
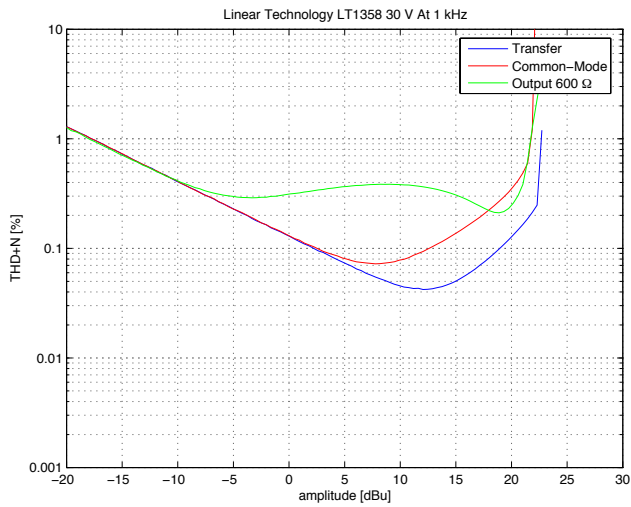
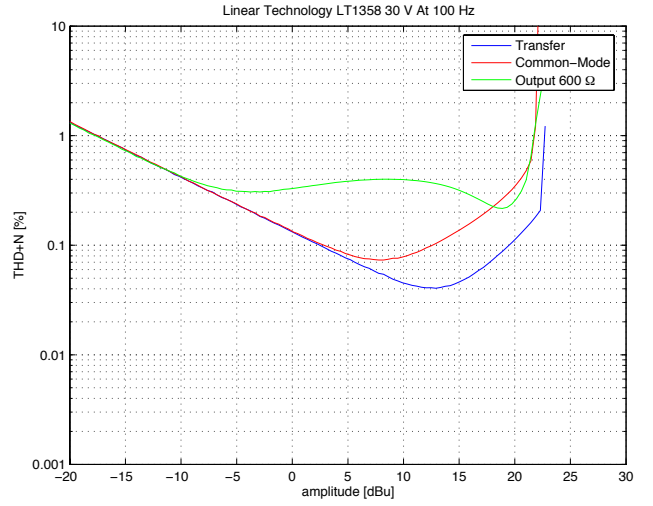
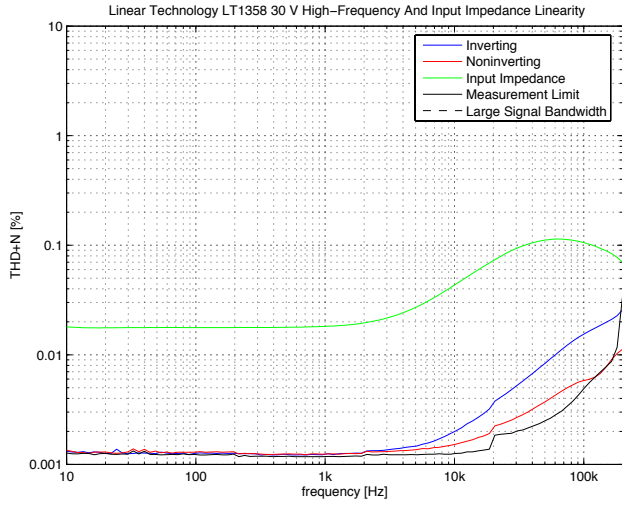
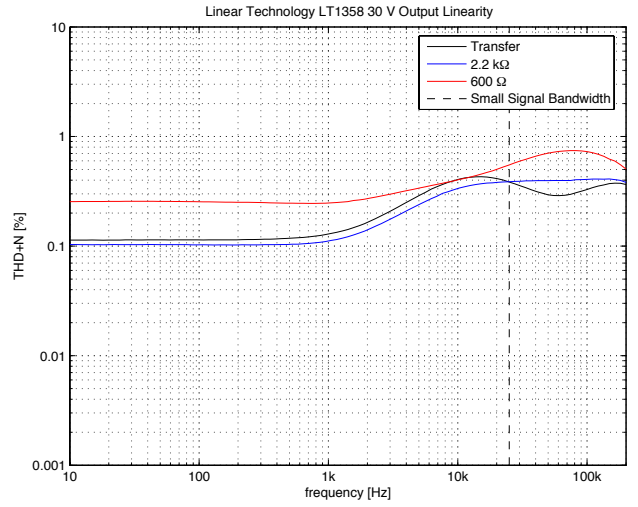
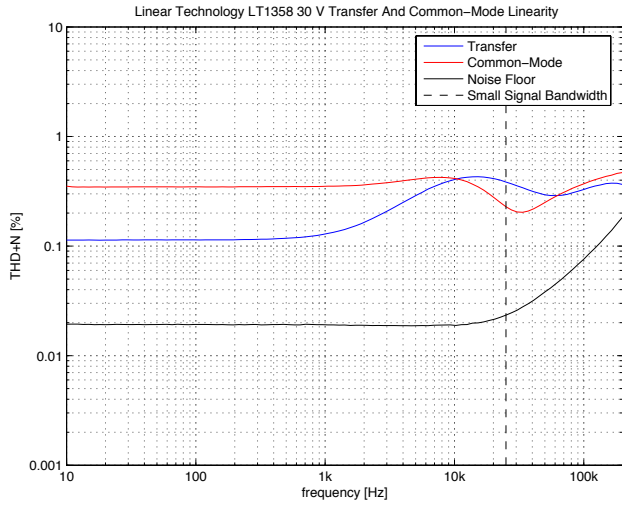
Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		0.2	0.6	mV
Input Bias Current		120	500	nA
Input Offset Current		40	120	nA
Gain Bandwidth Product	18	25		MHz
Slew-Rate	300	600		V/ $\mu$ S
Input Voltage Noise (f = 10 kHz)		8		nV/ $\sqrt{\text{Hz}}$
Input Current Noise (f = 10 kHz)		0.8		pA/ $\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 12$	+13.4/−13.2		V
Output Voltage Swing ( $R_L = 1 \text{ k}\Omega$ )	$\pm 13.3$	$\pm 13.8$		V
Output Voltage Swing ( $R_L = 500 \Omega$ )	$\pm 12.5$	$\pm 13$		V
Output Current	$\pm 25$	$\pm 30$		mA
Power Supply Voltage	$\pm 2.5$		$\pm 18$	V
Quiescent Current per Amplifier		2	2.5	mA

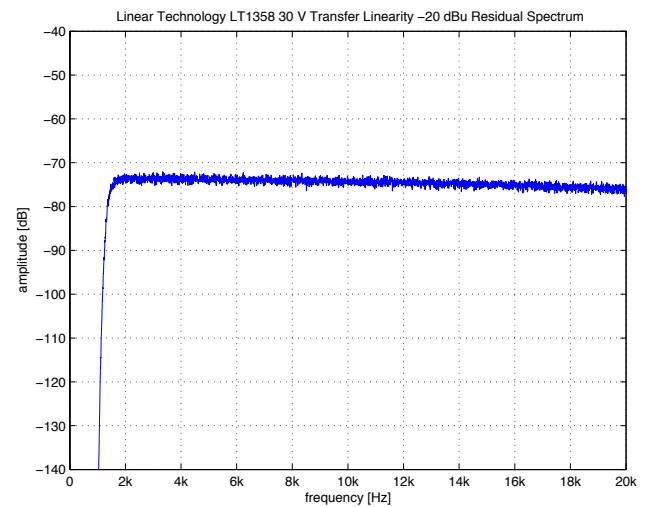
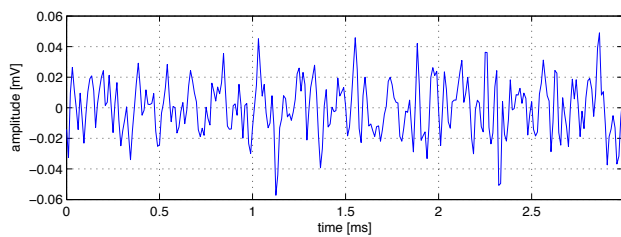
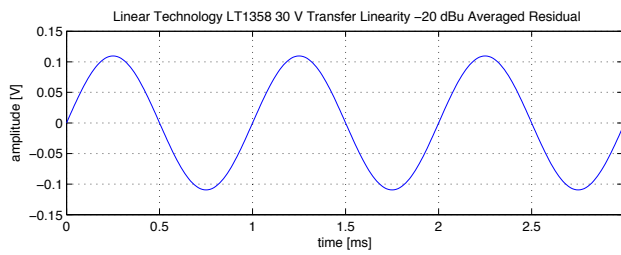
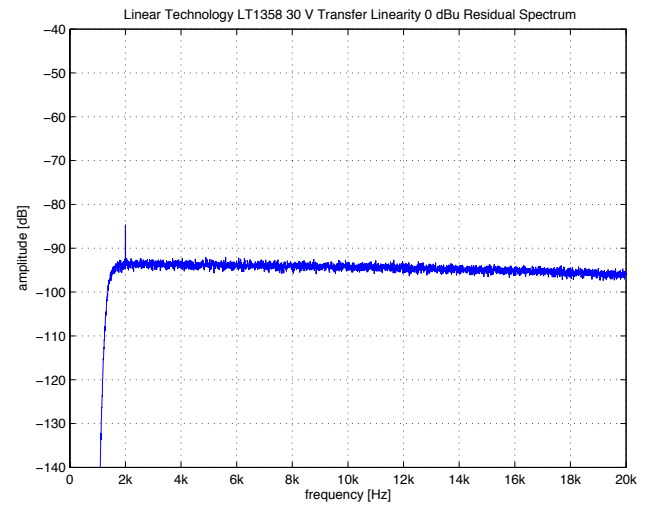
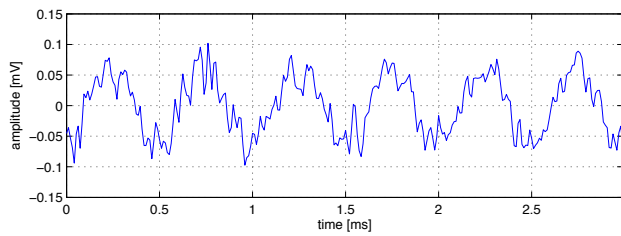
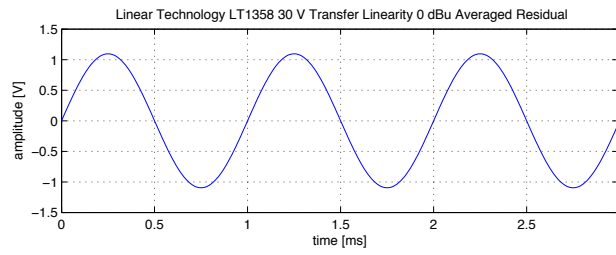
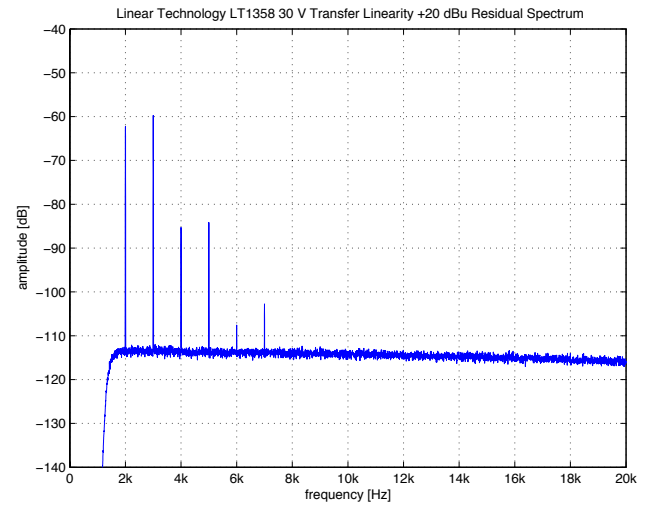
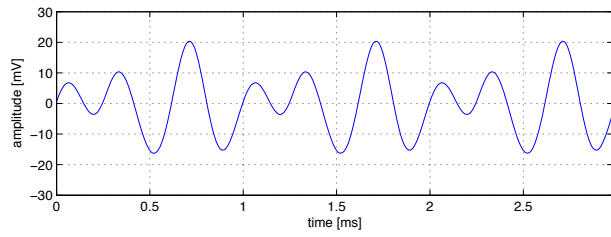
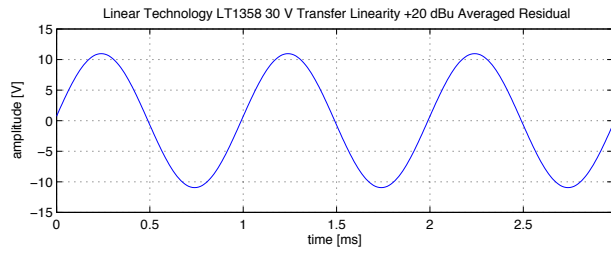
Table 3.12: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 15 \text{V}$ .

This amplifier is part of a large amplifier family (LT1354 through LT1363) which achieves high slew-rate and gain bandwidth at low quiescent current by means of a remarkable single-stage topology with class AB input stage. This performance is attained with pretty good DC precision (at least compared to typical current feedback amplifiers which offer similar slew-rate) and wide input and output voltage ranges, but at the cost of relatively high voltage and current noise. Equivalent single (LT1357) and quad (LT1359) amplifier packages are available.

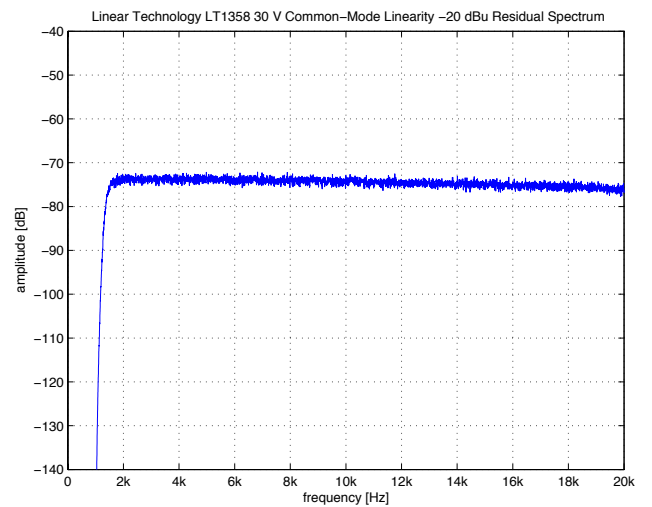
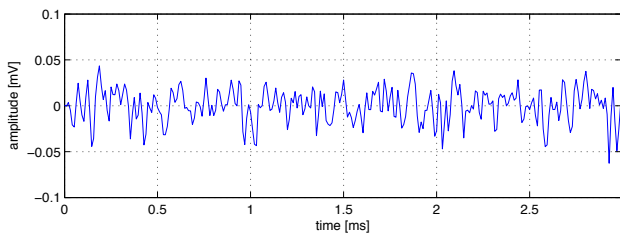
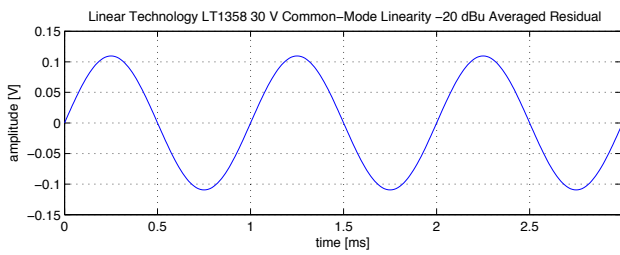
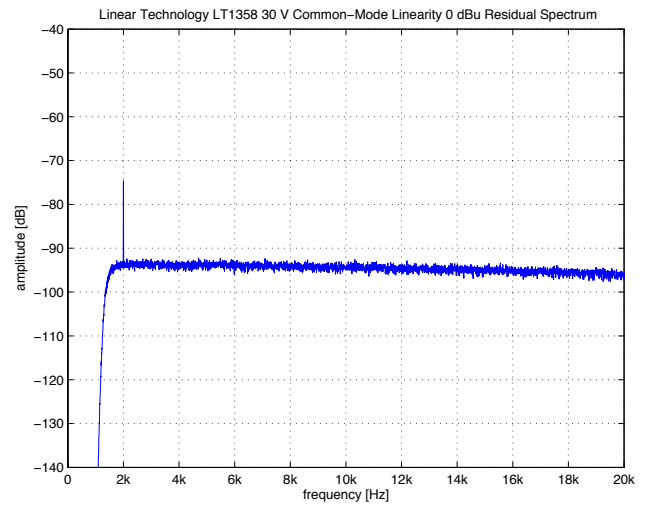
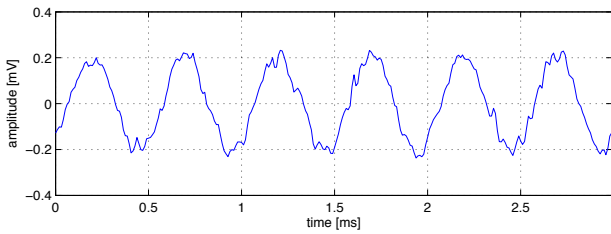
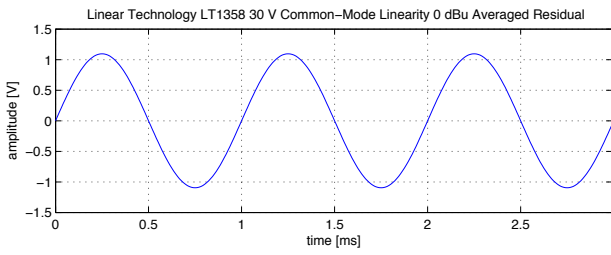
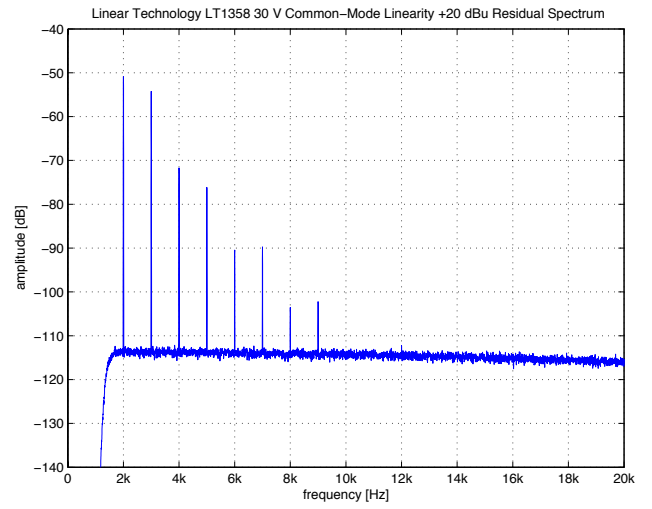
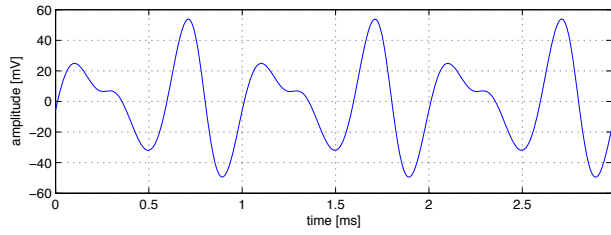
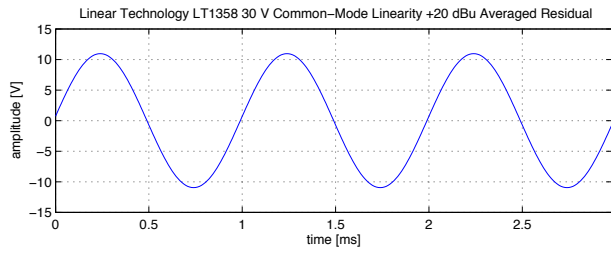
The distortion performance of this amplifier is less frequency dependent than what is typically observed for standard input stage topologies but also overall higher. Particularly conspicuous is distortion from output stage loading (measurable down to low levels) and common-mode effects. The input impedance modulation is unique in that it has a relatively low capacitive contribution but shows substantial frequency-independent distortion. High-frequency distortion is better than for typical amplifiers using standard input stage architectures and similarly low quiescent current but clearly not superior to standard amplifiers at higher quiescent current—even if they have substantially lower slew-rate specification.

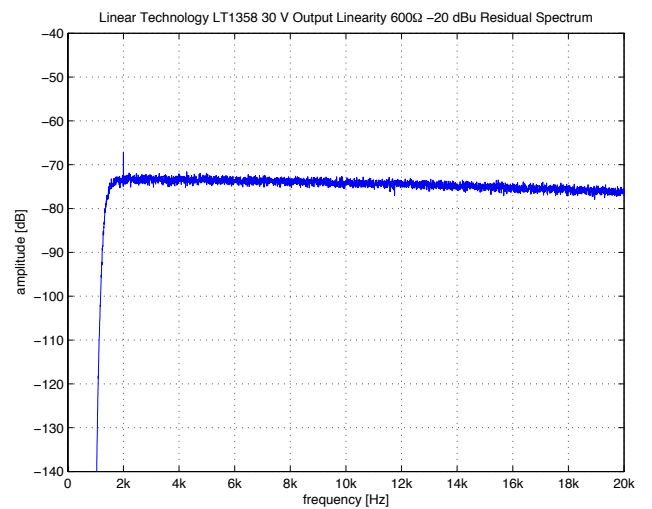
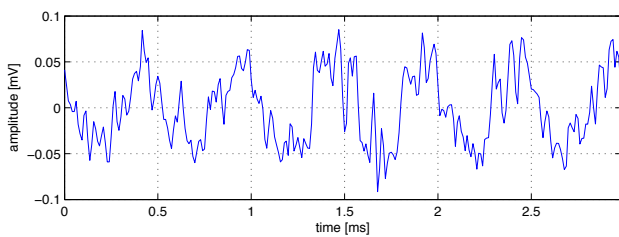
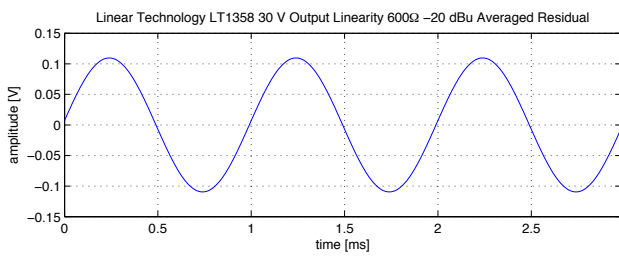
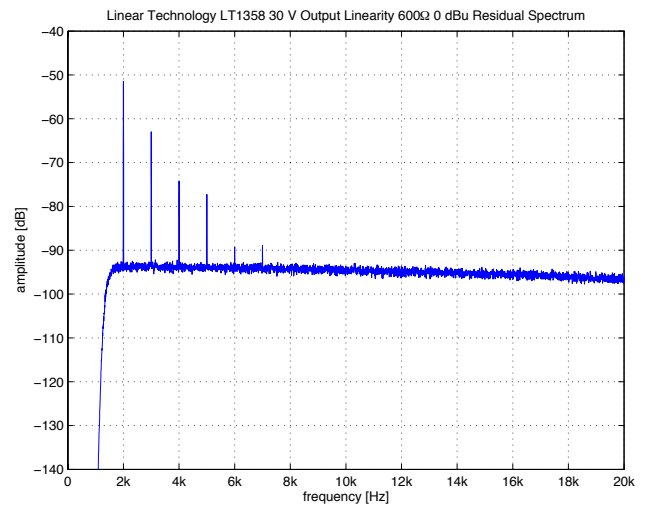
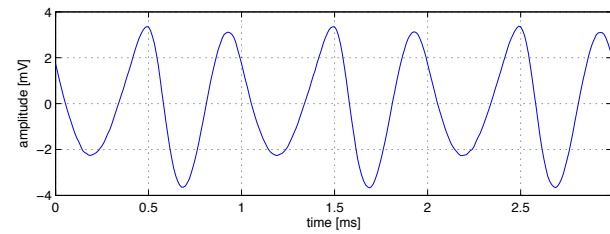
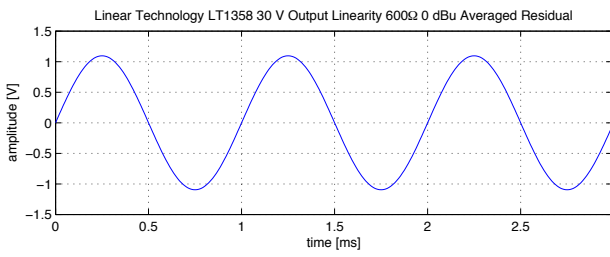
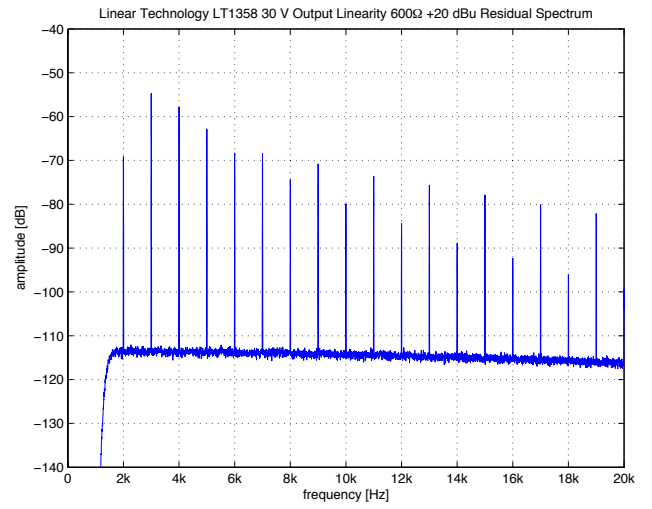
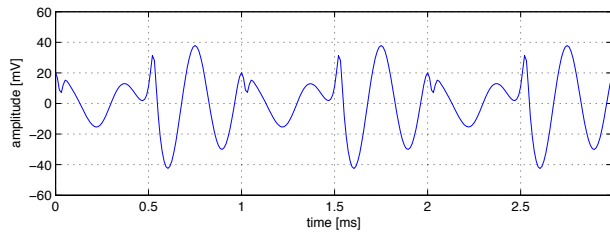
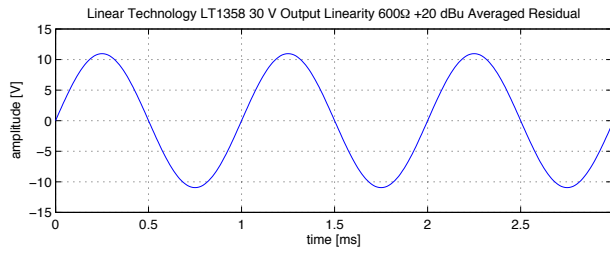
This part might be interesting where good high-frequency distortion must be achieved at low quiescent current; otherwise there seems little to recommend this part.











### 3.13 Linear Technology LT1363

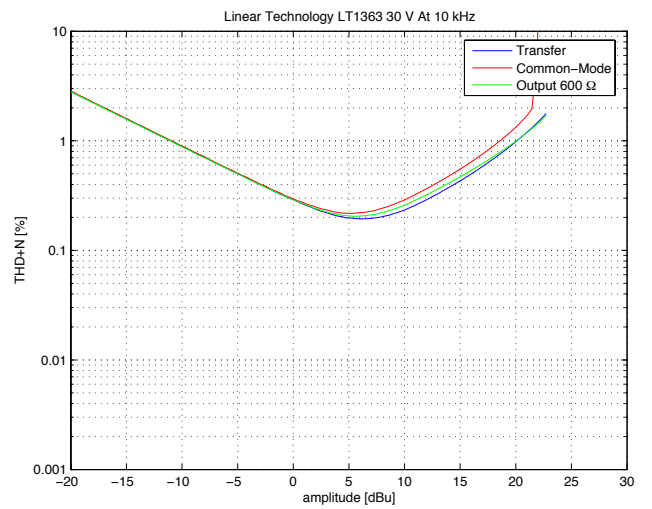
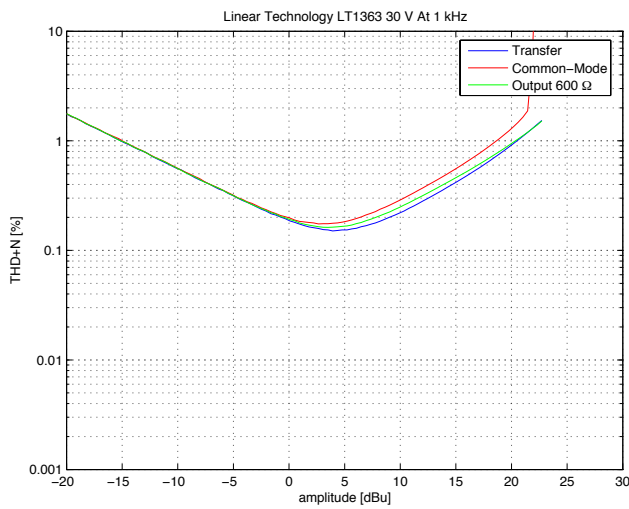
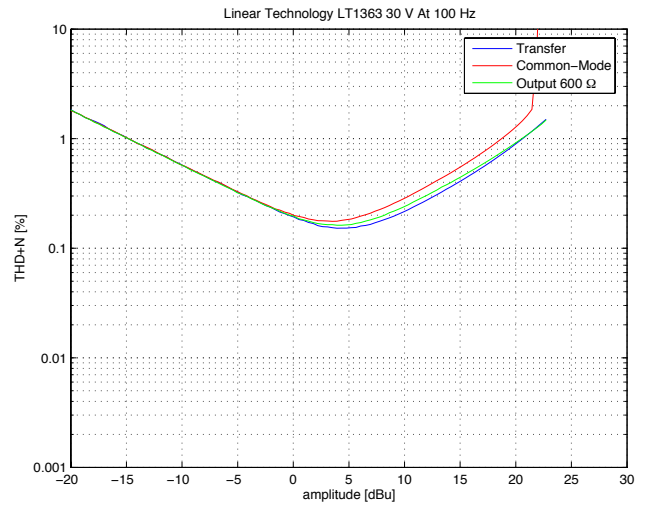
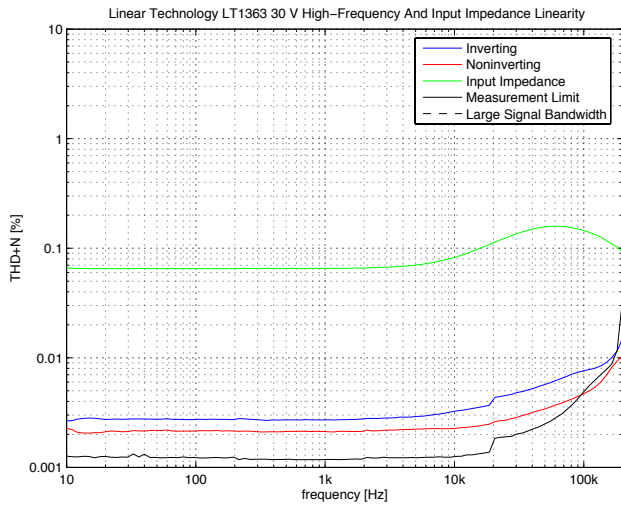
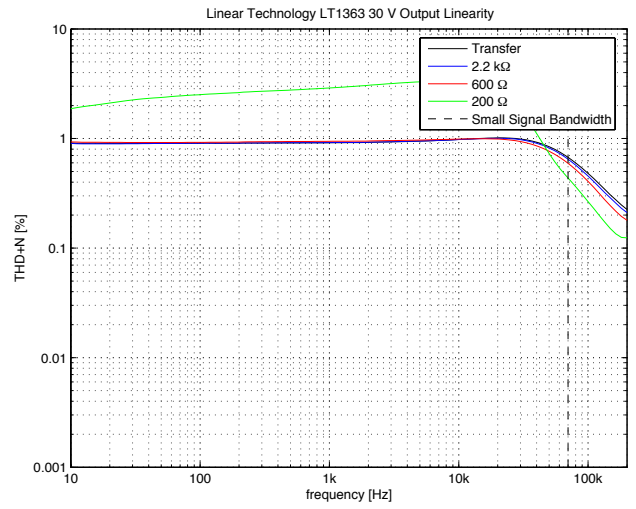
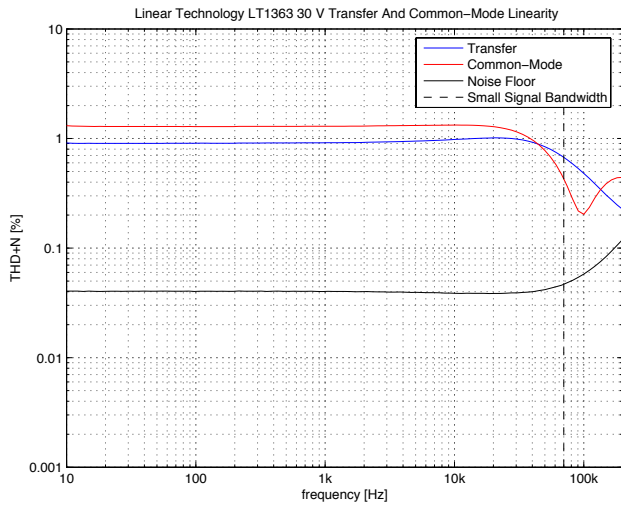
<b>Number of Channels</b>	1
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	2.40 US\$ at 1k units (August 2008)

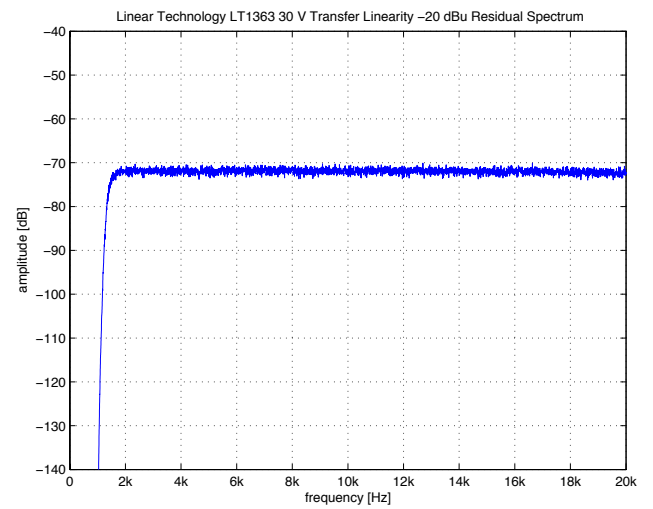
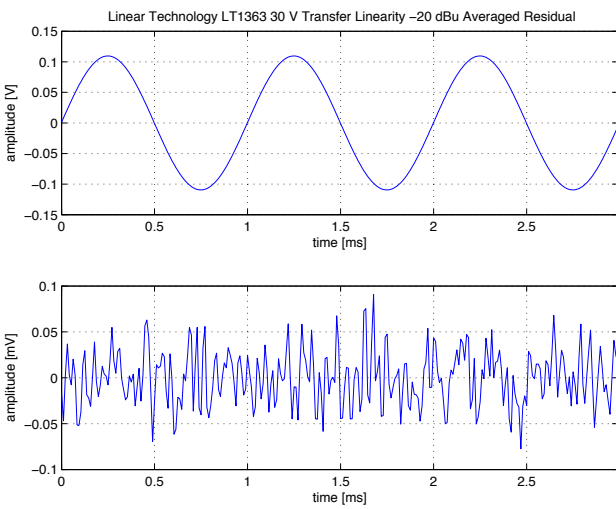
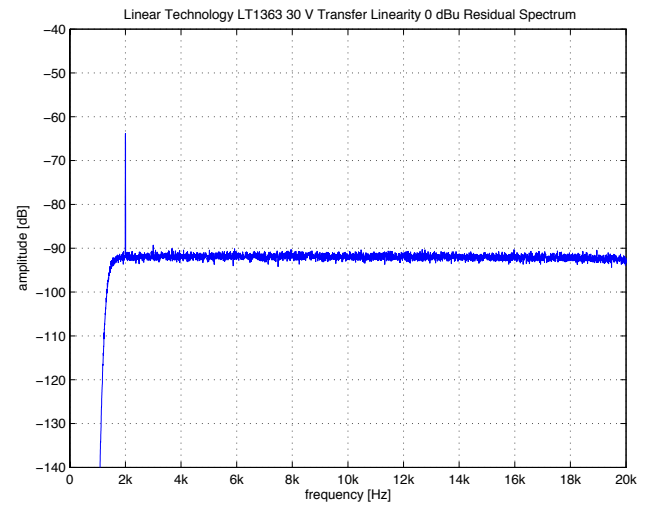
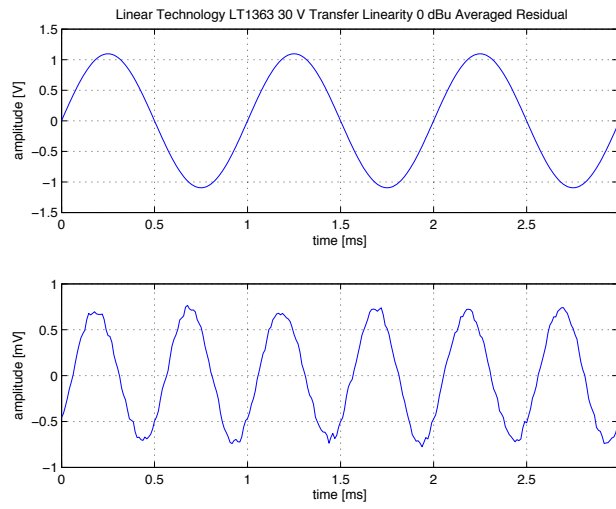
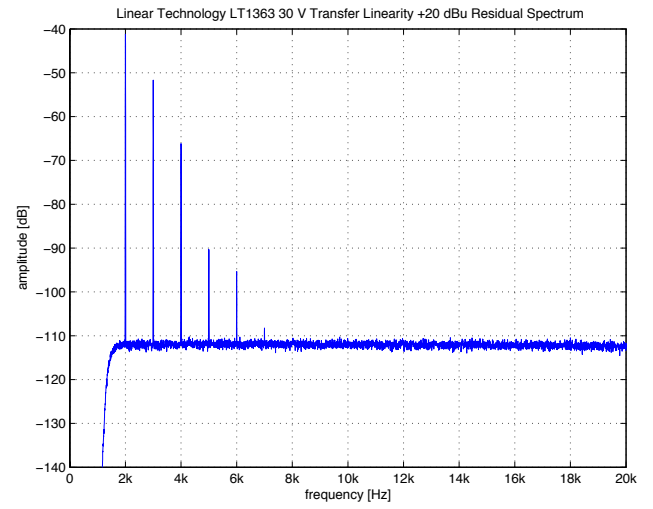
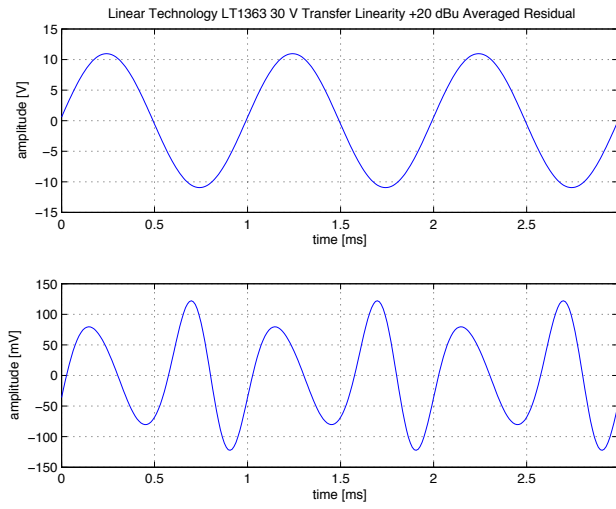
Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		0.5	1.5	mV
Input Bias Current		0.6	2	$\mu\text{A}$
Input Offset Current		120	350	nA
Gain Bandwidth Product		70		MHz
Slew-Rate	750	1000		V/ $\mu\text{S}$
Input Voltage Noise (f = 10 kHz)		9		nV/ $\sqrt{\text{Hz}}$
Input Current Noise (f = 10 kHz)		1		pA/ $\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 12$	+13.4/ - 13.2		V
Output Voltage Swing ( $R_L = 1 \text{ k}\Omega$ )	$\pm 13.5$	$\pm 14$		V
Output Voltage Swing ( $R_L = 500 \Omega$ )	$\pm 13$	$\pm 13.7$		V
Output Current	$\pm 50$	$\pm 60$		mA
Power Supply Voltage	$\pm 5$		$\pm 18$	V
Quiescent Current per Amplifier		6.3	7.5	mA

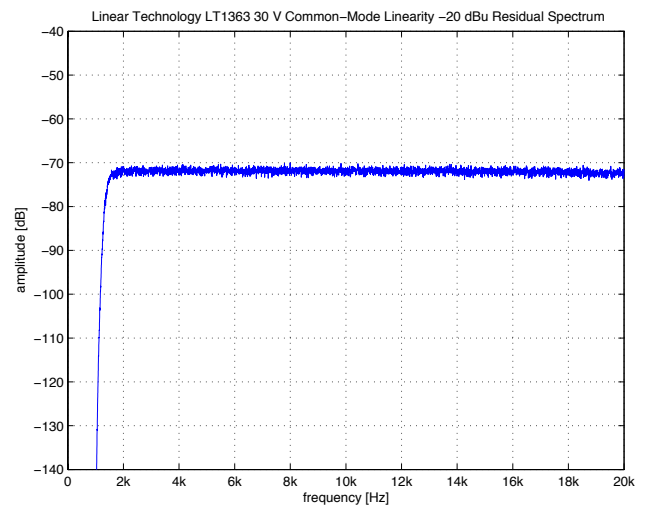
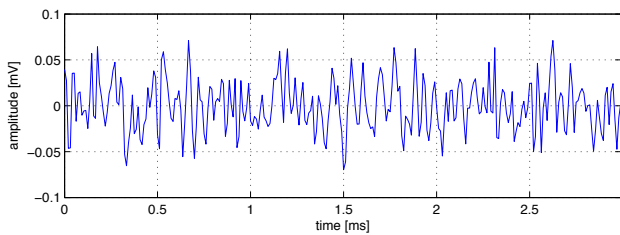
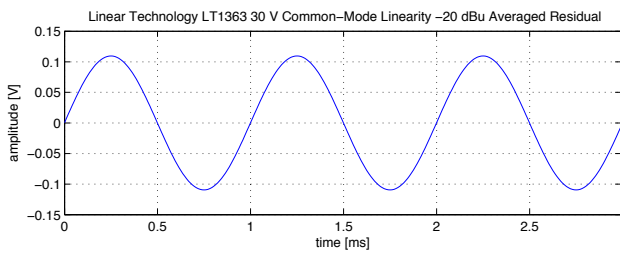
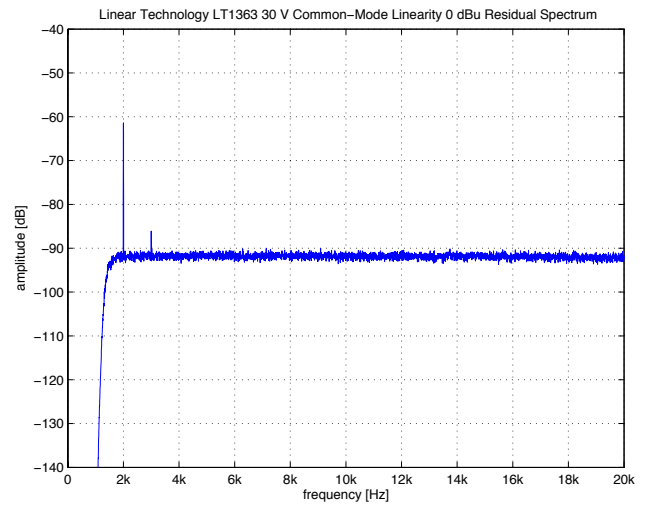
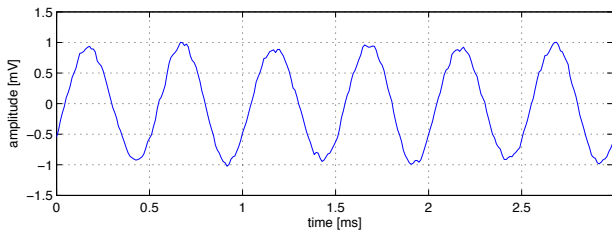
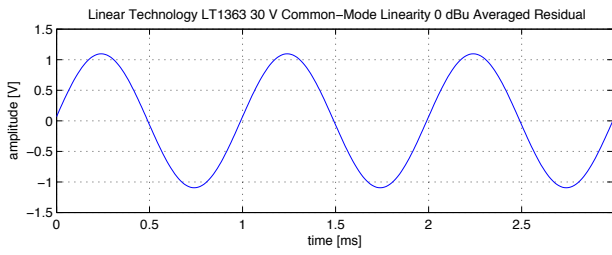
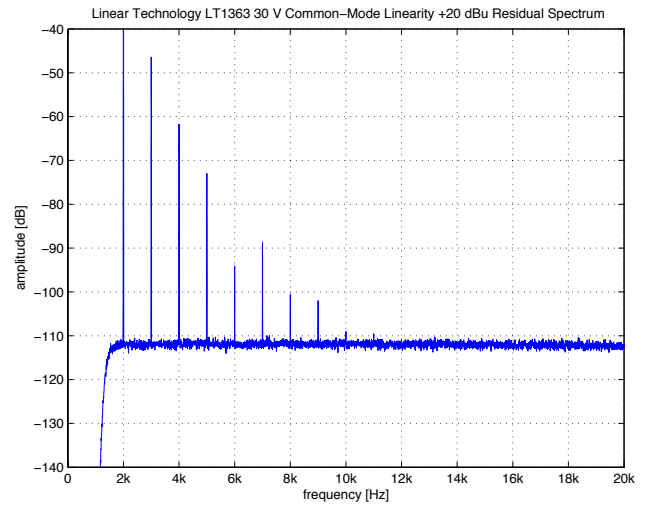
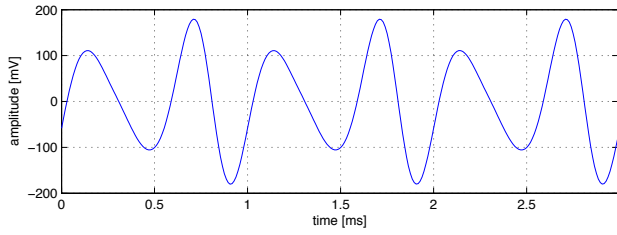
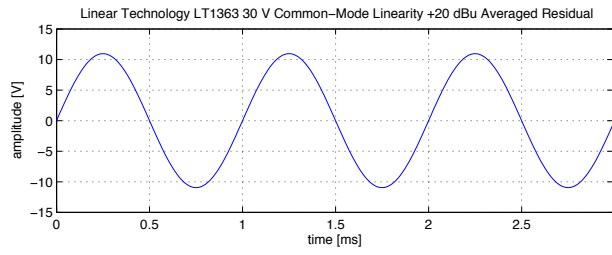
Table 3.13: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 15 \text{V}$ .

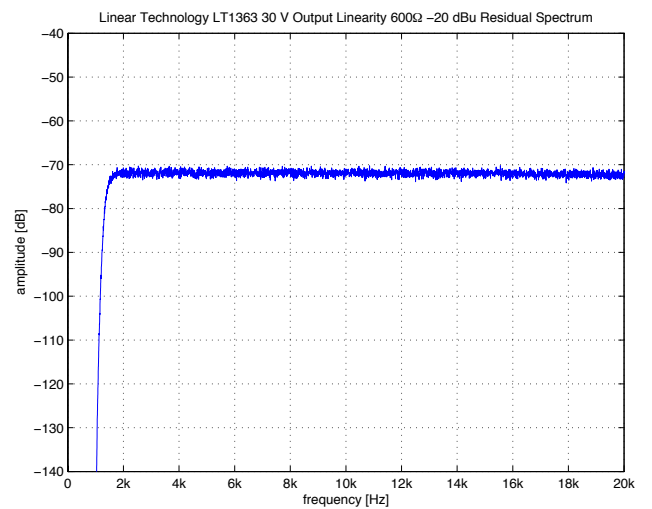
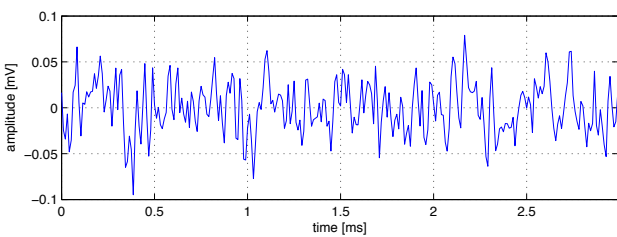
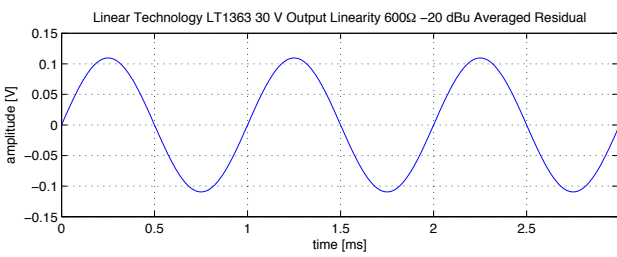
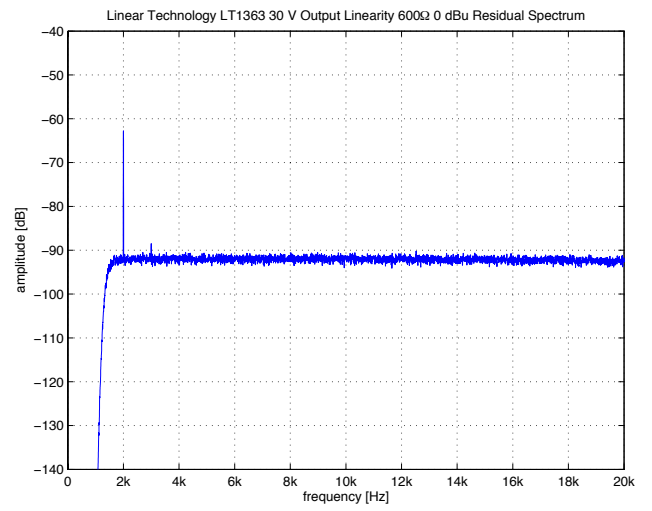
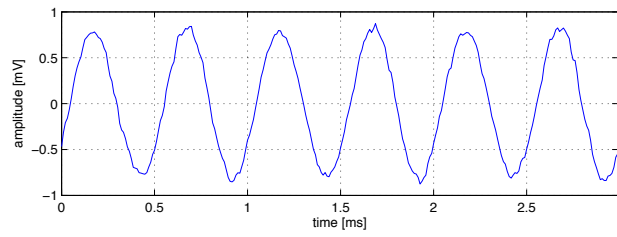
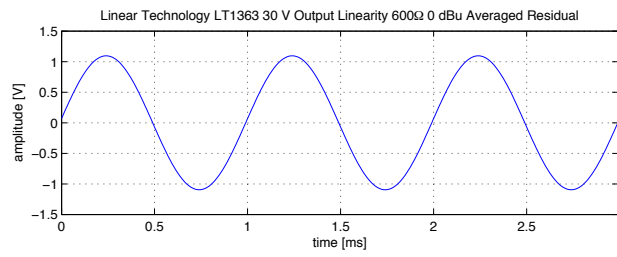
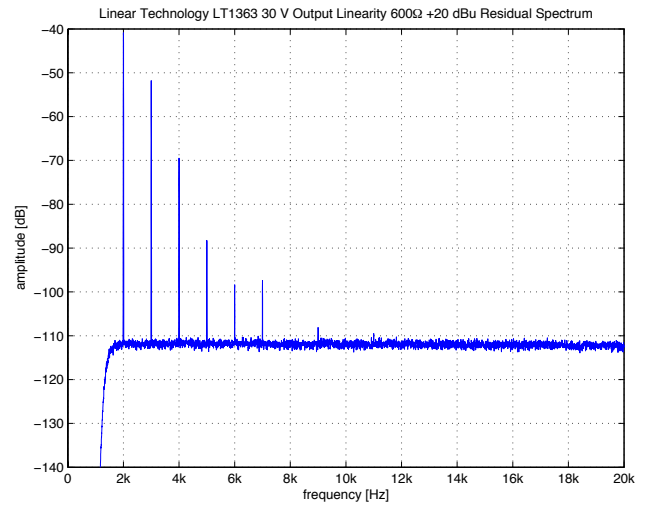
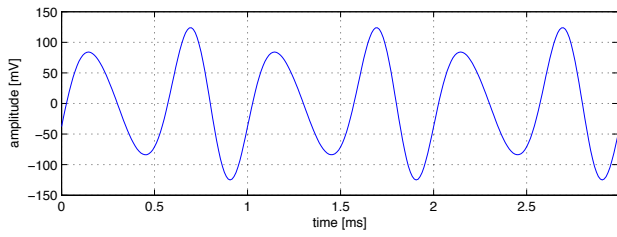
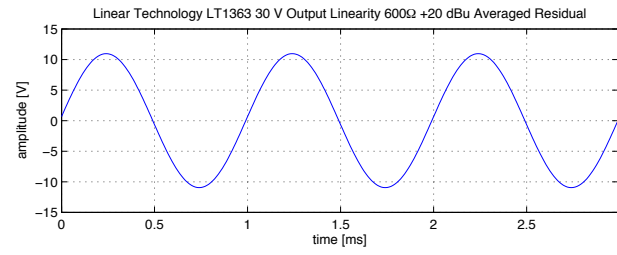
This amplifier belongs to the same opamp family as the LT1358 for which the distortion measurement results were shown on page 103. Its class AB input stage allows very high slew-rate and good gain bandwidth at comparatively low quiescent currents. The LT1363 as well as the equivalent dual and quad amplifiers LT1364 and LT1365 run at approximately three times the quiescent current of the LT1363; this reduces secondary slew-rate limits and allows higher bandwidth. Both voltage and current noise are rather high.

One would expect that with the higher quiescent current, gain bandwidth product and slew-rate this amplifier shows much improved linearity over the LT1358—right the opposite is true; all tests show very high distortion. There are better opamps out there at that price.









### 3.14 Linear Technology LT1469

<b>Number of Channels</b>	2
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	2.48 US\$ at 1k units (July 2008)

Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		50	125	$\mu\text{V}$
Input Bias Current		10	40	nA
Input Offset Current		3	10	nA
Gain Bandwidth Product	60	90		MHz
Slew-Rate	15	22		$\text{V}/\mu\text{S}$
Input Voltage Noise ( $f = 1 \text{ kHz}$ )		5		$\text{nV}/\sqrt{\text{Hz}}$
Input Current Noise ( $f = 1 \text{ kHz}$ )		0.6		$\text{pA}/\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 12.5$	$+13.5/-14.3$		V
Output Voltage Swing ( $R_L = 2 \text{ k}\Omega$ )	$\pm 12.8$	$\pm 13.5$		V
Output Current	$\pm 15$	$\pm 22$		mA
Power Supply Voltage	$\pm 4.5$		$\pm 18$	V
Quiescent Current per Amplifier		4.1	5.2	mA

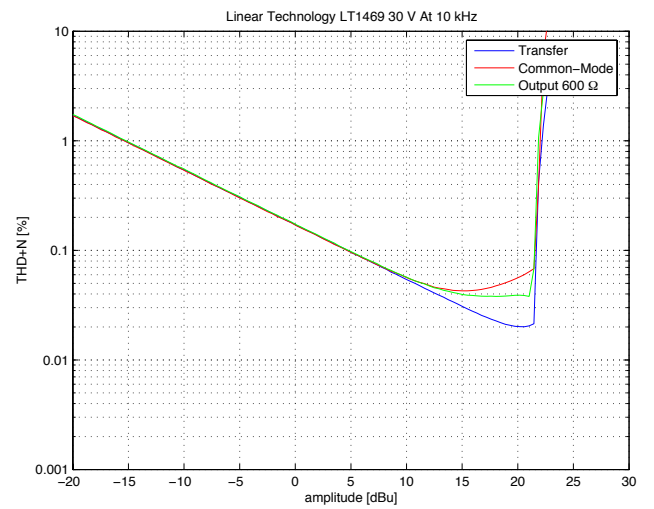
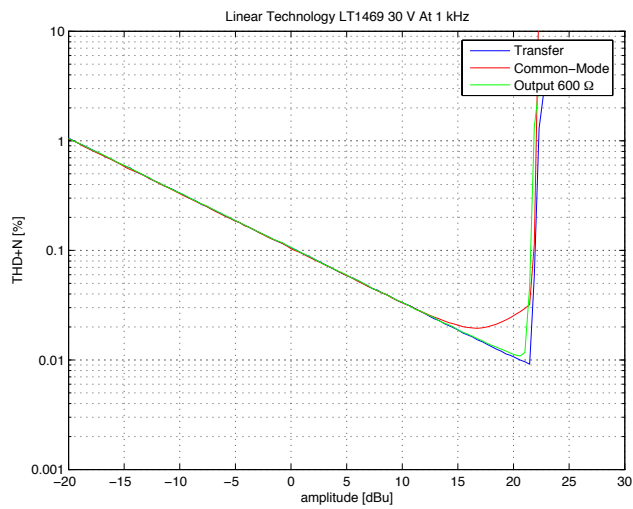
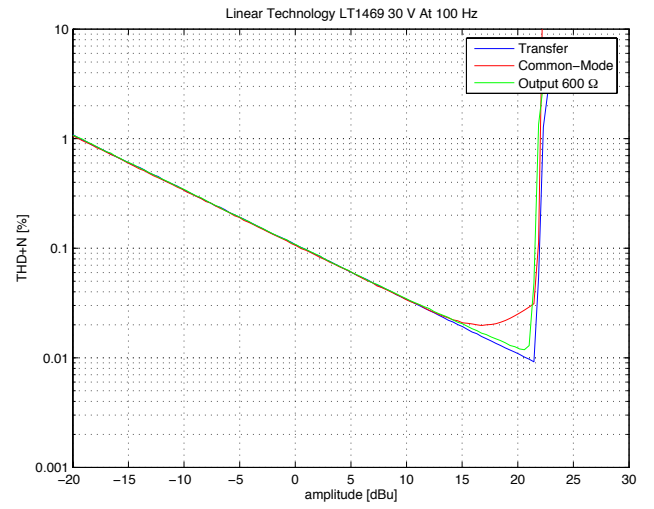
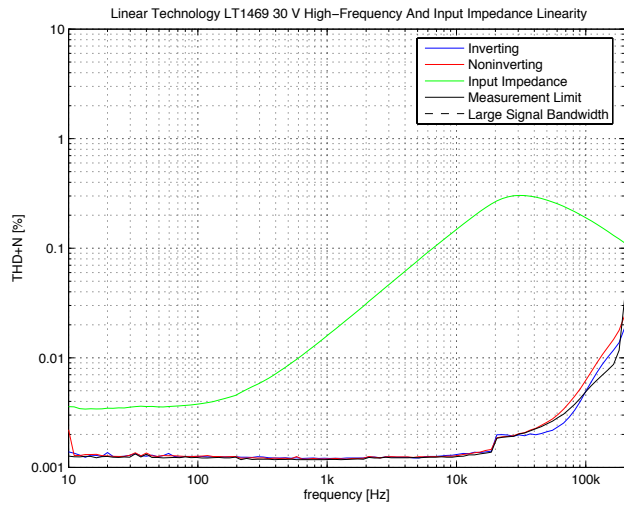
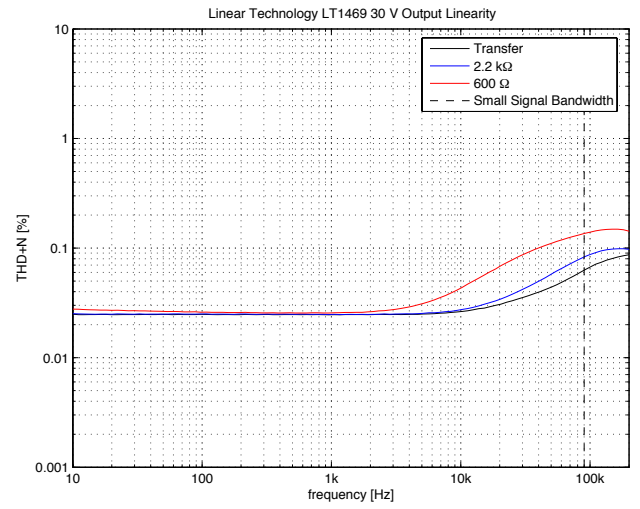
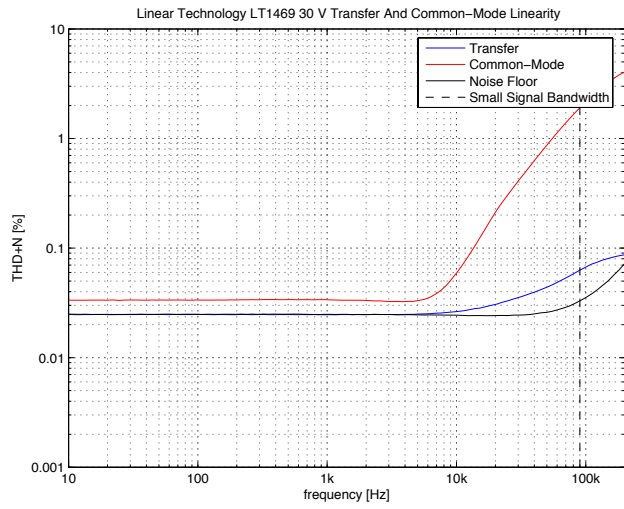
Table 3.14: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 15 \text{ V}$ .

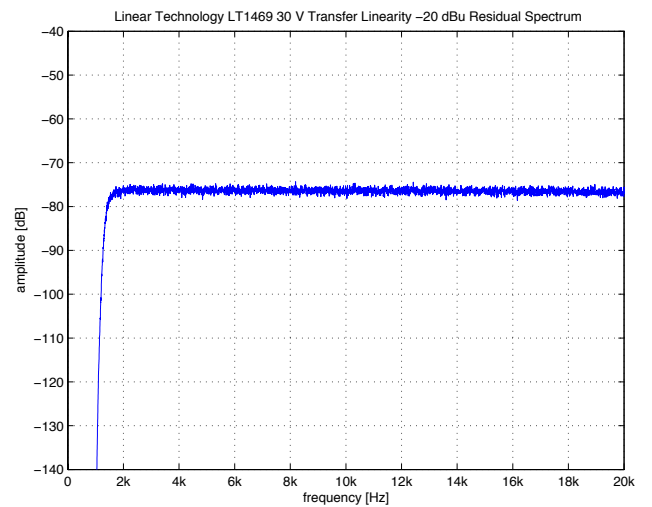
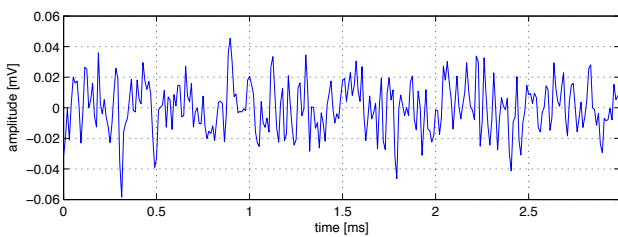
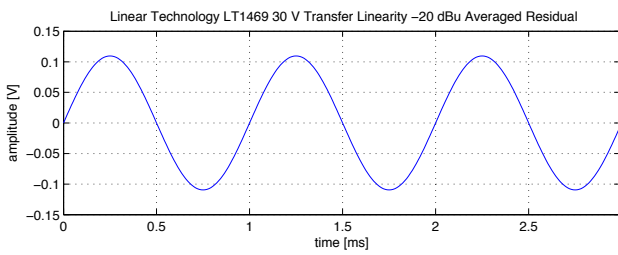
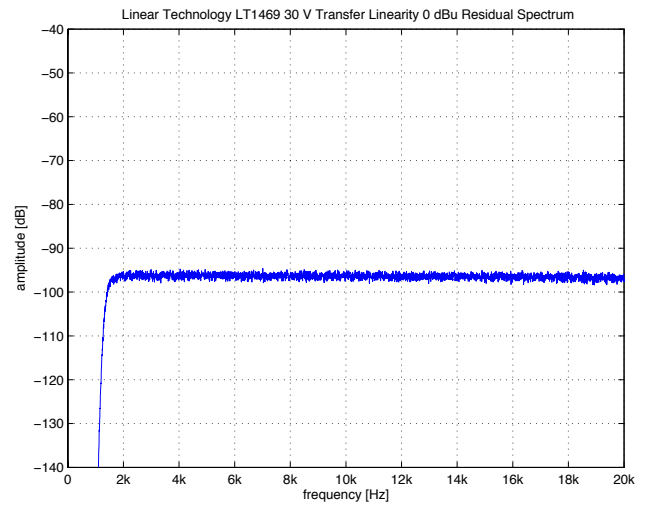
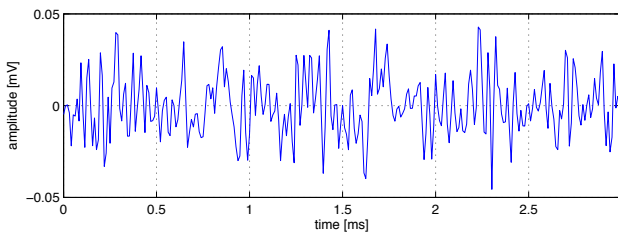
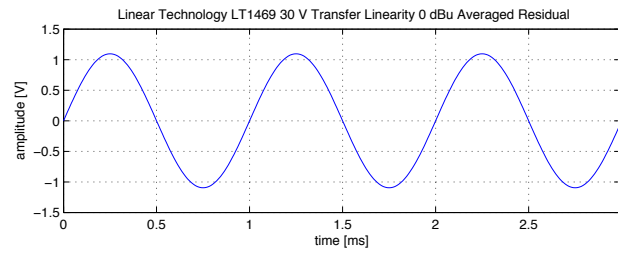
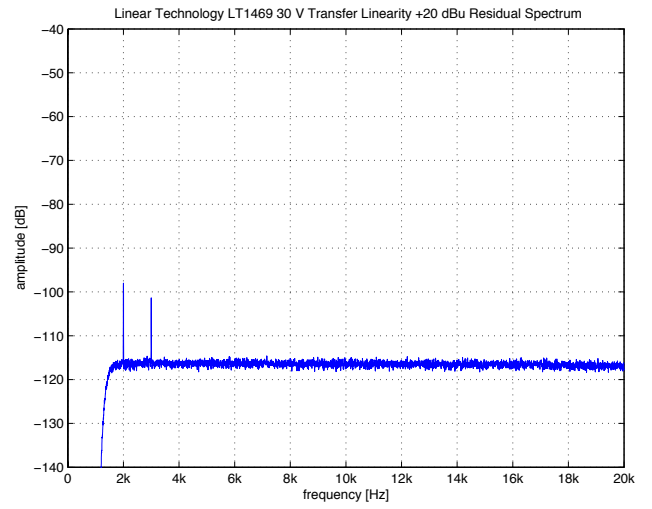
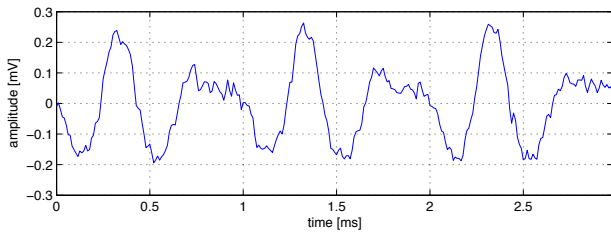
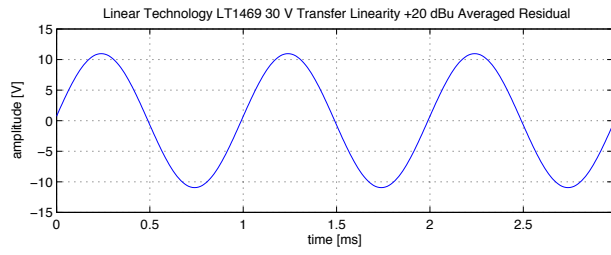
A dual amplifier using a single-stage folded cascode architecture with bootstrapped current mirror and BJT input [14]. Combines good DC precision with high slew-rate at low current noise; a single version is available (LT1468). As the voltage noise is only moderately low it achieves best noise figure at medium-low source impedances.

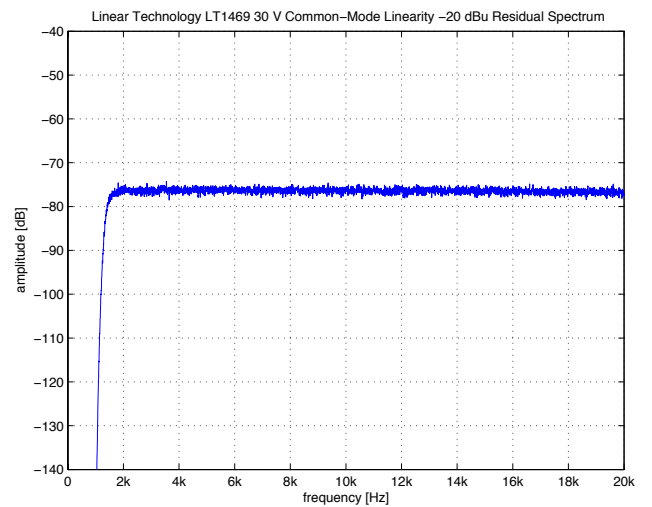
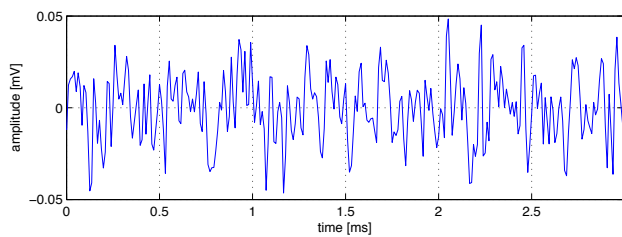
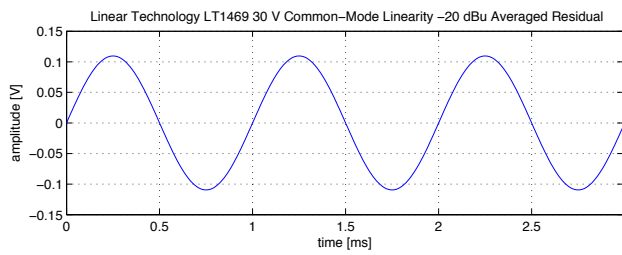
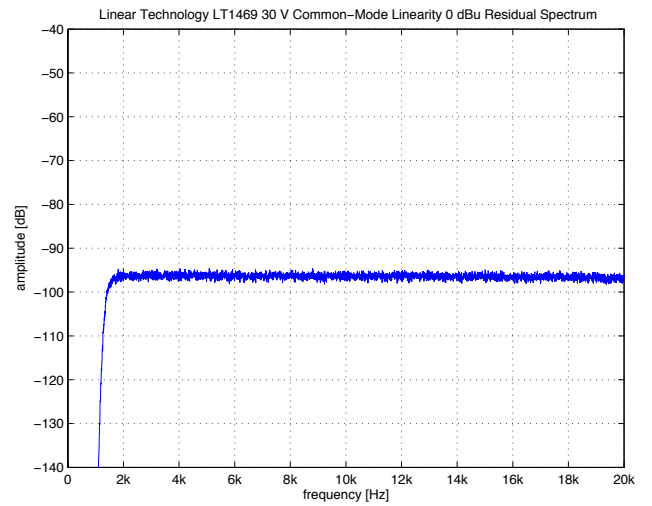
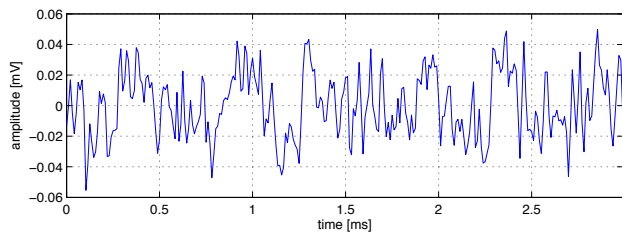
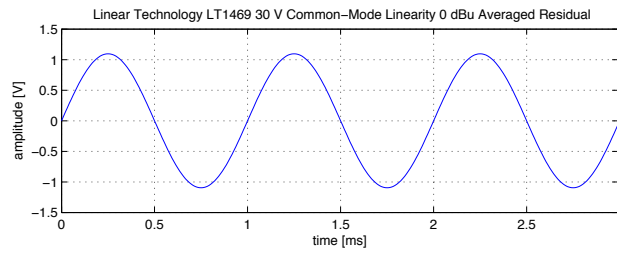
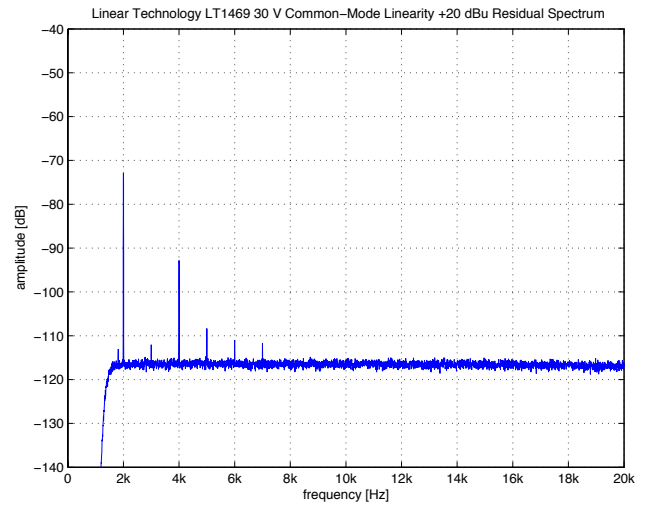
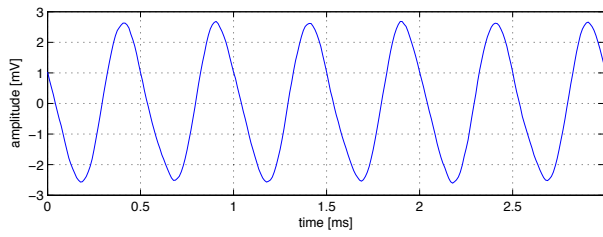
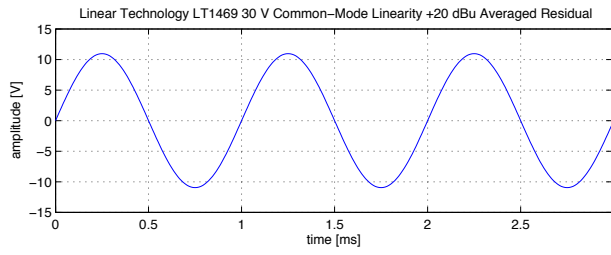
Transfer linearity is exceptionally good up to high frequencies. Common-mode distortion consists of two effects. First a relatively modest distortion which is independent of frequency and dominates at medium and low frequencies; second a for BJT inputs untypically rapidly rising contribution above about 6 kHz. Output loading effects are relatively benign at medium and low frequencies. Input impedance linearity is relatively poor, down to the lowest frequencies.

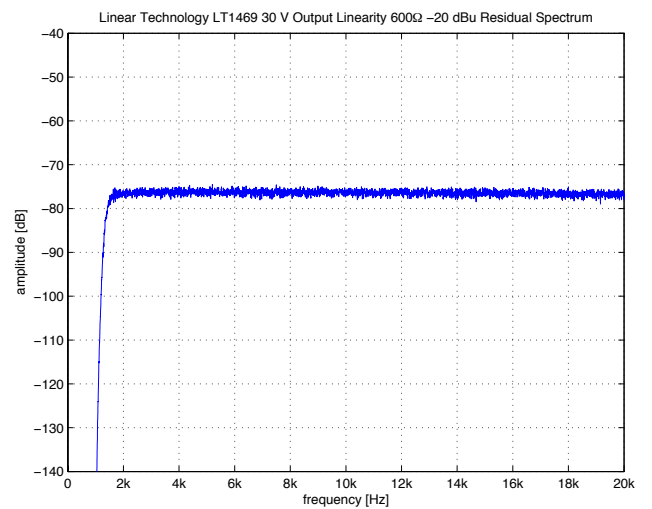
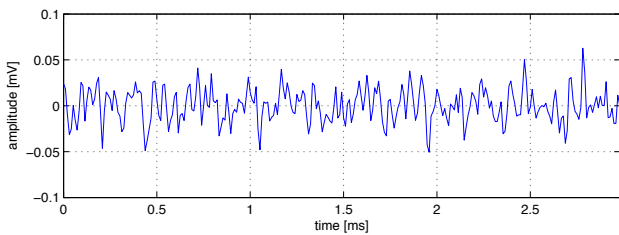
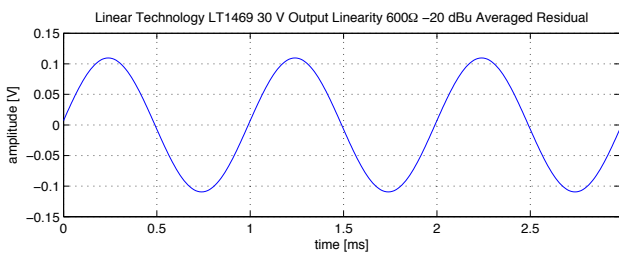
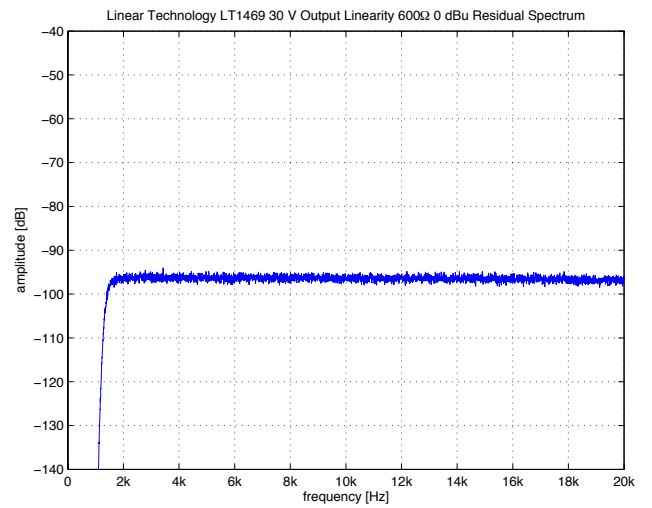
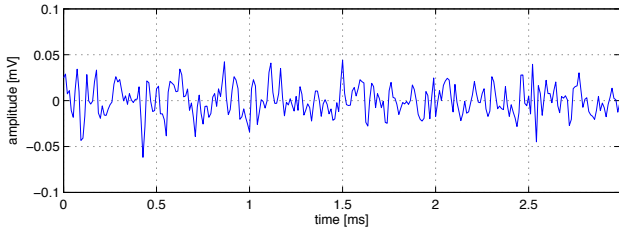
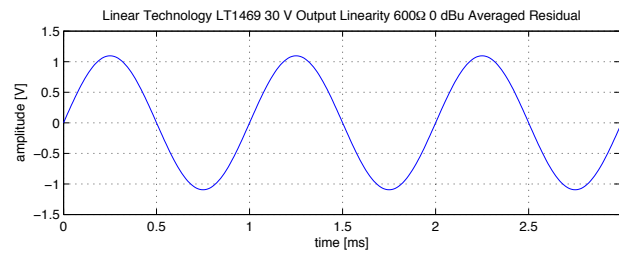
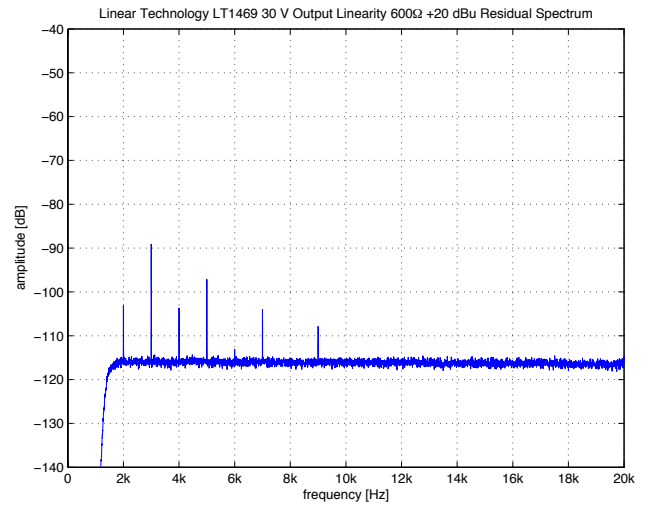
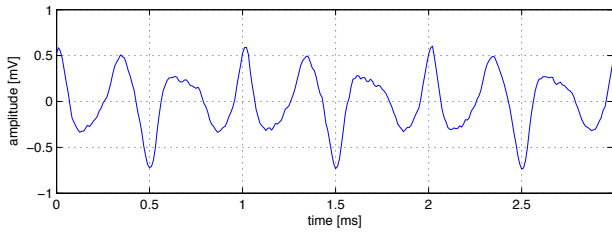
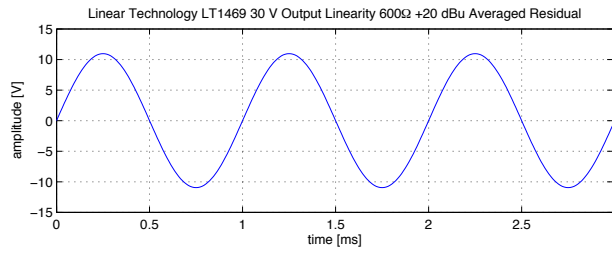
Offers good overall distortion figures at medium cost. For best performance some care to common-mode, input impedance and output loading effects must be given though. Appears to be an ideal upgrade for NE5532 amplifiers as its noise performance and quiescent current are similar. Note the lower maximum supply voltage of the LT1469 though.











### 3.15 Linear Technology LT1630

<b>Number of Channels</b>	2
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	1.48 US\$ at 1k units (August 2008)

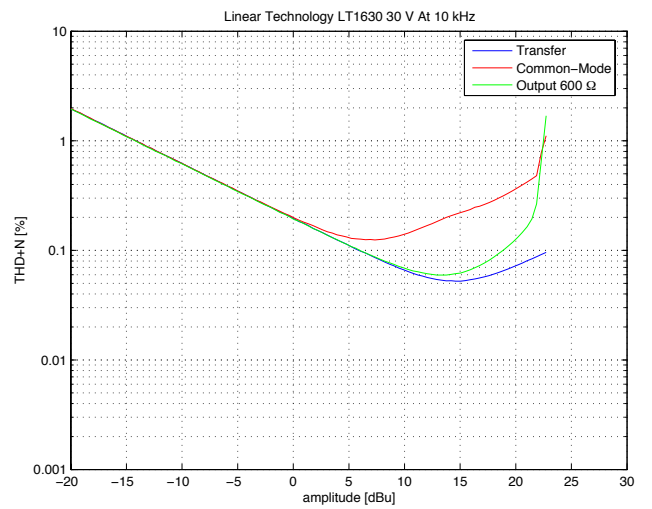
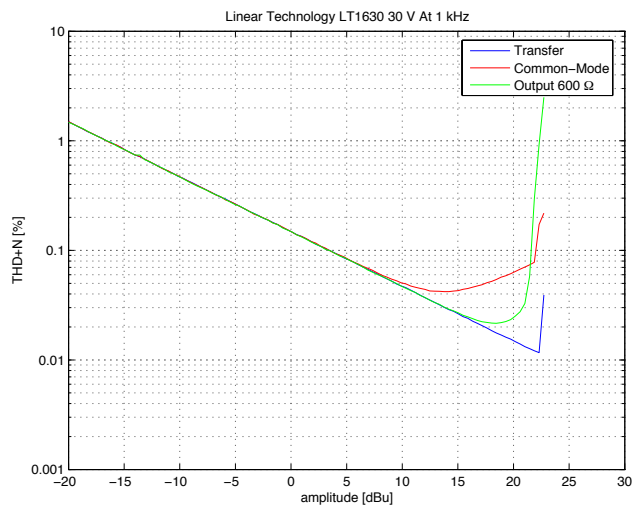
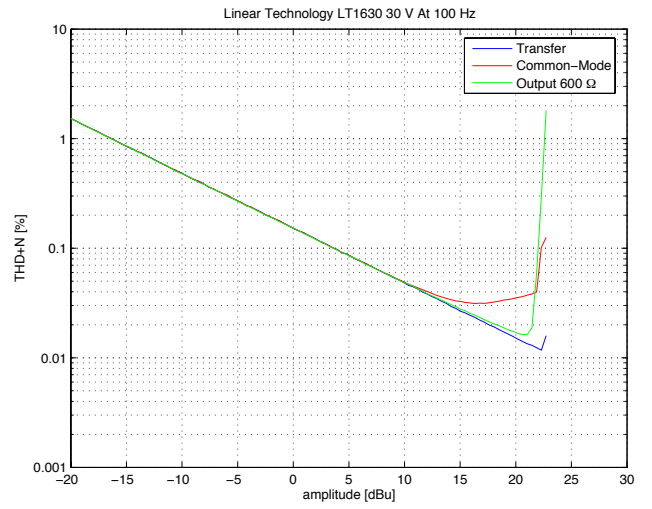
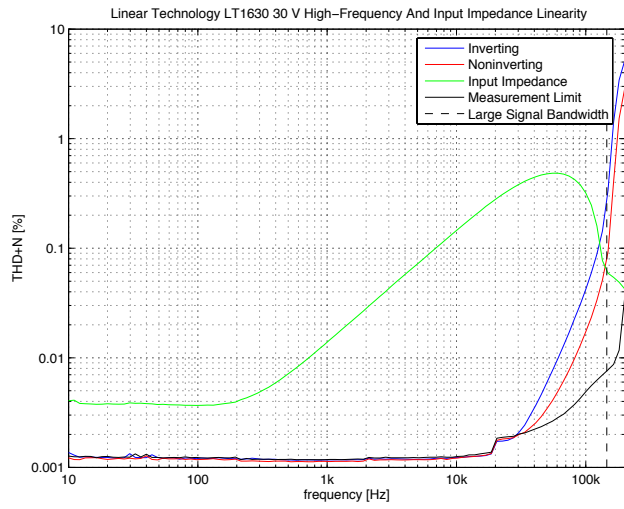
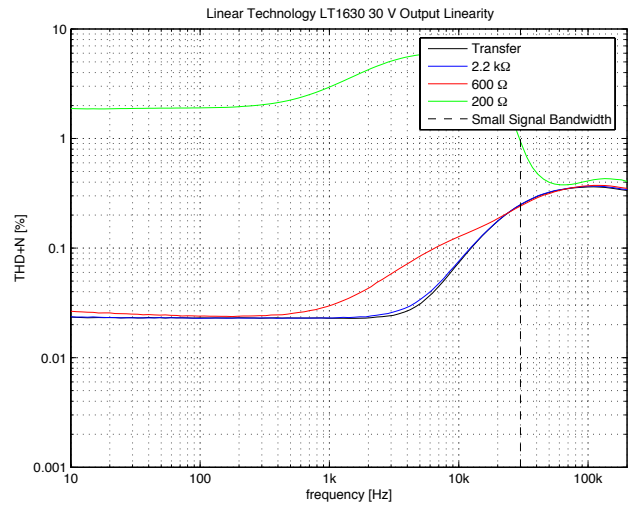
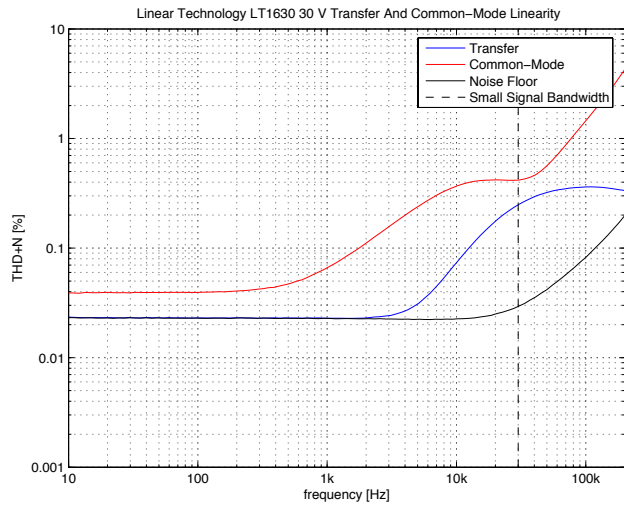
Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		220	1000	$\mu\text{V}$
Input Bias Current		550	1100	nA
Input Offset Current		20	150	nA
Gain Bandwidth Product	15	30		MHz
Slew-Rate	5	10		$\text{V}/\mu\text{S}$
Input Voltage Noise (f = 1 kHz)		6		$\text{nV}/\sqrt{\text{Hz}}$
Input Current Noise (f = 1 kHz)		0.9		$\text{pA}/\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 15$			V
Output Voltage Swing ( $I_{\text{OUT}} = 5 \text{ mA}$ )	+14.5/-14.7	+14.75/-14.85		V
Output Voltage Swing ( $I_{\text{OUT}} = 25 \text{ mA}$ )	+13.8/-14.4	+12.6/-13.8		V
Output Current	$\pm 35$	$\pm 70$		mA
Power Supply Voltage	$\pm 1.35$		$\pm 18$	V
Quiescent Current per Amplifier		4.1	5	mA

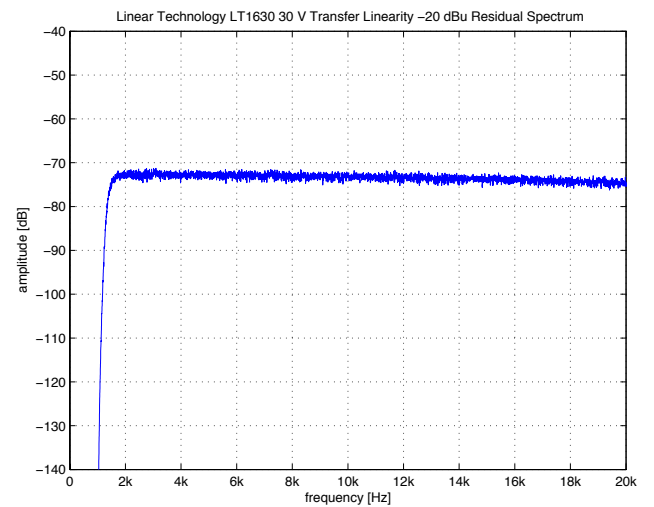
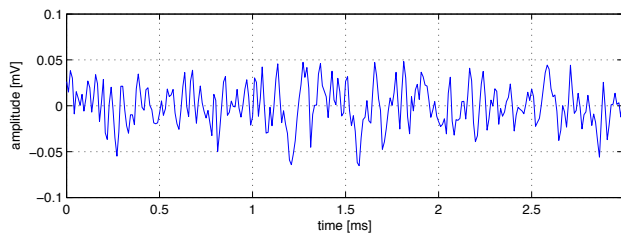
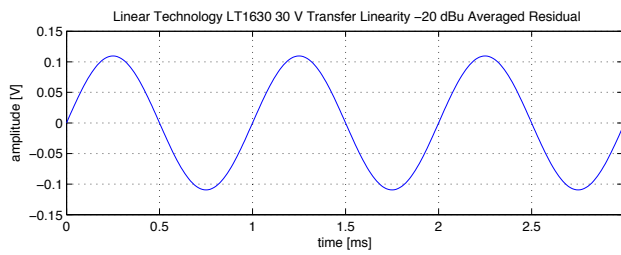
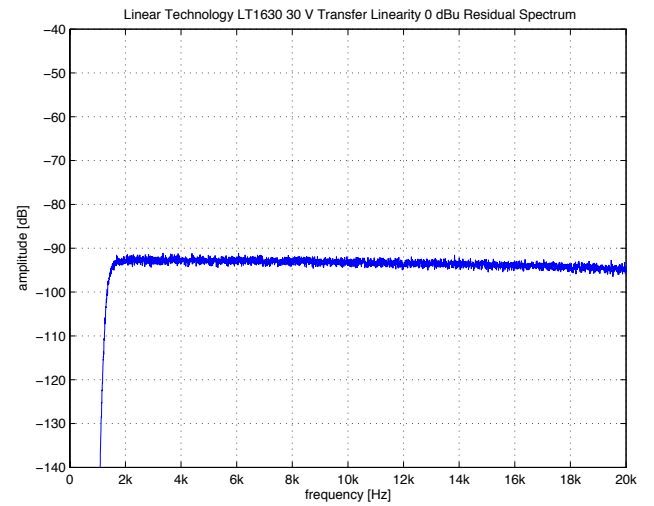
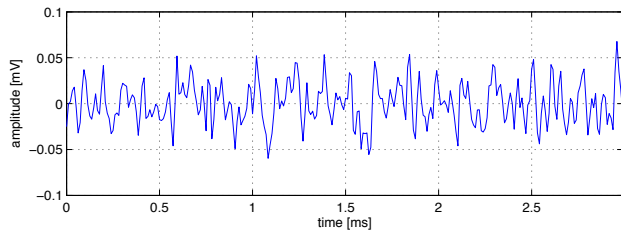
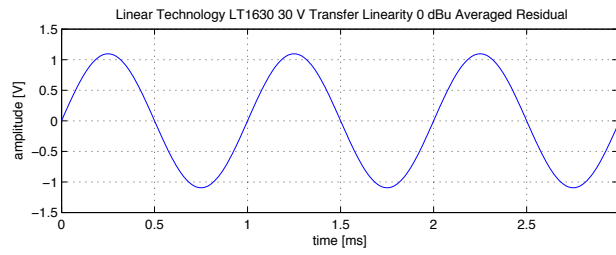
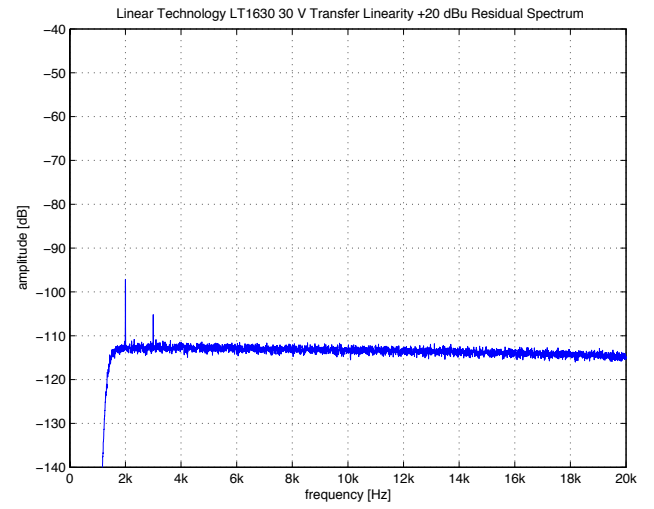
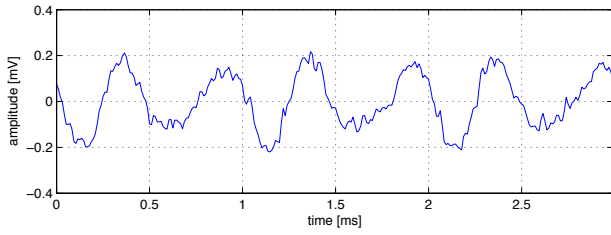
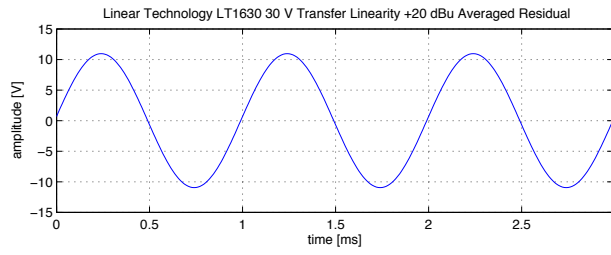
Table 3.15: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 15 \text{ V}$ .

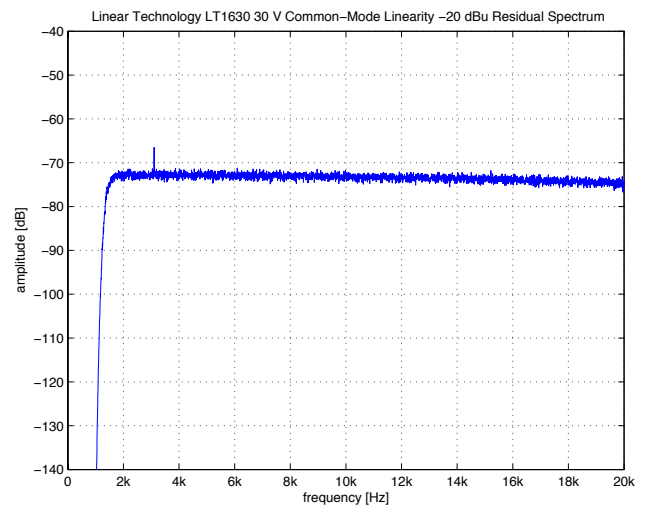
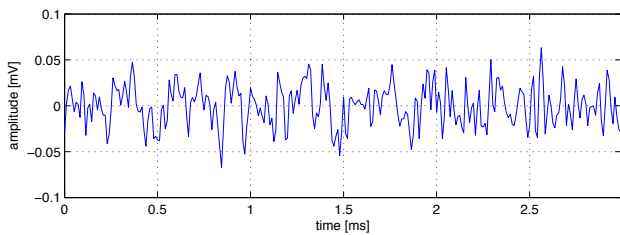
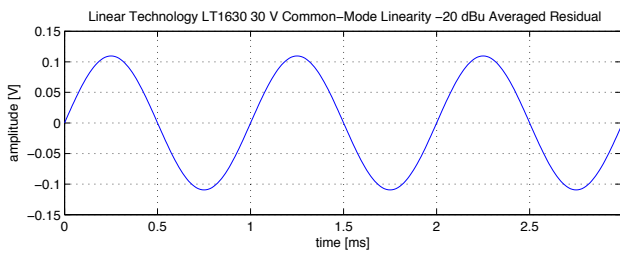
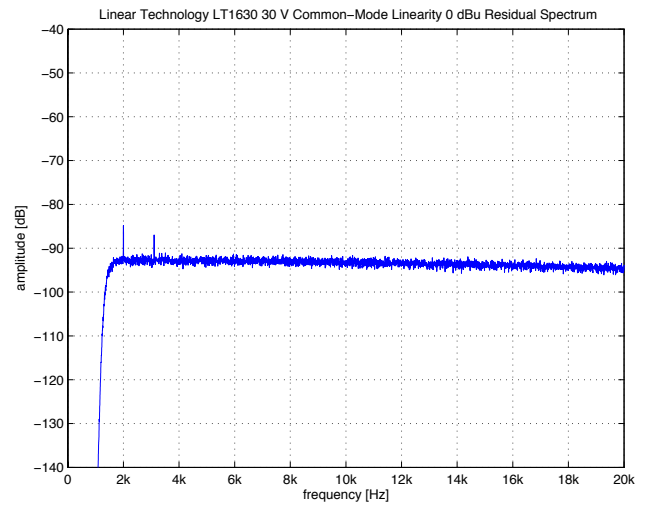
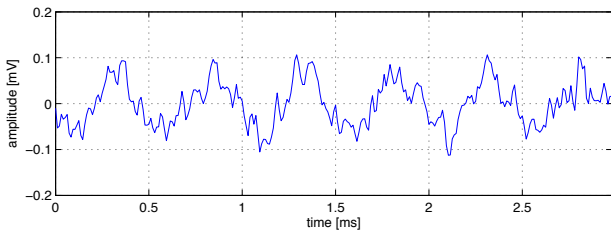
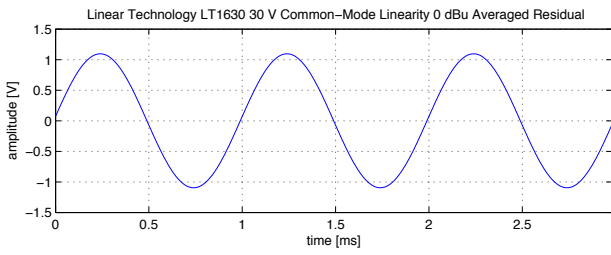
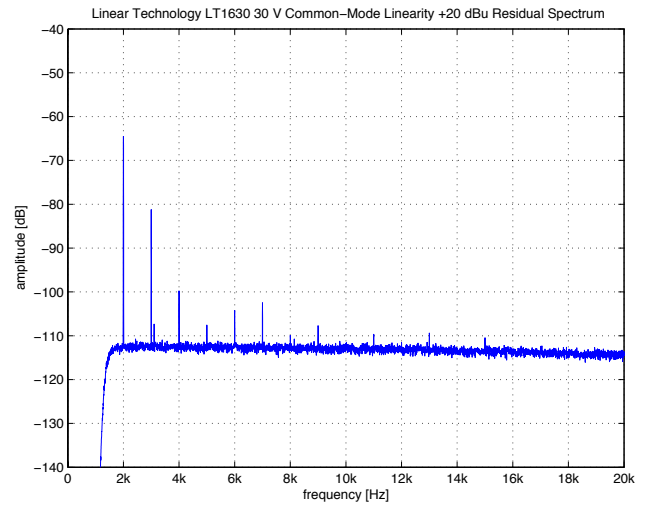
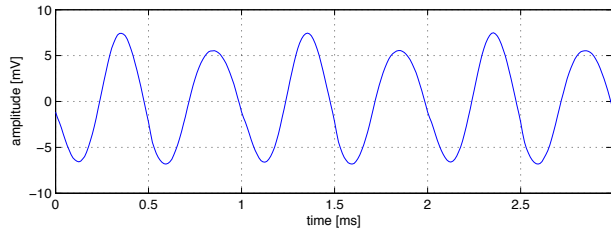
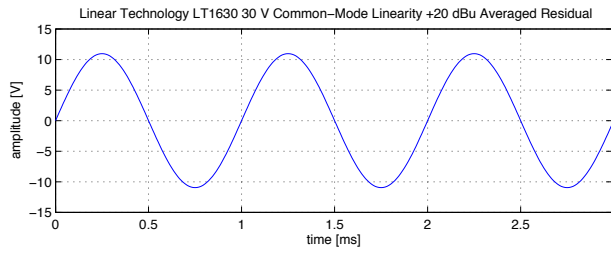
A bipolar operational amplifier with a complementary folded cascode topology; both input and output stage are designed for rail-to-rail operation. Dedication for low voltage applications is further stressed by the support of very low supply rail voltages. Noise performance is not superbe, but at medium impedances acceptable performance will be realised.

The transfer linearity is very good at a few kHz and below; due to the only medium high slew-rate high-frequency distortion is clearly present. Common-mode and input impedance linearity performance is not particularly good, but at least better than for other parts. Although this amplifier uses a collector output stage to obtain rail-to-rail voltage swing output load-line distortion is surprisingly well controlled. Thermal effects are just visible at  $600 \Omega$  loading. Note that there is some interference at 3 kHz visible in the common-mode linearity FFT plots.

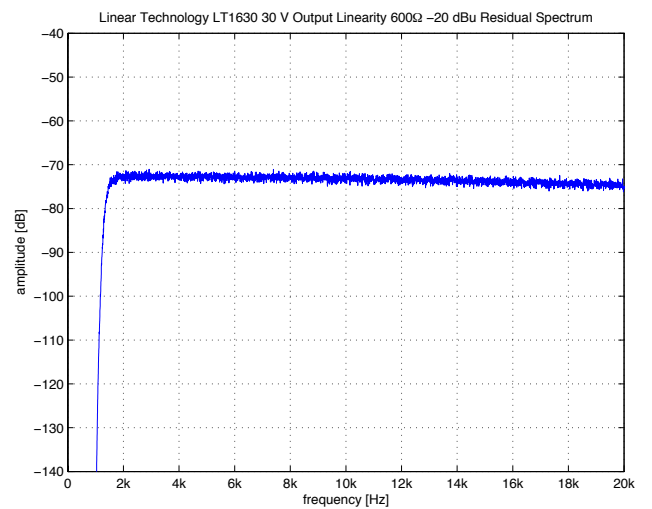
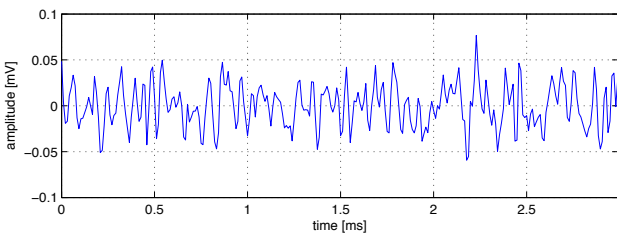
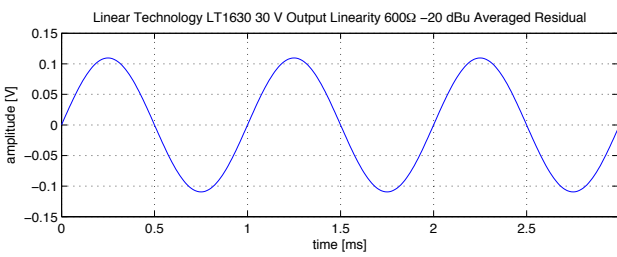
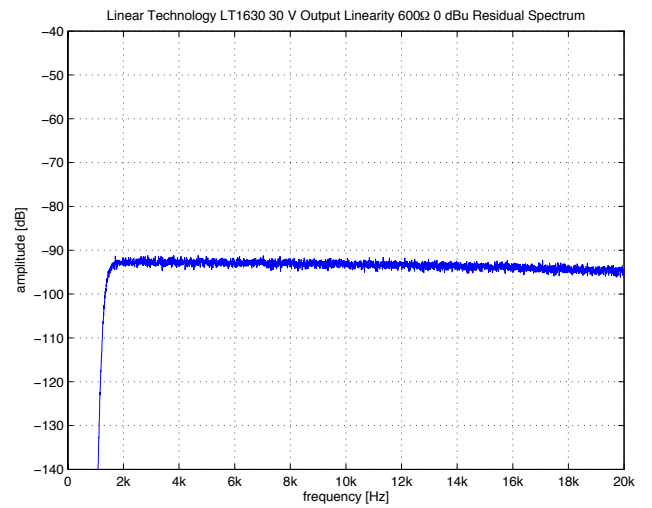
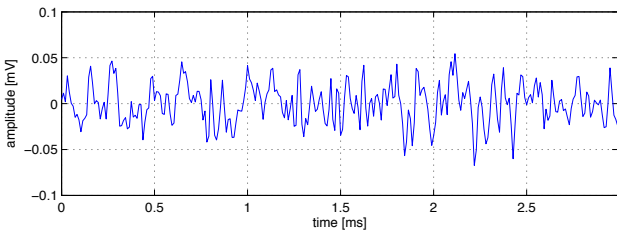
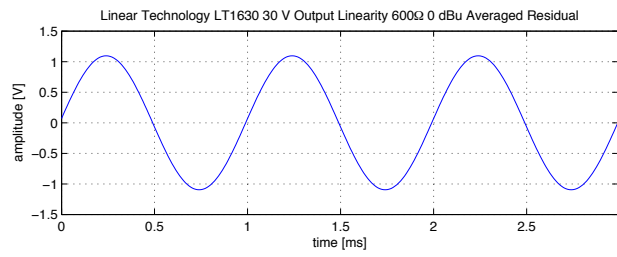
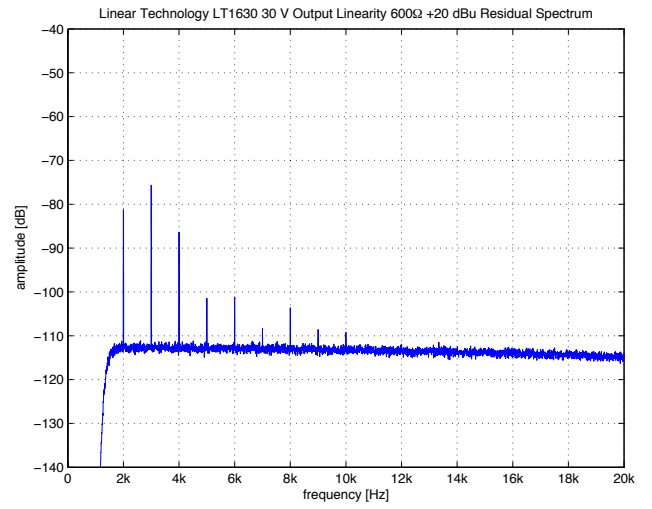
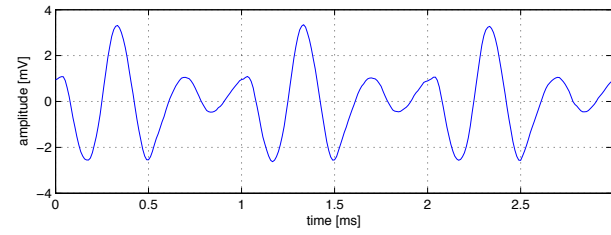
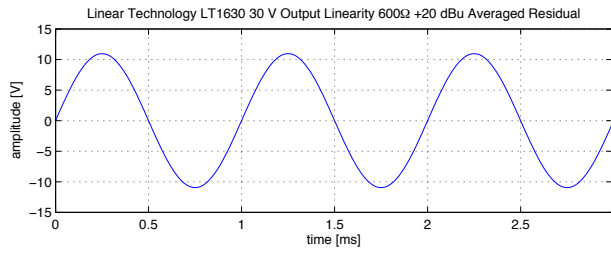
Definitely a part to consider where compliance with low supply voltages and/or rail-to-rail performance is needed; at low supply voltages the limited slew-rate will be less of a problem as output voltage swings will be much lower. Common-mode effects will however need special consideration for lowest distortion. For given performance reasonably priced.











### 3.16 National Semiconductor LME49860

<b>Number of Channels</b>	2
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	1.05 US\$ at 100 units (July 2008)

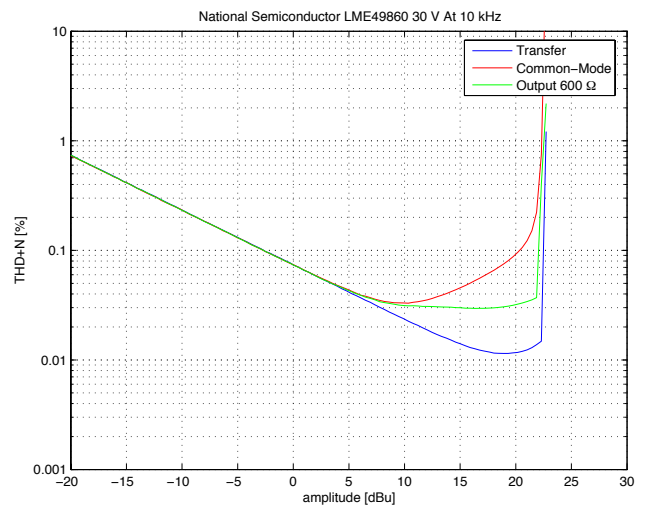
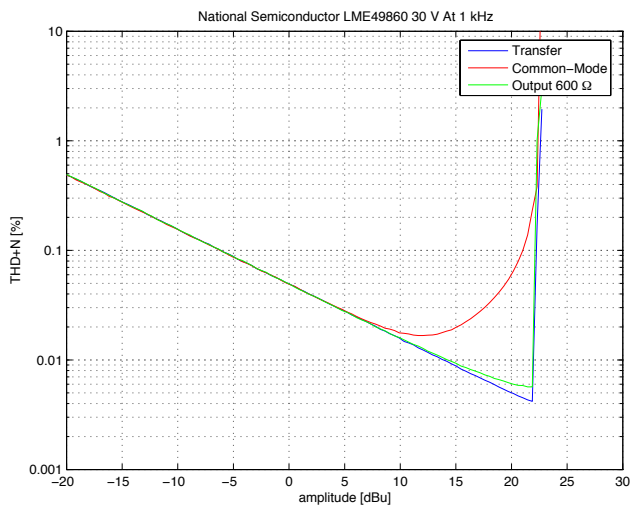
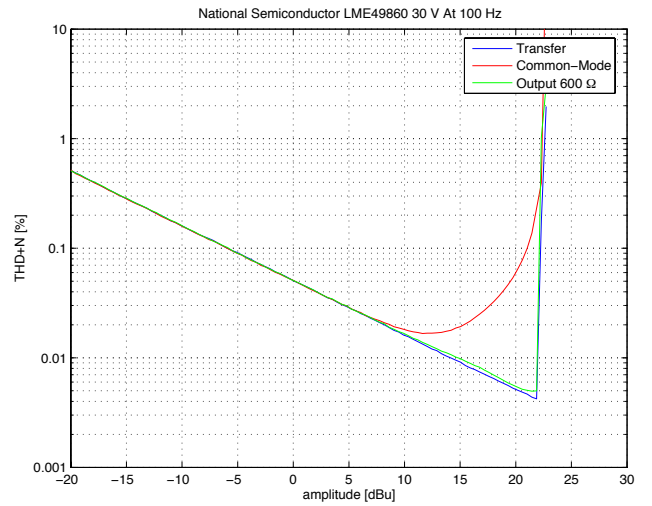
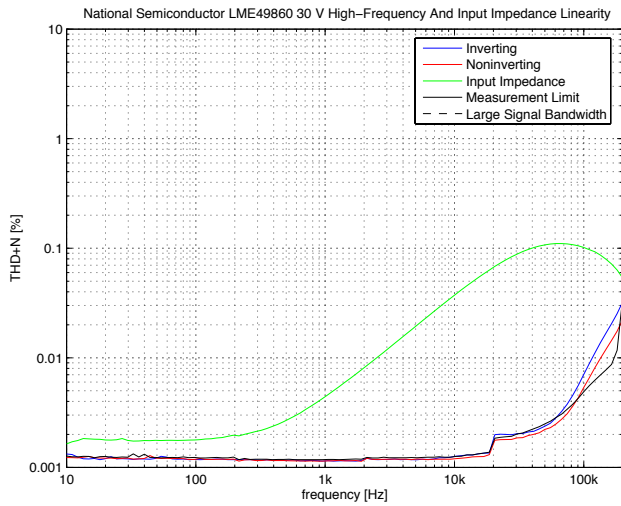
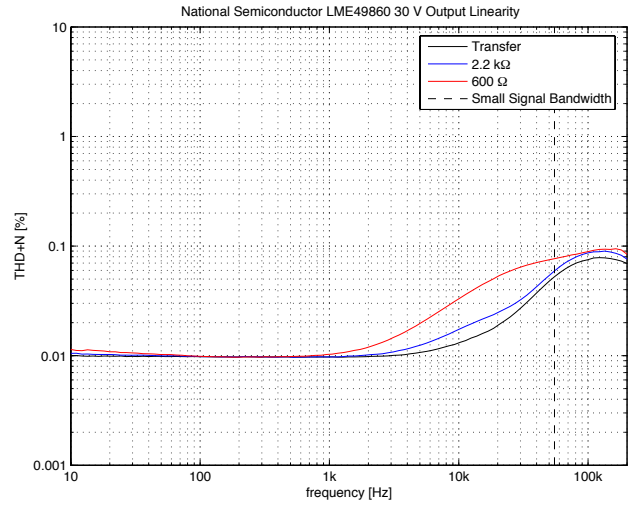
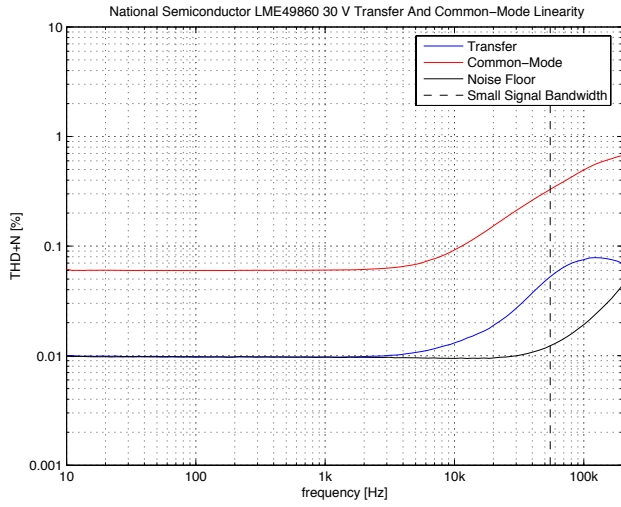
Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		0.12	0.70	mV
Input Bias Current		10	72	nA
Input Offset Current		11	65	nA
Gain Bandwidth Product	45	55		MHz
Slew-Rate	15	20		V/ $\mu$ S
Input Voltage Noise (f = 1 kHz)		2.7	4.7	nV/ $\sqrt{\text{Hz}}$
Input Current Noise (f = 1 kHz)		1.6		pA/ $\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 16$	+17.1/-16.9		V
Output Voltage Swing ( $R_L = 2 \text{ k}\Omega$ )		$\pm 17$		V
Output Voltage Swing ( $R_L = 600 \Omega$ )		$\pm 16.7$		V
Output Current		$\pm 31$		mA
Power Supply Voltage	$\pm 2.5$		$\pm 22$	V
Quiescent Current per Amplifier		5.1		mA

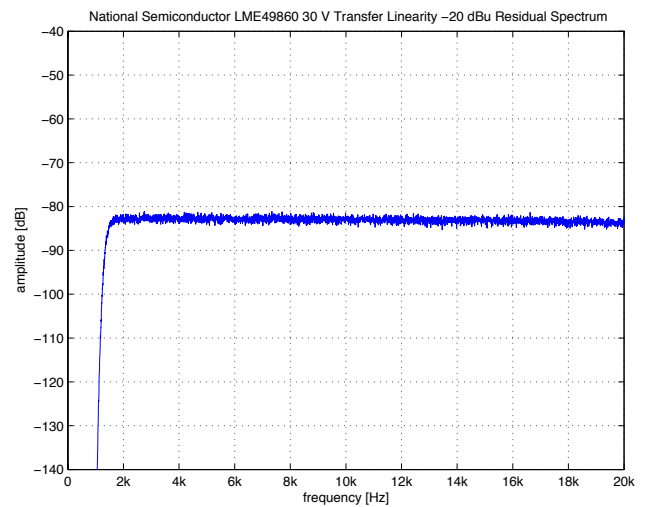
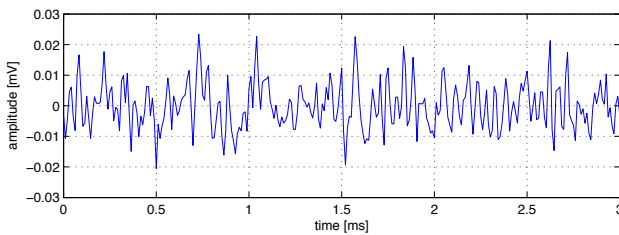
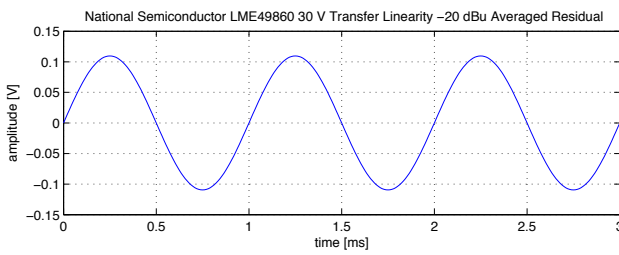
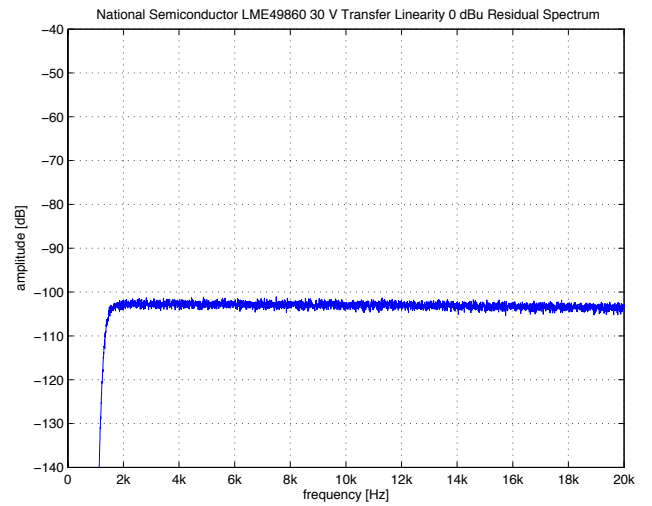
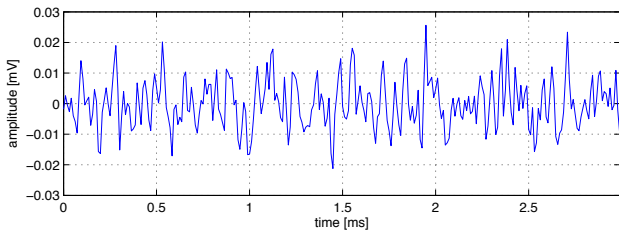
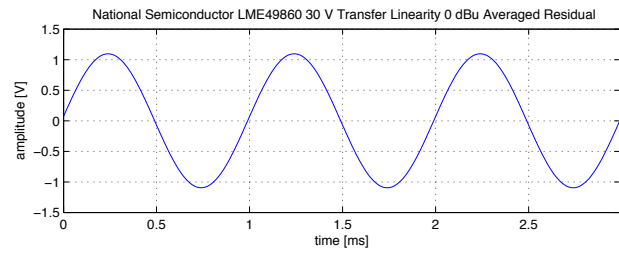
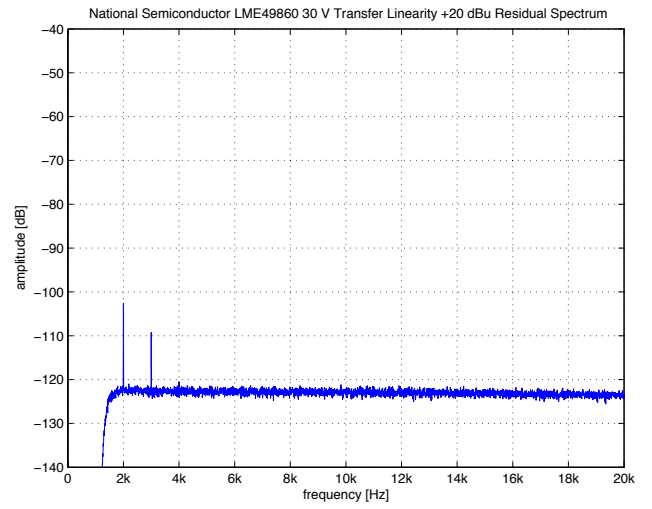
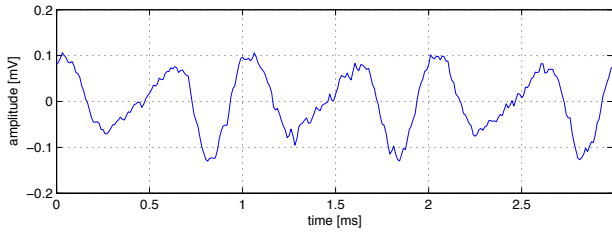
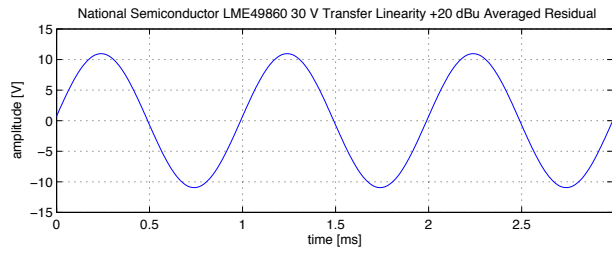
Table 3.16: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 18 \text{ V}$ .

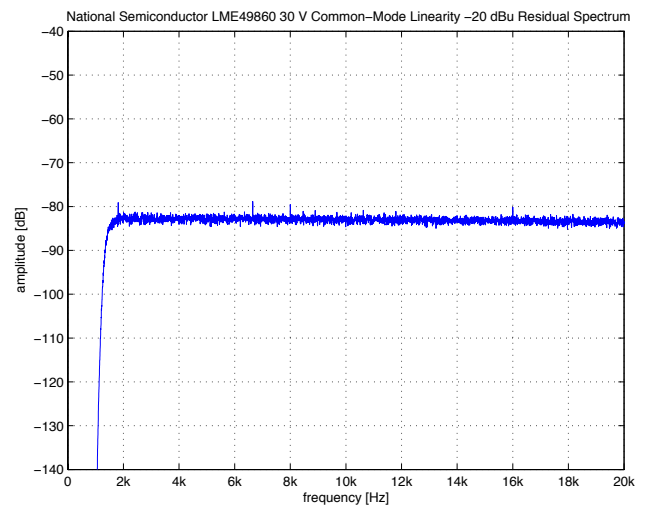
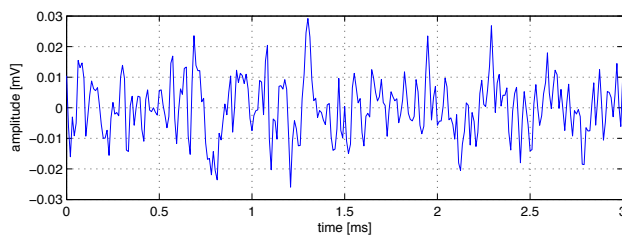
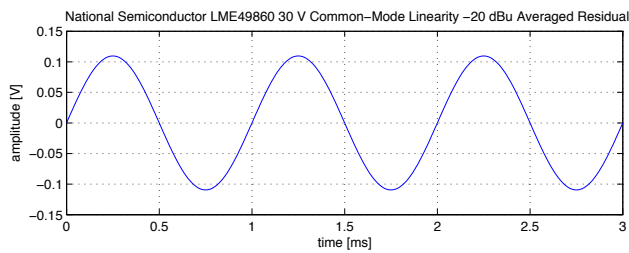
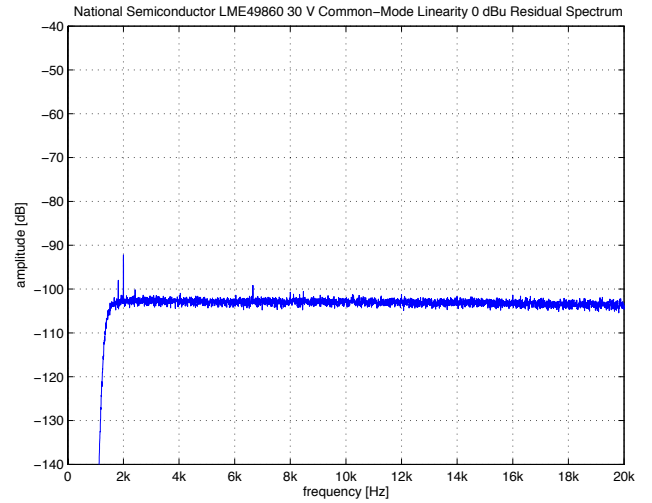
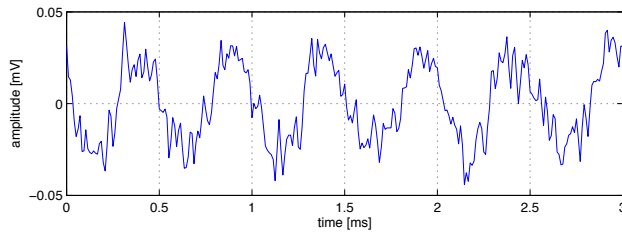
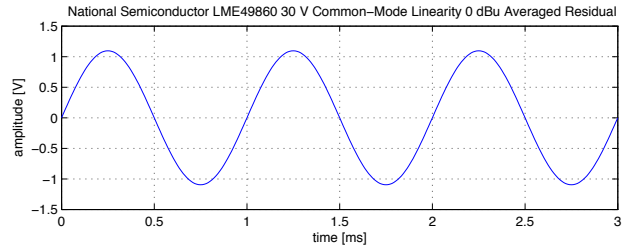
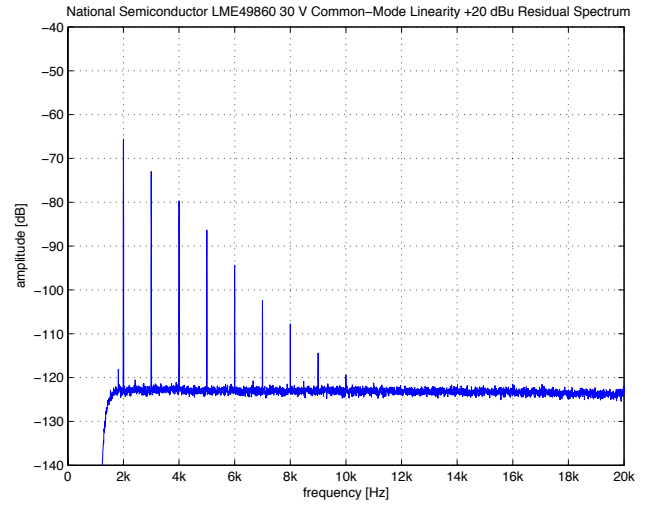
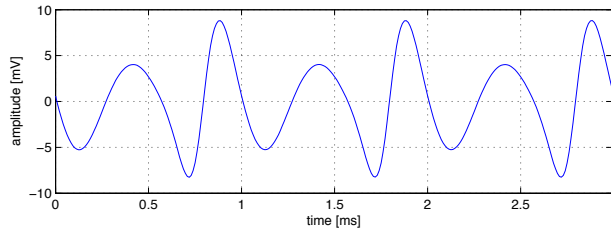
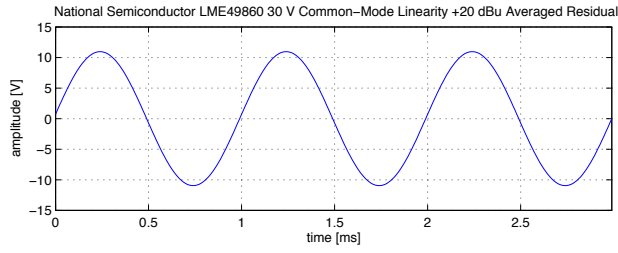
A dual opamp designed for audio use which offers a very wide power supply range. No internal circuit details are known except the use of a BJT input. The current noise density is relatively high considering the medium-low voltage noise figure, suggesting the presence of an emitter degenerated input stage running at high tail current.

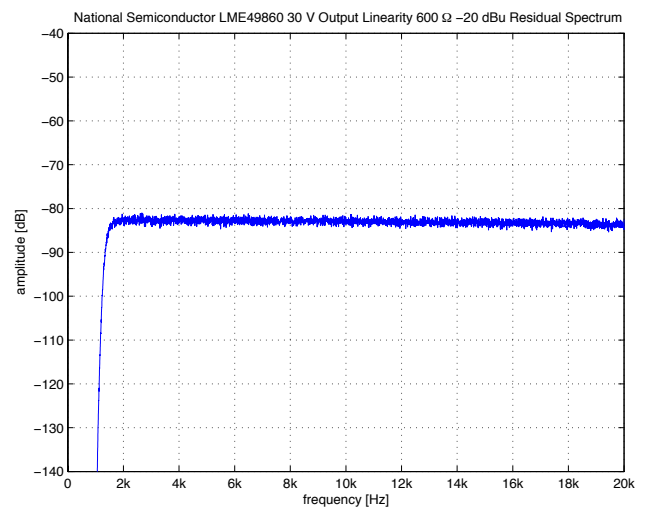
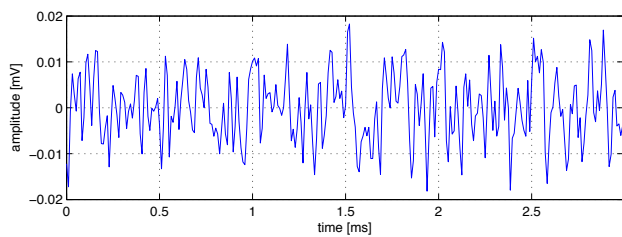
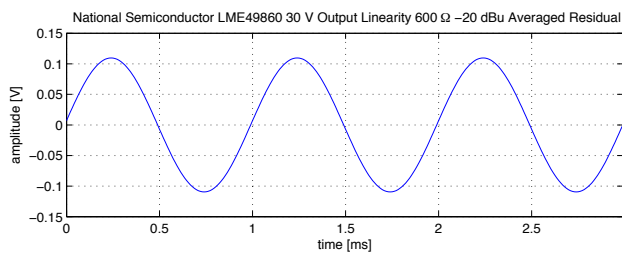
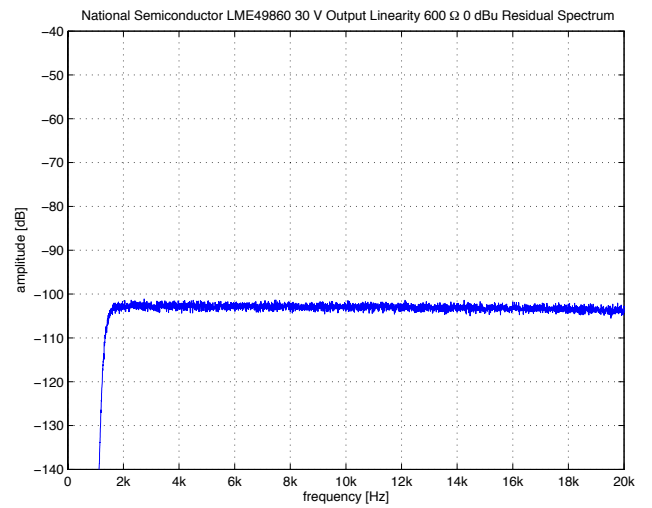
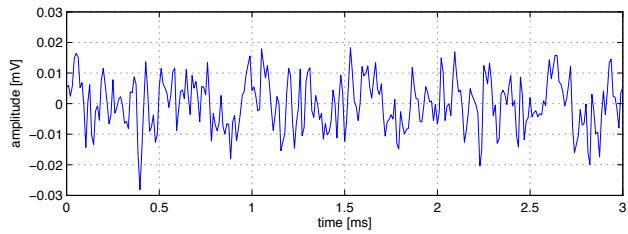
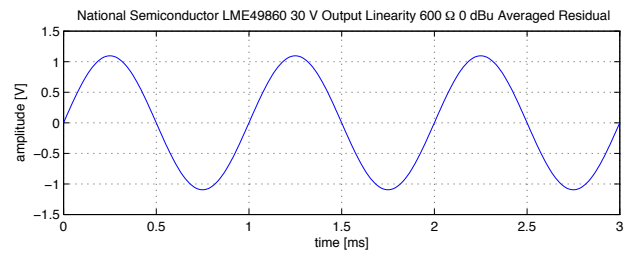
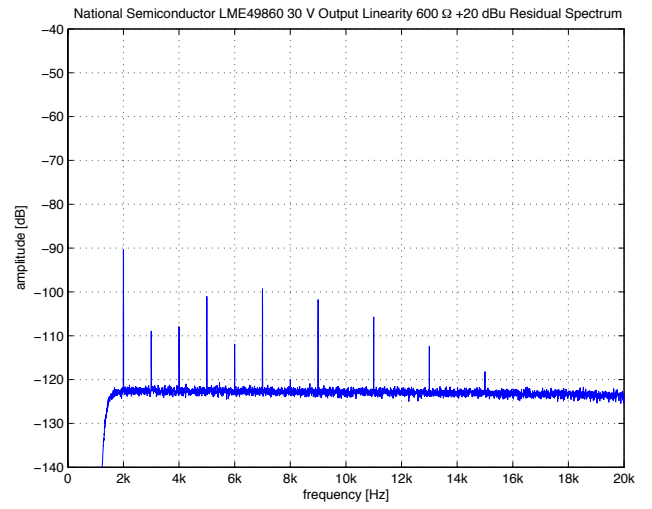
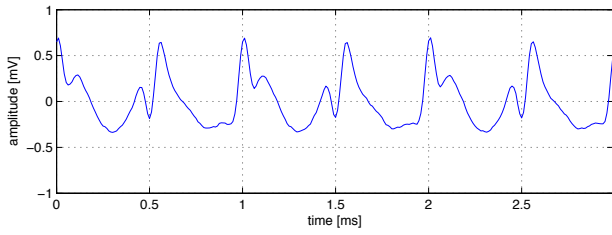
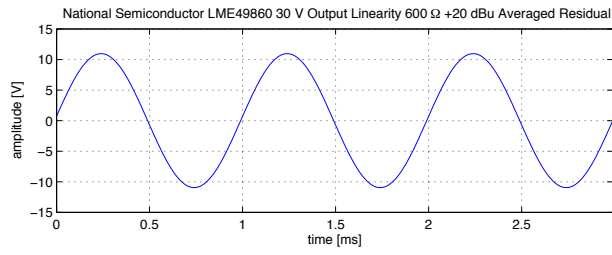
The basic transfer linearity is exceptionally good. Unfortunately the present heavy common-mode distortion degrades distortion performance by about one to two orders of magnitude at +20 dBu. This effect is greatly reduced for higher supply voltages and lower frequencies, but there remains high-frequency distortion which shows little reduction. Thermal effects are clearly visible at higher supply voltages, otherwise output loading distortion is relatively well controlled except at the upper end of the audio frequency range. The input impedance is relatively linear, especially at higher supply voltages.

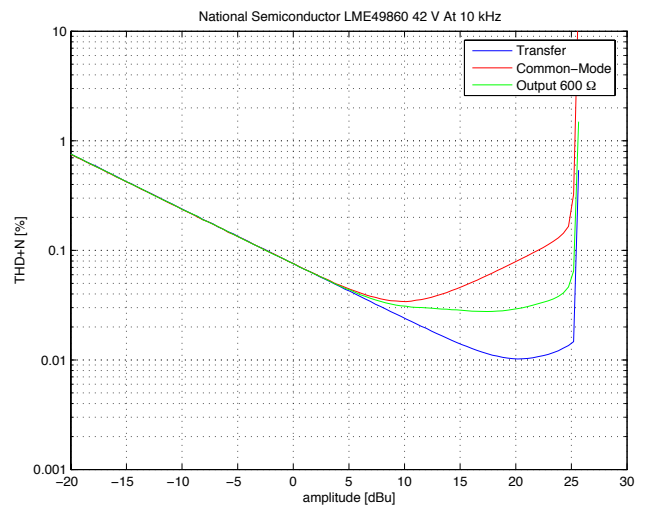
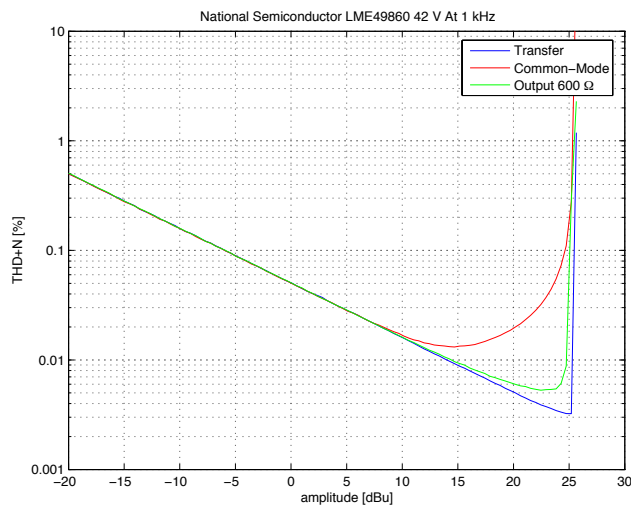
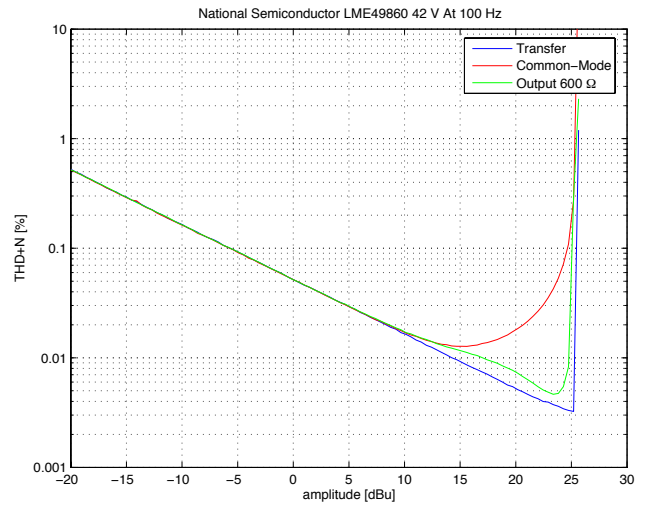
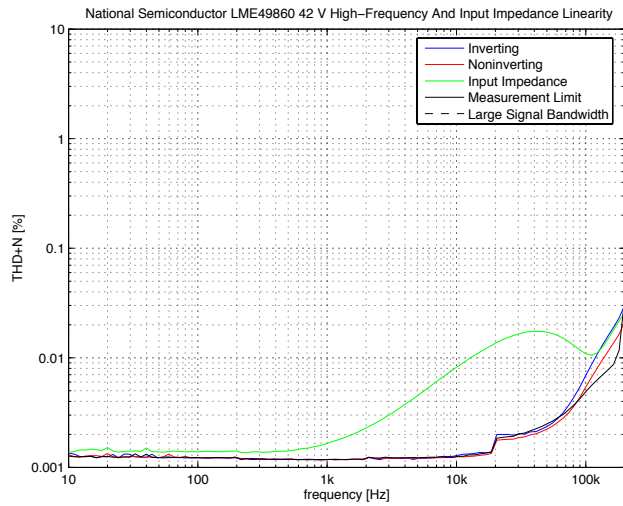
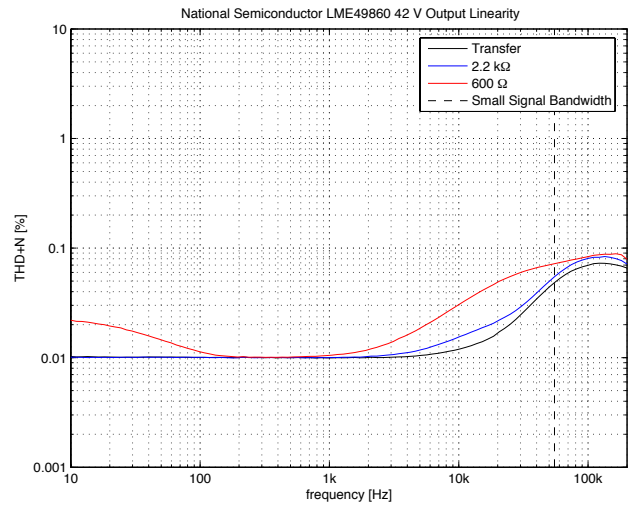
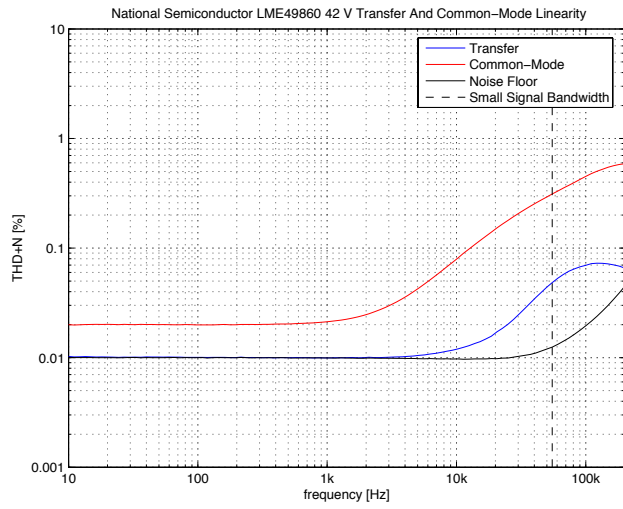
Good all-round low distortion opamp which needs careful attention to common-mode effects. For the given performance rather low cost. Can upgrade NE5532 amplifiers where the higher quiescent current and current noise is no issue.

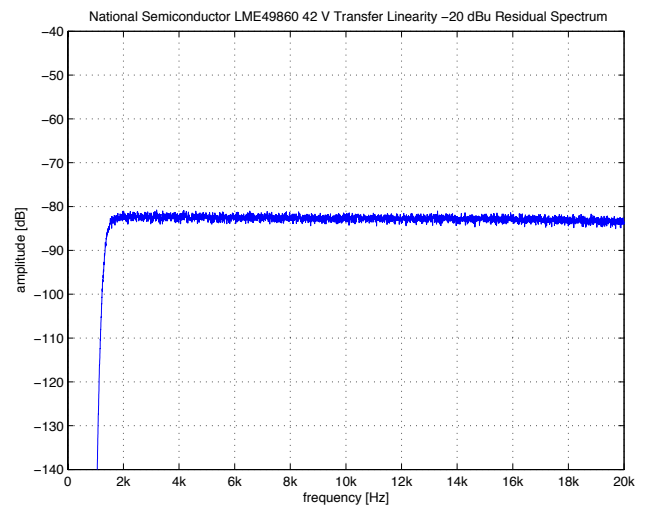
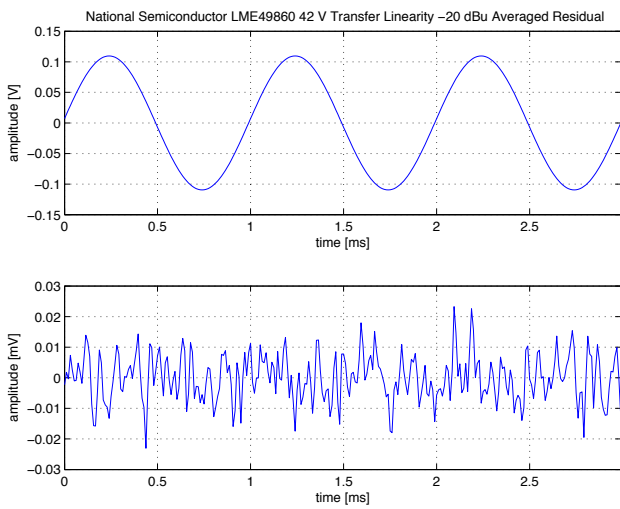
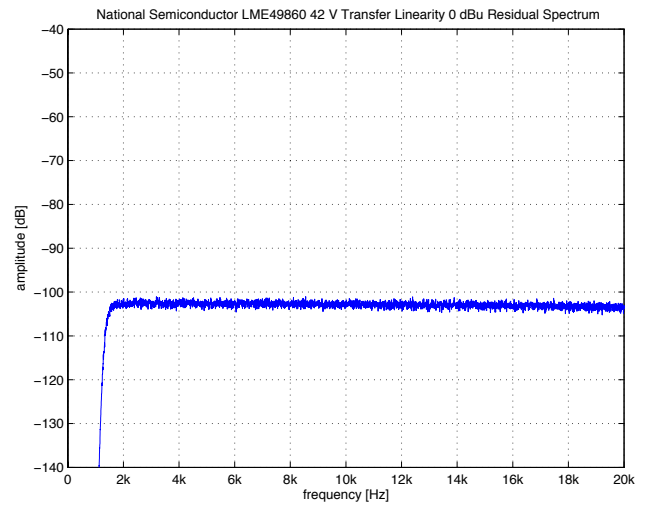
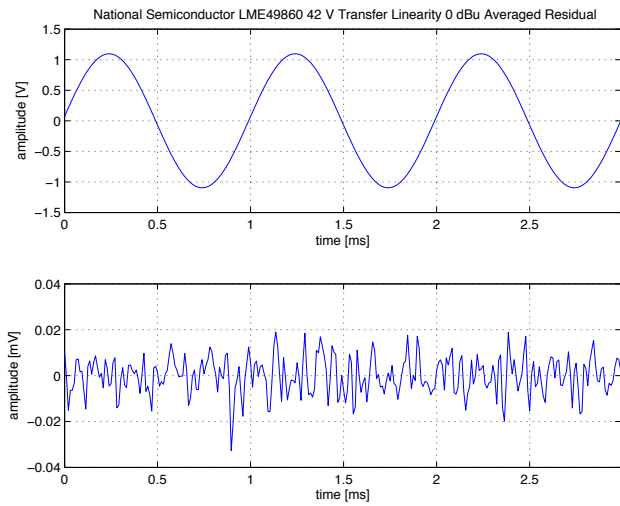
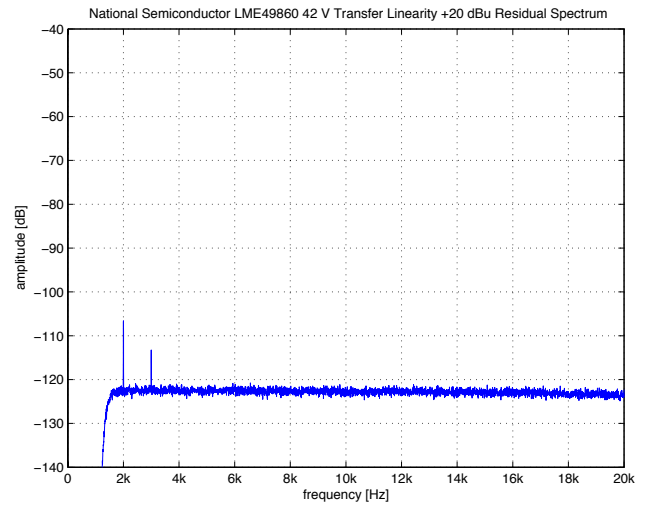
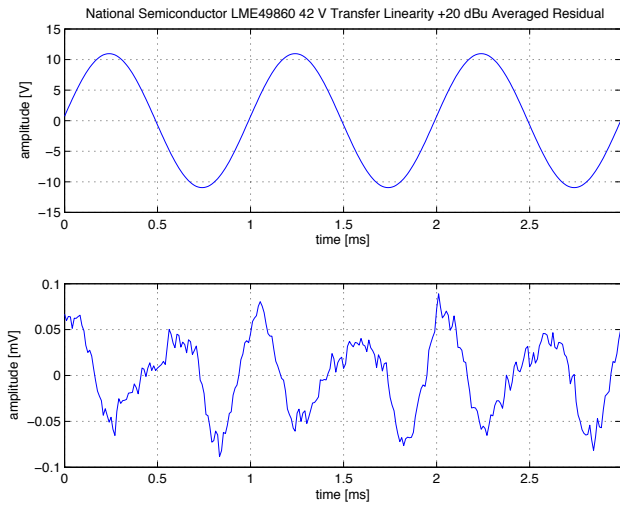




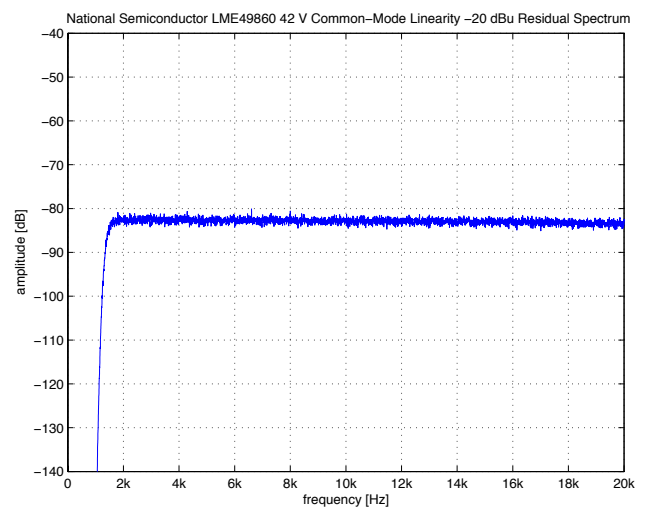
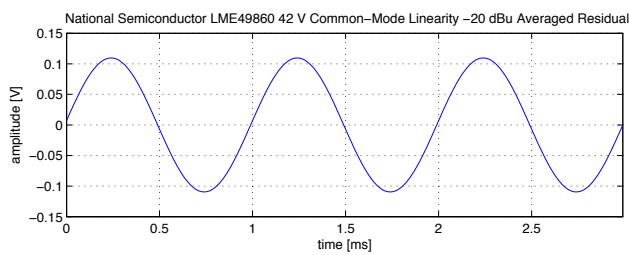
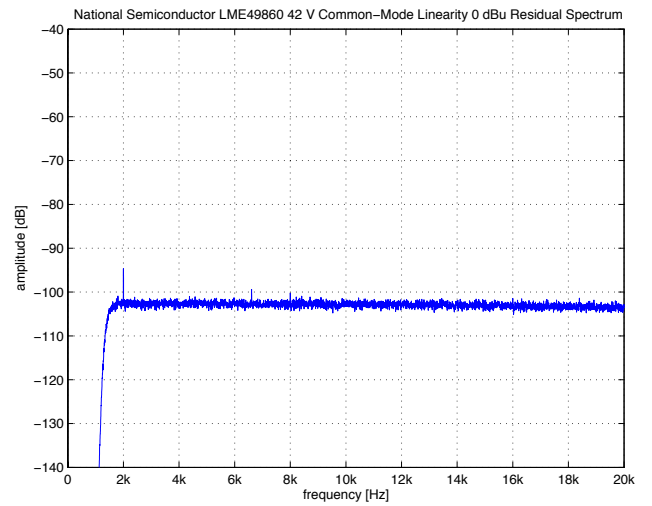
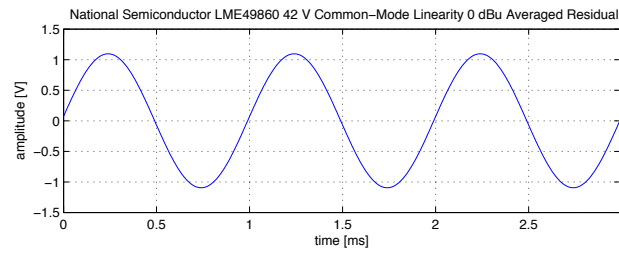
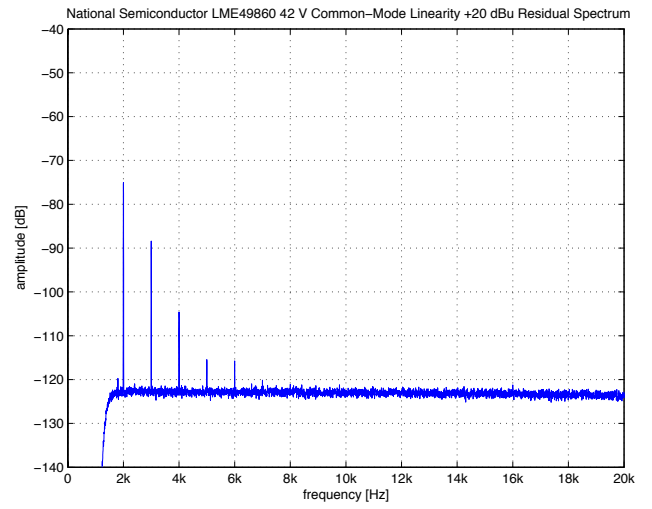
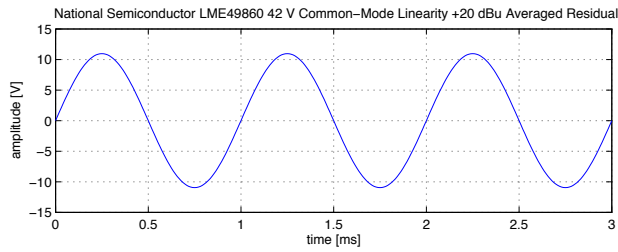


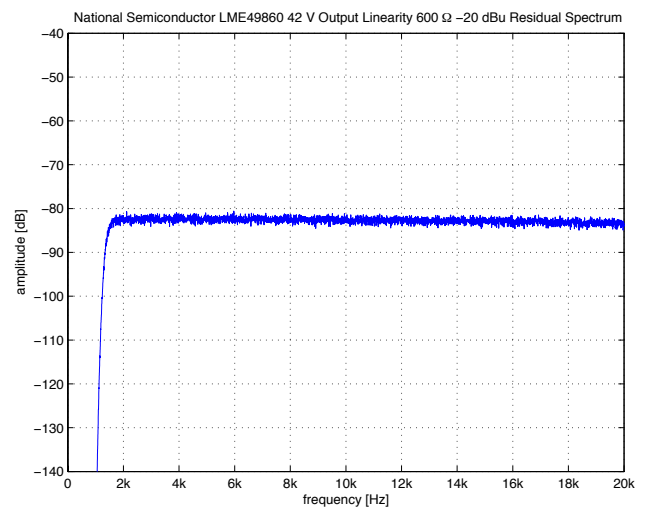
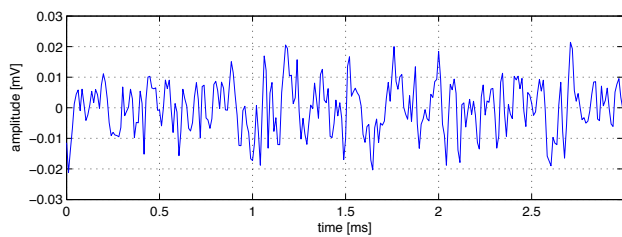
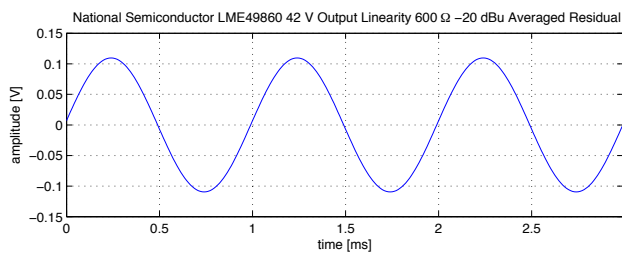
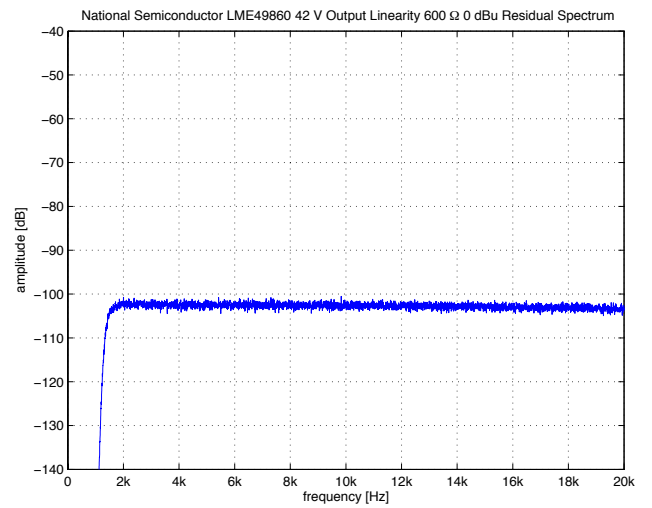
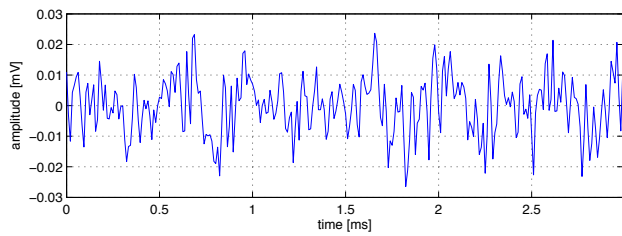
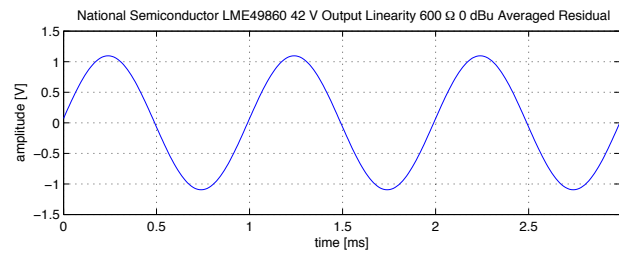
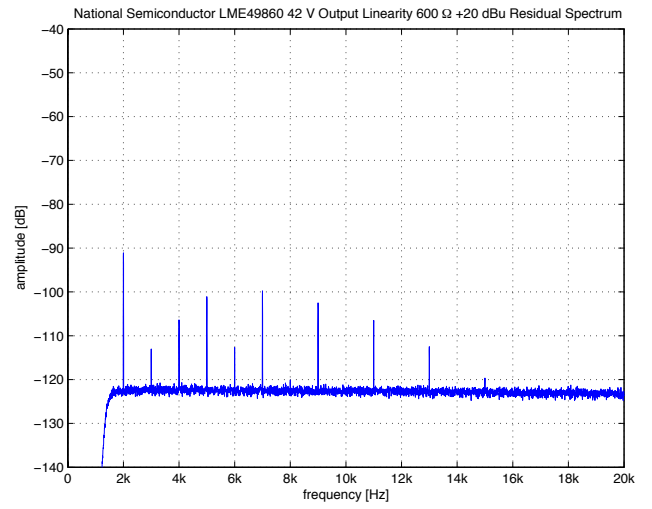
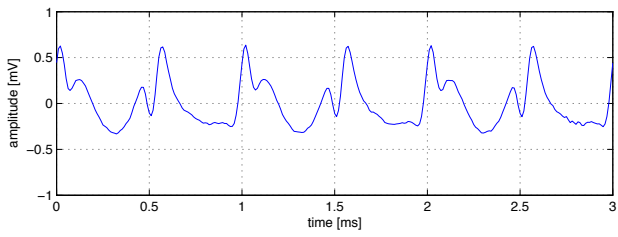
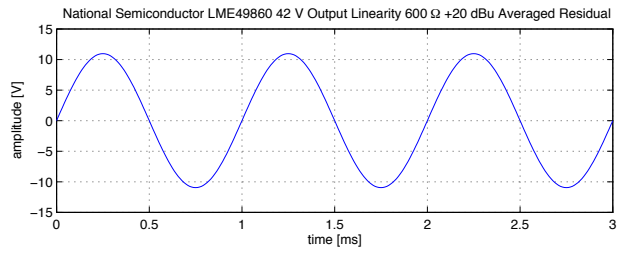












## 3.17 SGA-SOA-1

<b>Number of Channels</b>	1
<b>Packages</b>	API 2500 style

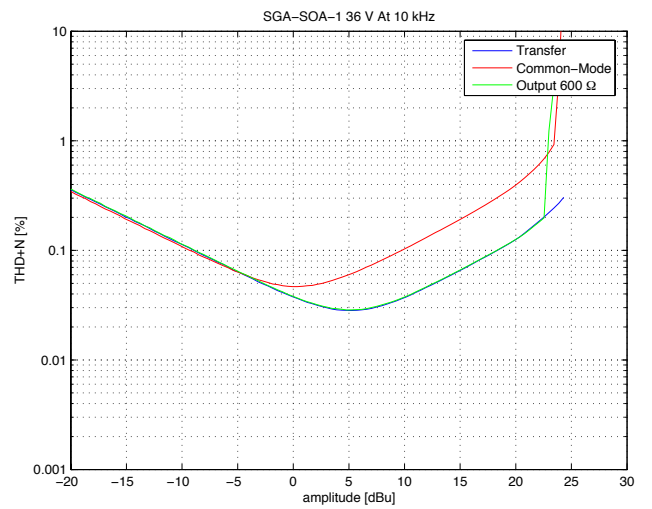
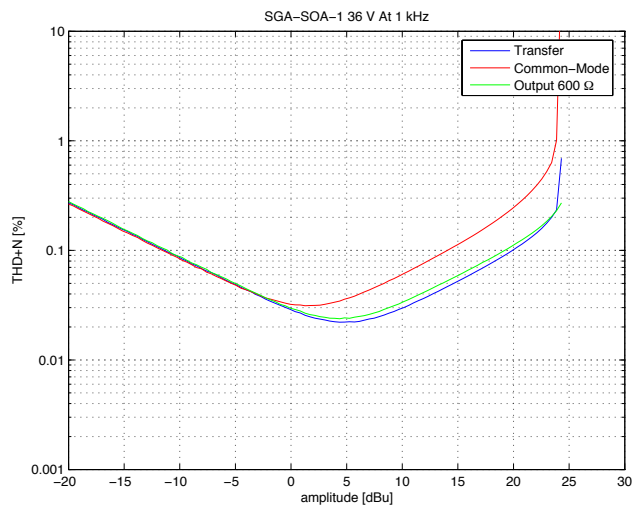
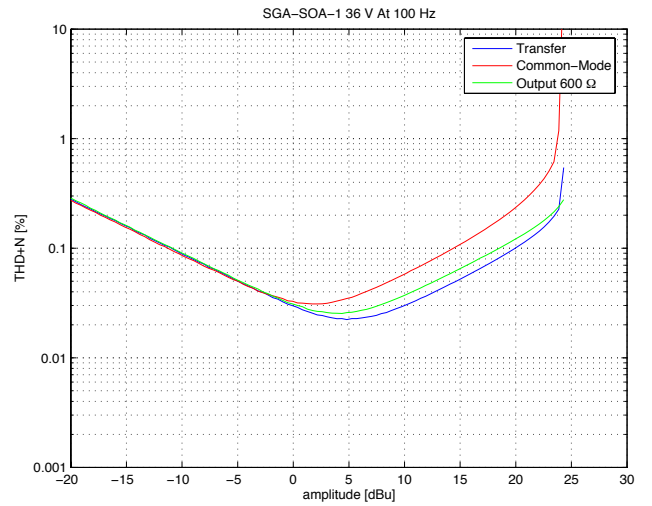
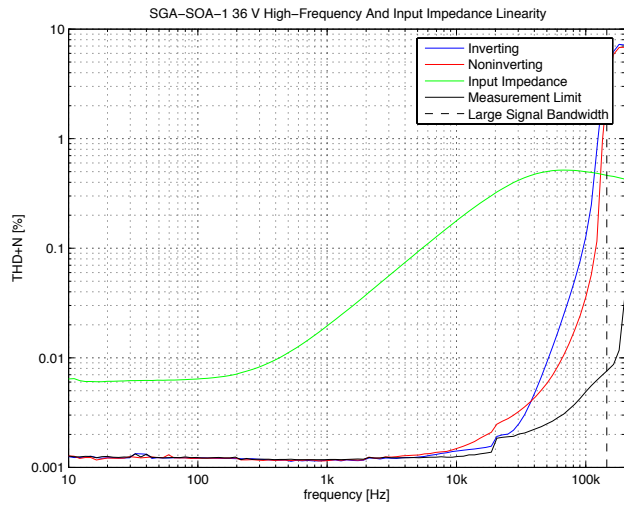
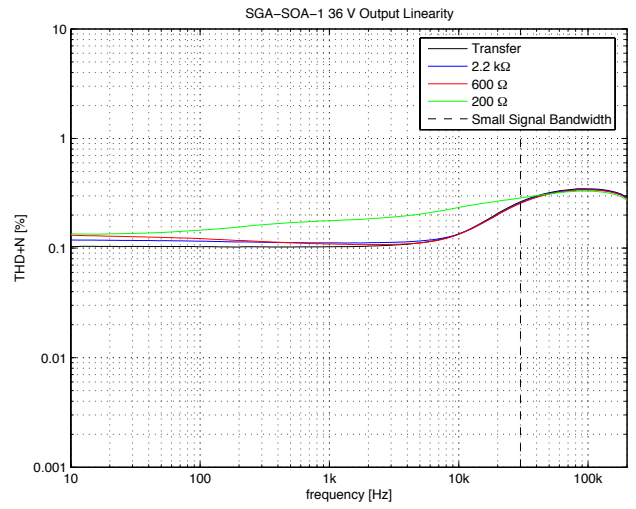
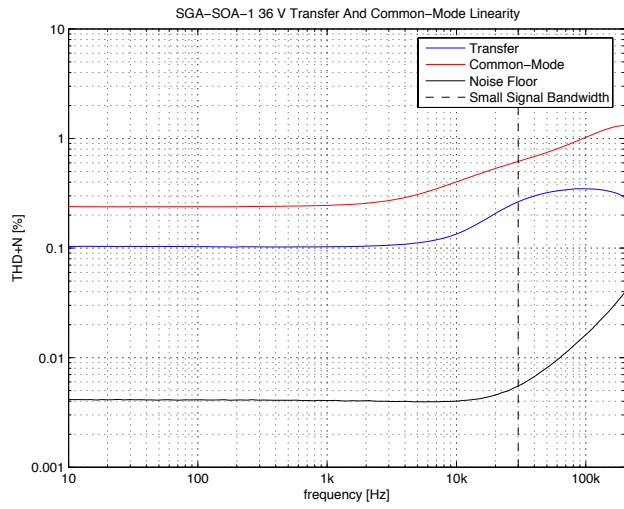
<b>Parameter</b>	<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Unit</b>
Input Offset Voltage		5	20	mV
Input Bias Current		1		$\mu\text{A}$
Gain Bandwidth Product		30		MHz
Slew-Rate		10		$\text{V}/\mu\text{S}$
Input Voltage Noise ( $f = 1 \text{ kHz}$ )		1.5		$\text{nV}/\sqrt{\text{Hz}}$
Input Current Noise ( $f = 1 \text{ kHz}$ )		0.6		$\text{pA}/\sqrt{\text{Hz}}$
Output Voltage Swing ( $R_L = 600 \Omega$ )		$\pm 17$		V
Output Current		$\pm 300$		mA
Power Supply Voltage	$\pm 10$		$\pm 20$	V
Quiescent Current per Amplifier		21		mA

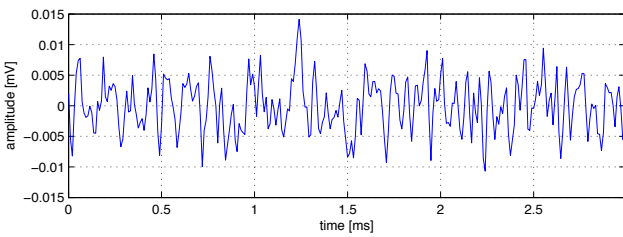
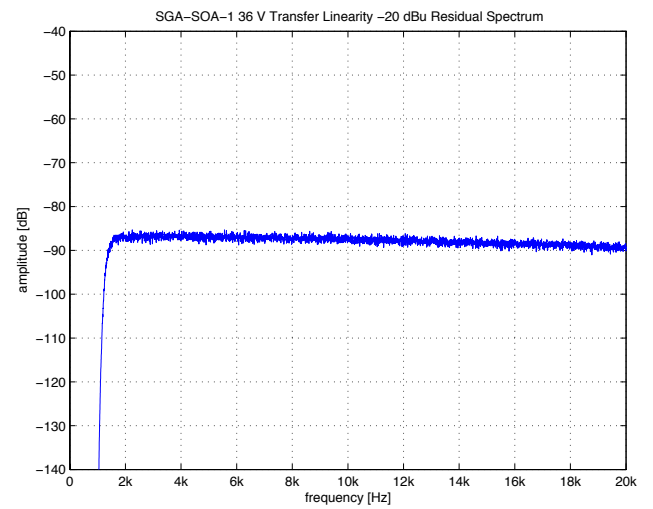
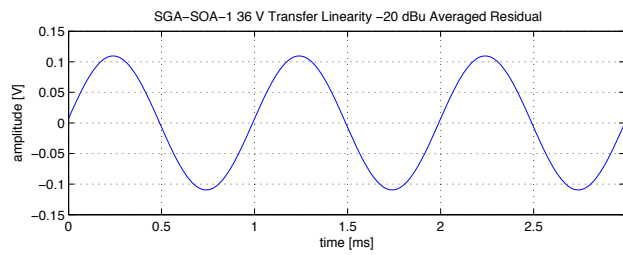
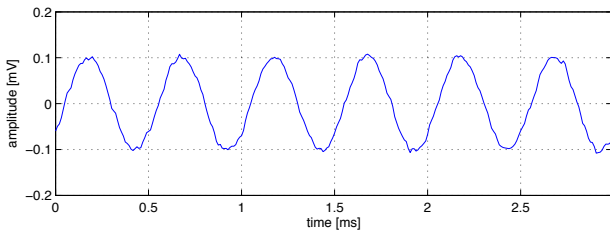
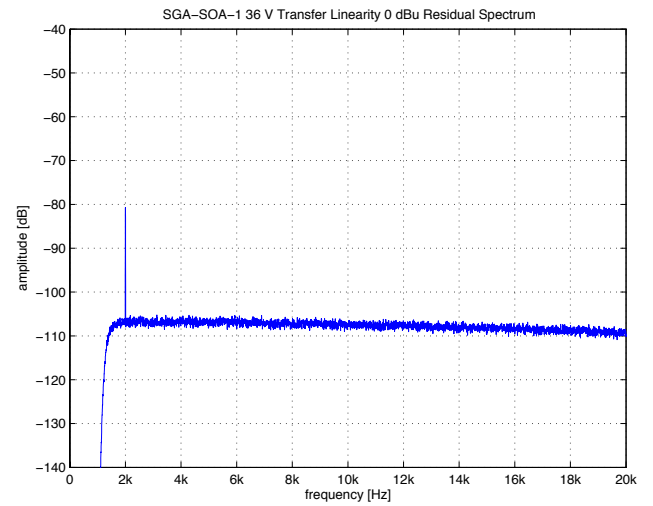
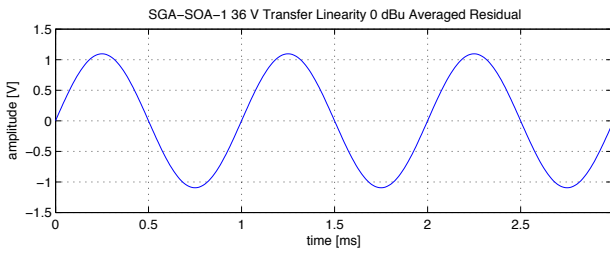
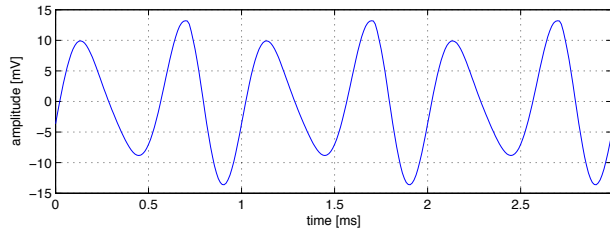
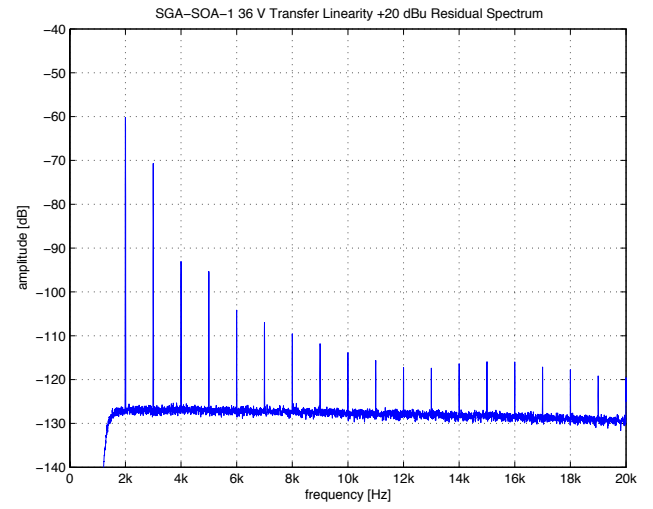
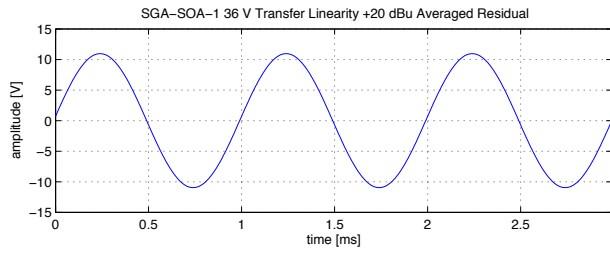
Table 3.17: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 18 \text{ V}$ .

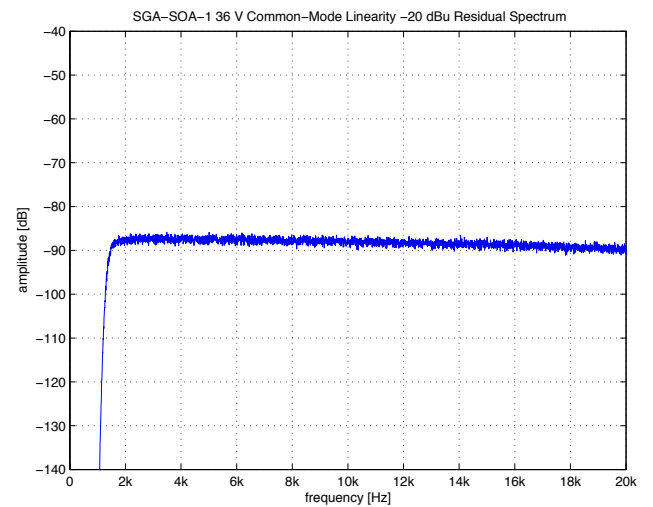
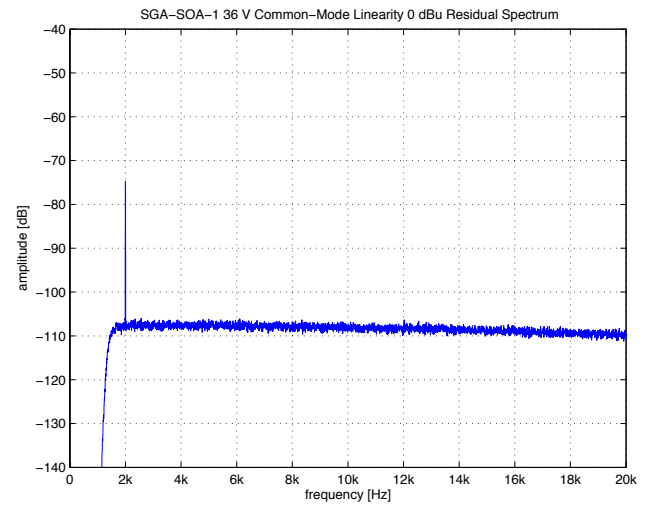
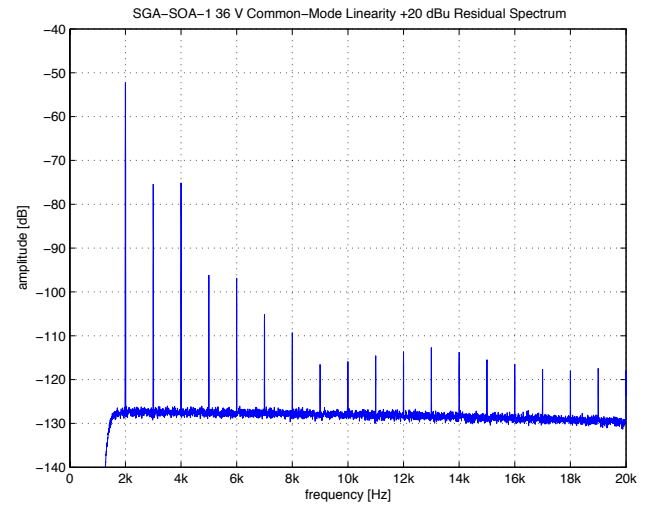
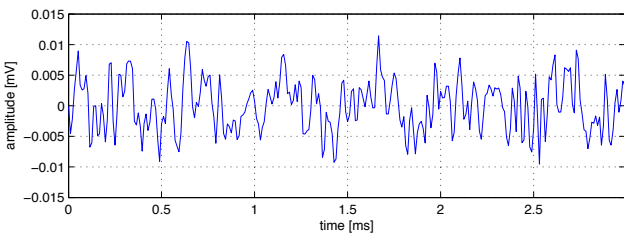
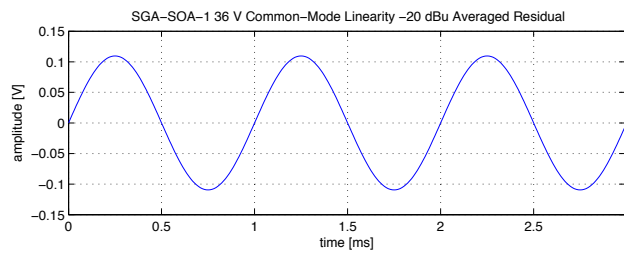
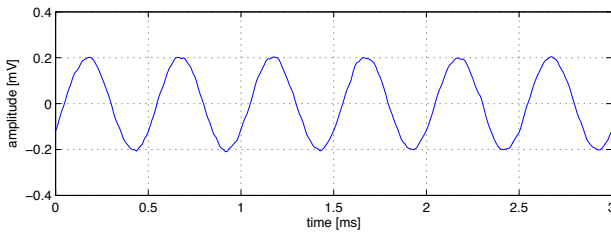
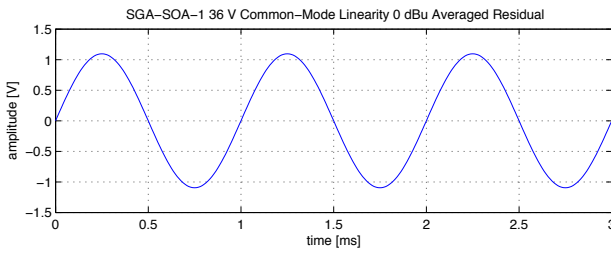
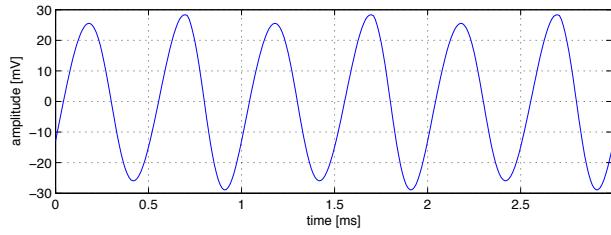
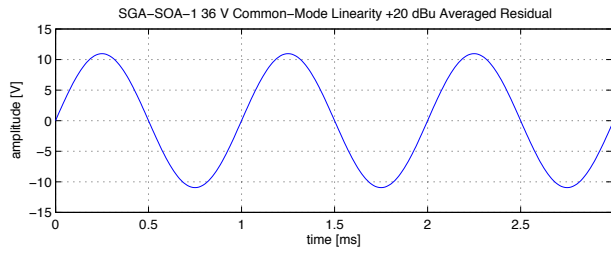
A discrete opamp based on a two-stage topology, designed by the author [15]. The compared with IC amplifiers much simpler circuit does not offer good DC precision but shines with a combination of low voltage noise and excellent load driving capabilities.

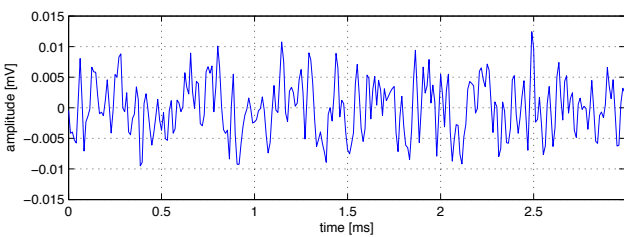
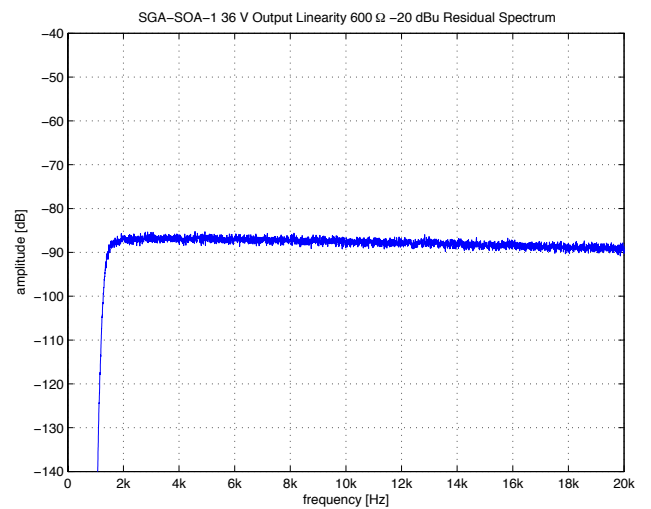
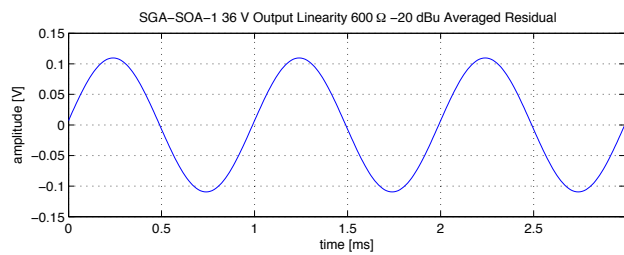
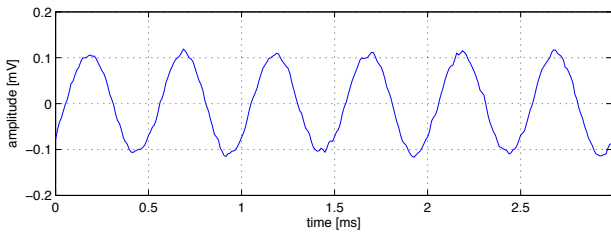
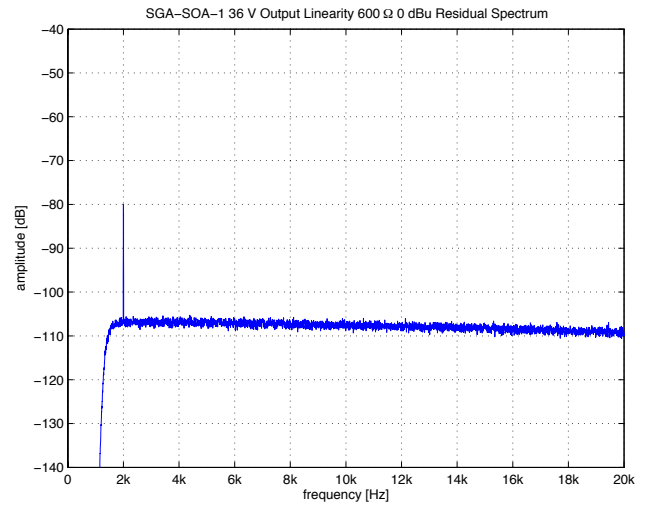
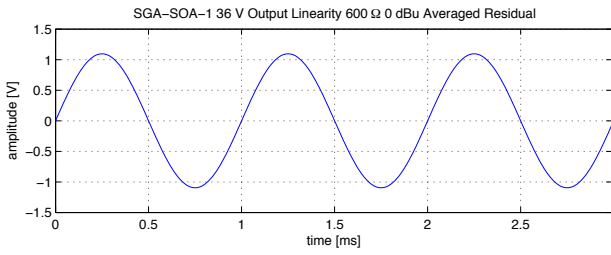
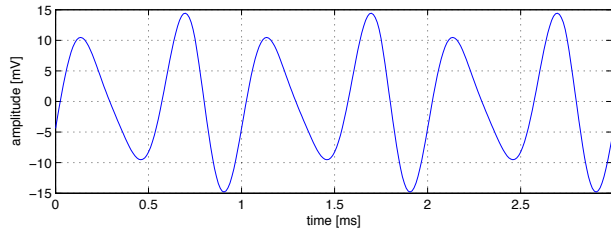
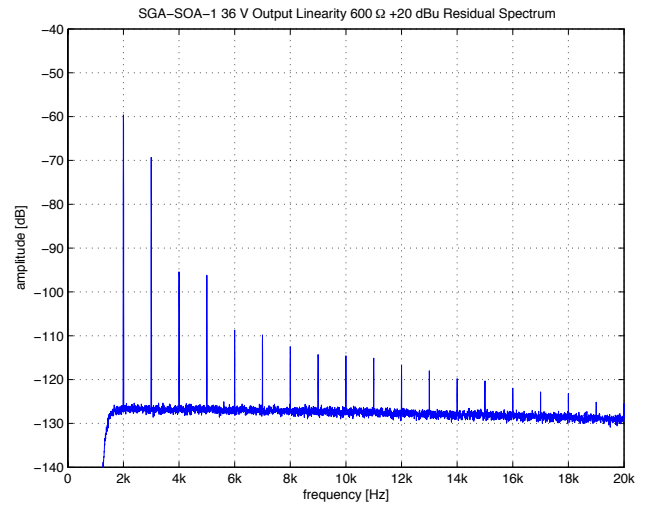
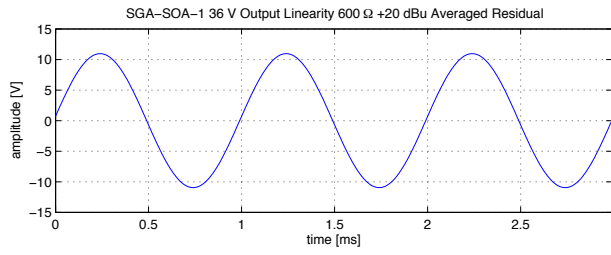
The distortion characteristics of this amplifier are different from the typical IC amplifiers, mainly as a result of the simple circuit design (which uses just 7 transistors) and the class A output stage. While the former causes measurably higher distortion with respect to transfer and common-mode linearity compared to good IC amplifiers the later makes the amplifier performance much more independent of output loading—not only at +20 dBu but especially at lower levels. The relatively low slew-rate limits distortion performance at very high frequencies.

Perhaps interesting where low loads are to be driven. Otherwise behind most IC amplifiers distortion wise.









### 3.18 Signetics NE5532

<b>Number of Channels</b>	2
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	obsolete

Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		0.5	4	mV
Input Bias Current		200	800	nA
Input Offset Current		10	150	nA
Gain Bandwidth Product		22		MHz
Slew-Rate		9		V/ $\mu$ S
Input Voltage Noise (f = 1 kHz)		5		nV/ $\sqrt{\text{Hz}}$
Input Current Noise (f = 1 kHz)		0.7		pA/ $\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 12$	$\pm 13$		V
Output Voltage Swing ( $R_L = 600 \Omega$ )	$\pm 12$	$\pm 13$		V
Output Voltage Swing ( $R_L = 2 \text{ k}\Omega$ )	$\pm 13$	$\pm 13.5$		V
Power Supply Voltage	$\pm 3$		$\pm 22$	V
Quiescent Current per Amplifier		4	8	mA

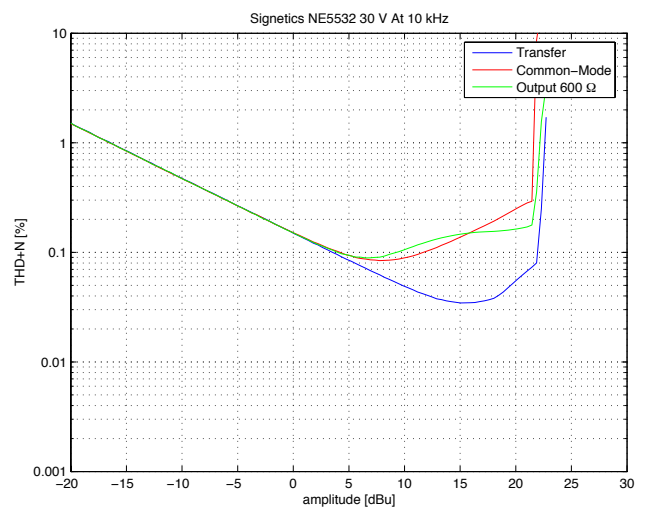
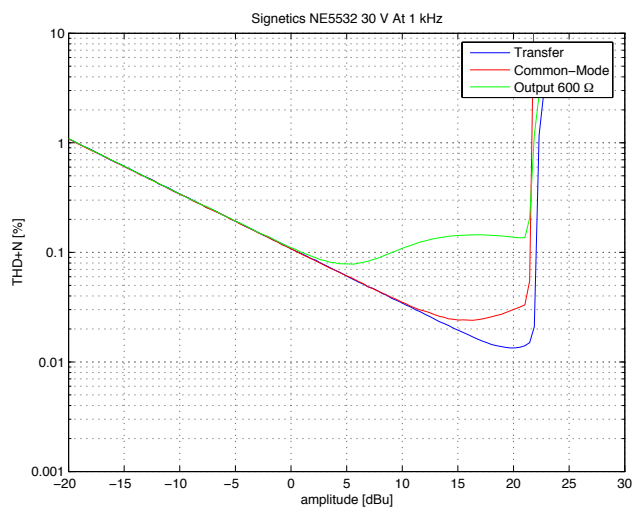
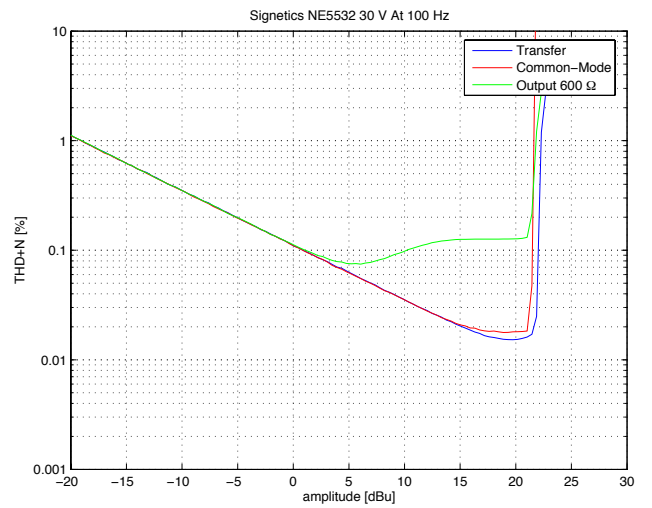
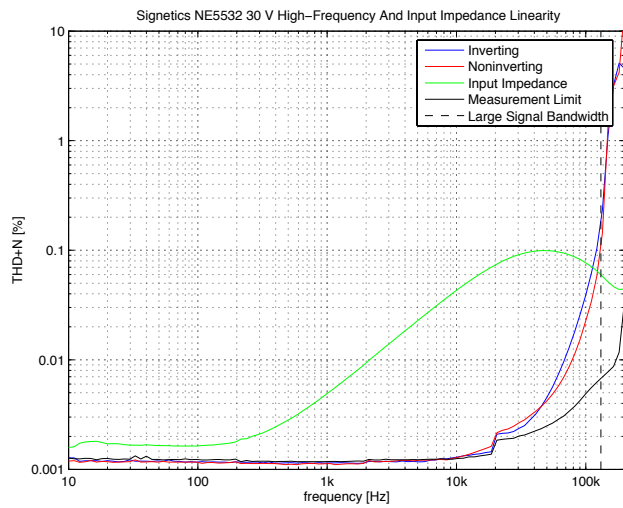
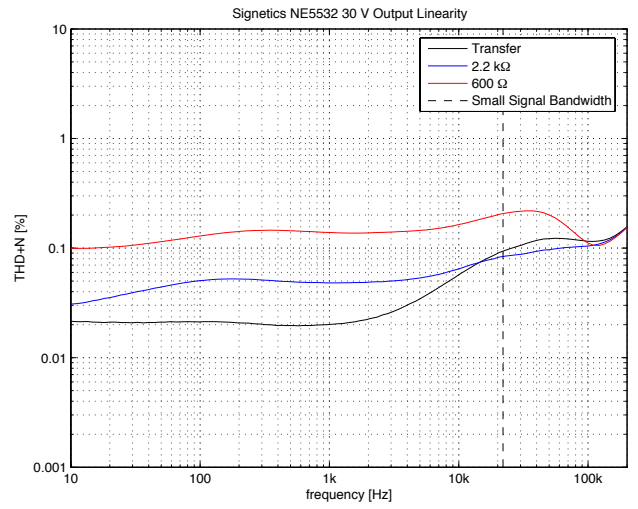
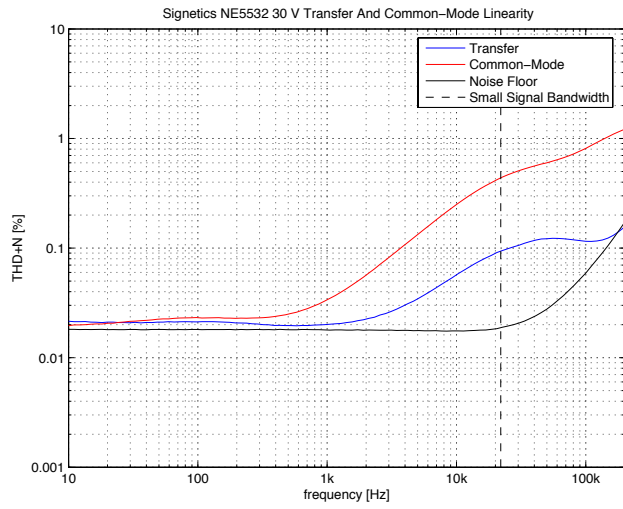
Table 3.18: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 15 \text{V}$ .

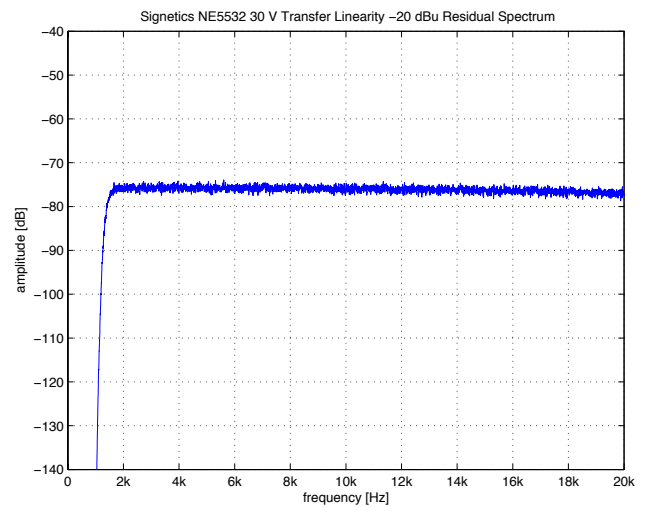
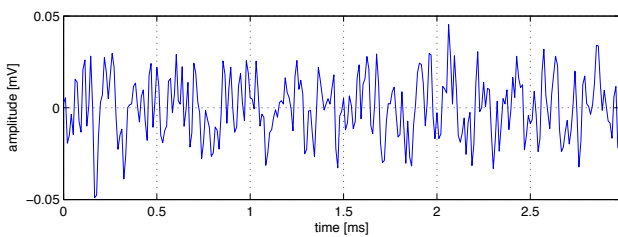
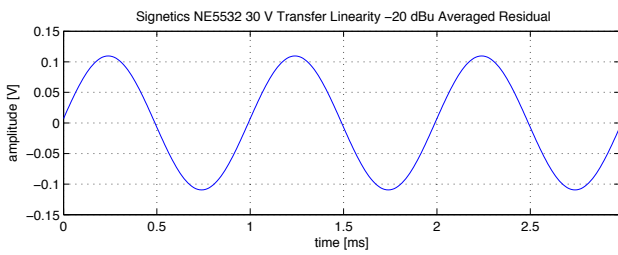
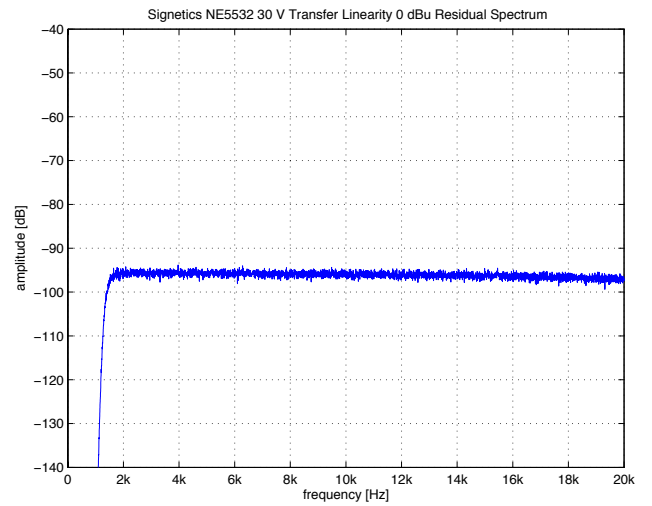
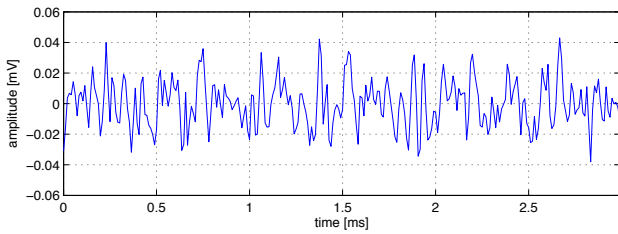
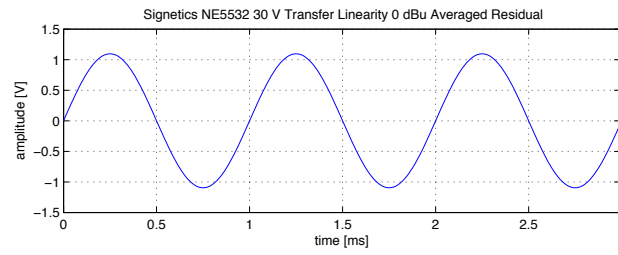
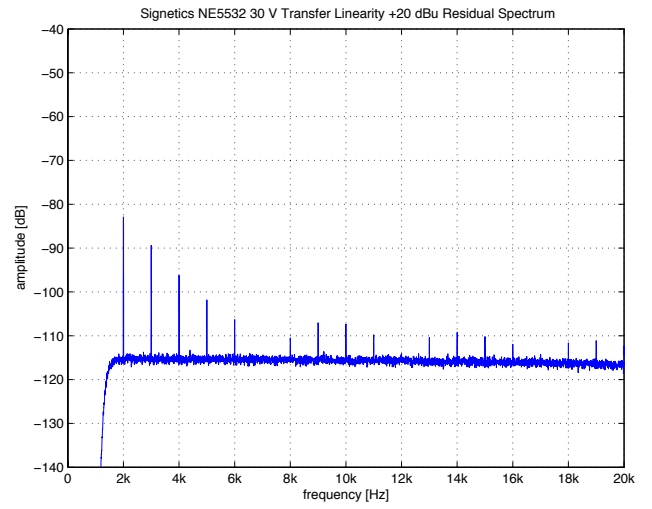
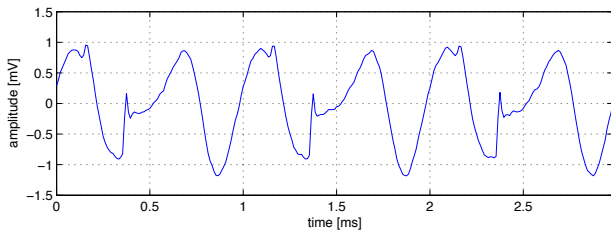
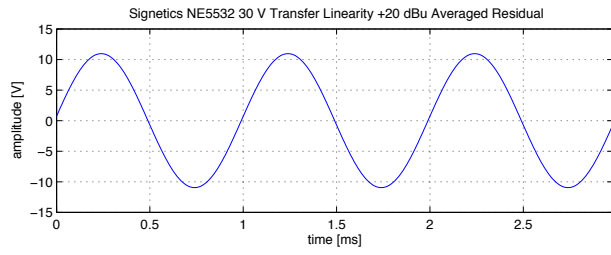
An obsolete dual amplifier, now sourced by other manufacturers. It was included for the test mainly to see whether significant differences in performance compared to other manufacturers can be observed; the measurements with higher supply voltage were omitted though.

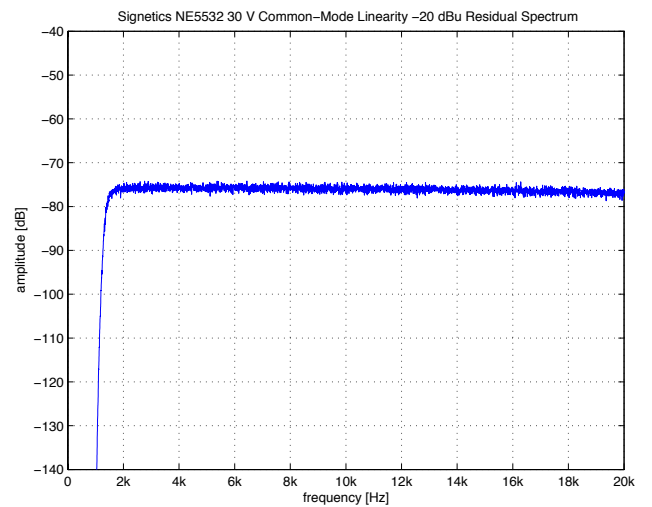
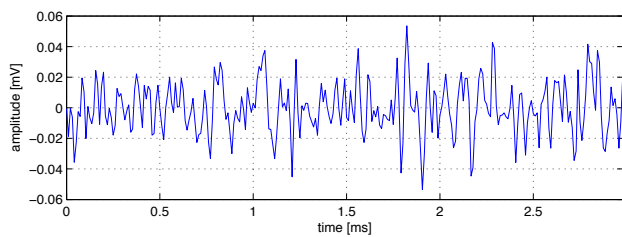
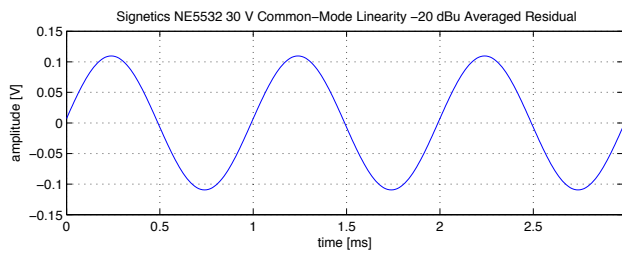
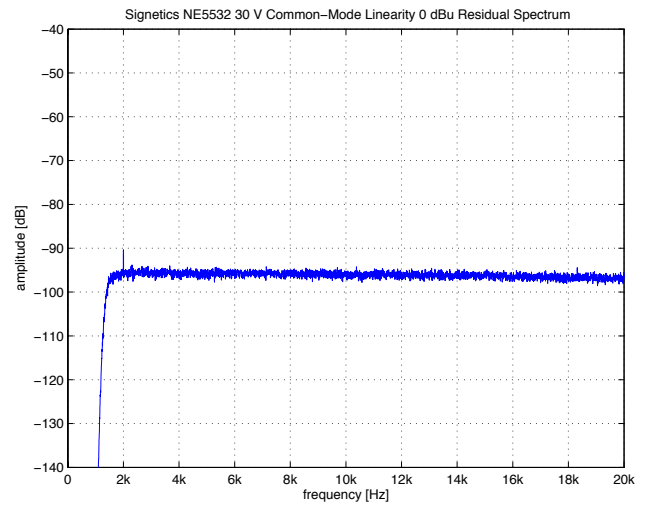
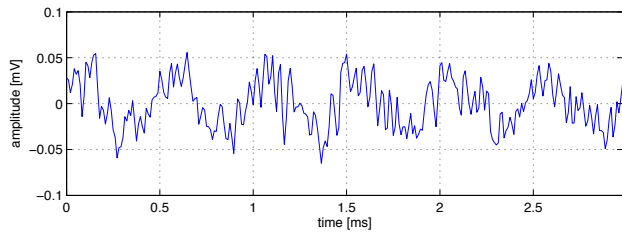
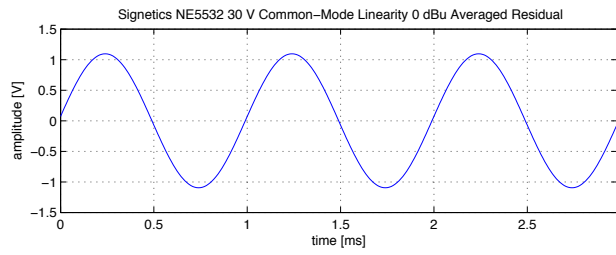
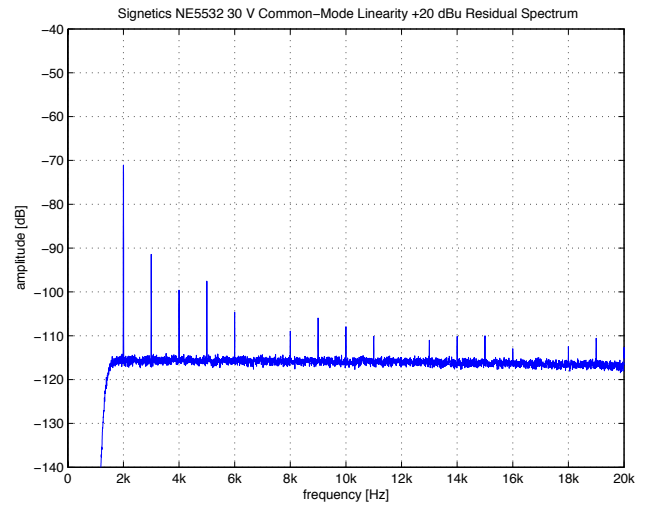
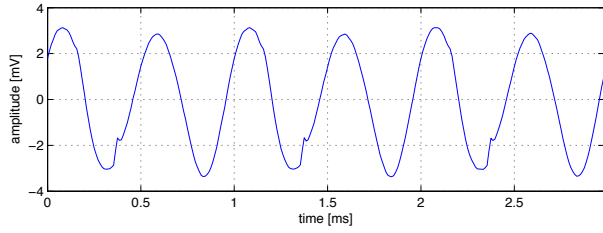
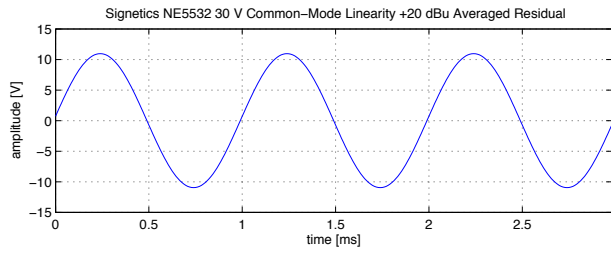
The amplifier uses a three-stage topology with bipolar input. Note that the input bias currents are not cancelled, hence rather large. Voltage and current noise are moderately low, giving good noise figure at medium-low source impedances.

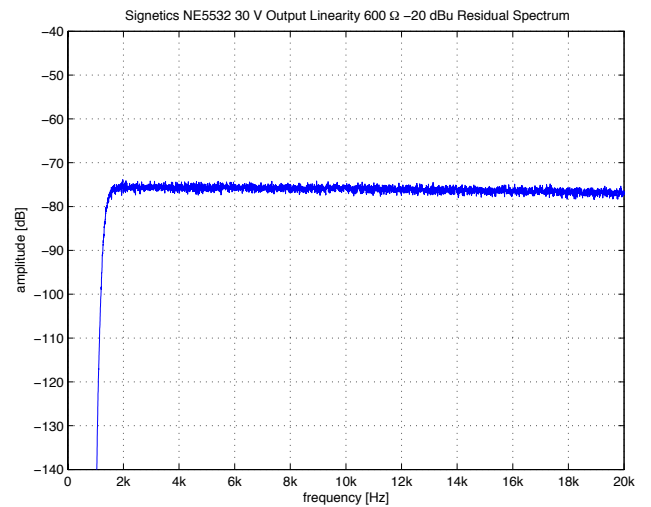
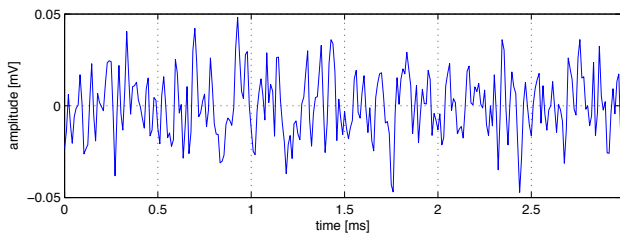
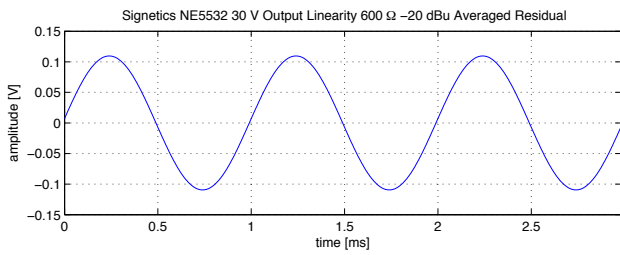
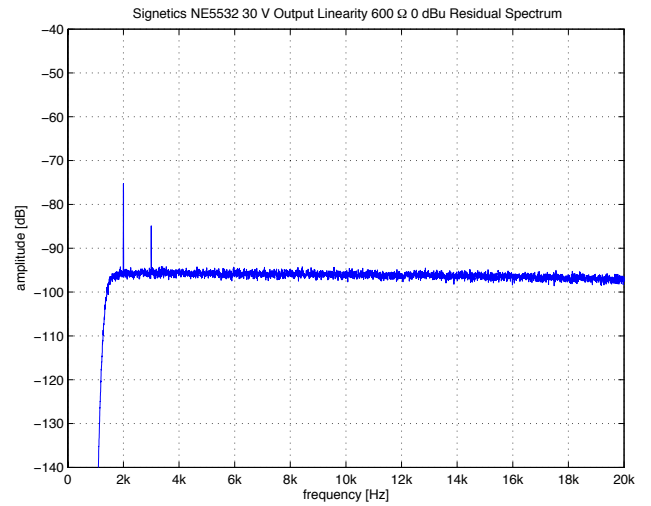
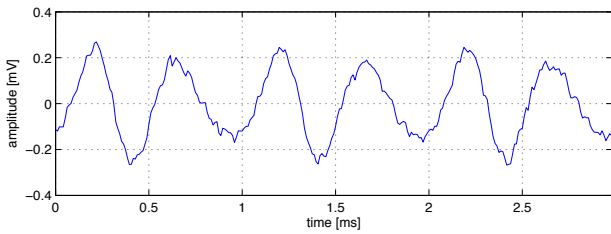
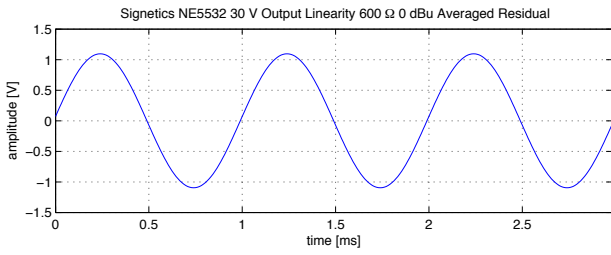
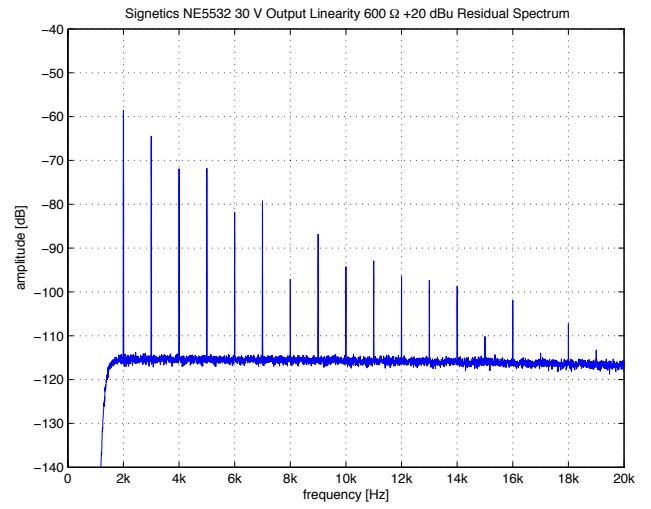
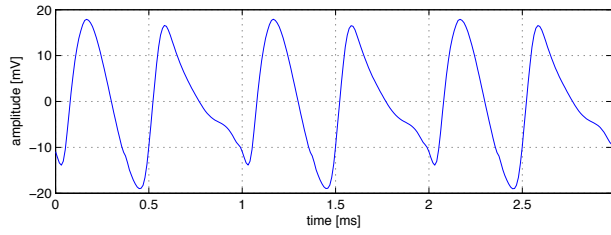
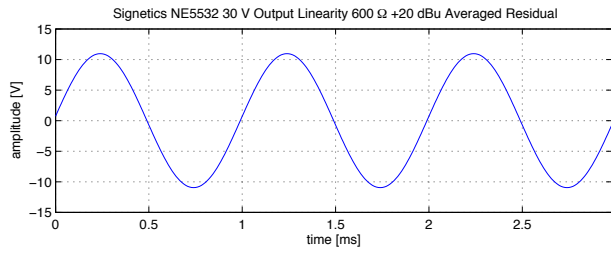
The overall distortion performance is relatively similar to the equivalent amplifier manufactured by Texas Instruments (see page 148). A noticeable exception is common-mode distortion which is clearly better at higher frequencies for the Signetics part. On the other hand the residual at +20 dBu shows conspicuously spiky waveforms for the transfer and common-mode linearity measurement. It is unclear what could cause such behaviour—at least the artefacts are at low level such that they do not significantly degrade total harmonic distortion.











## 3.19 Texas Instruments MC33078

<b>Number of Channels</b>	2
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	0.15 US\$ at 1k units (August 2008)

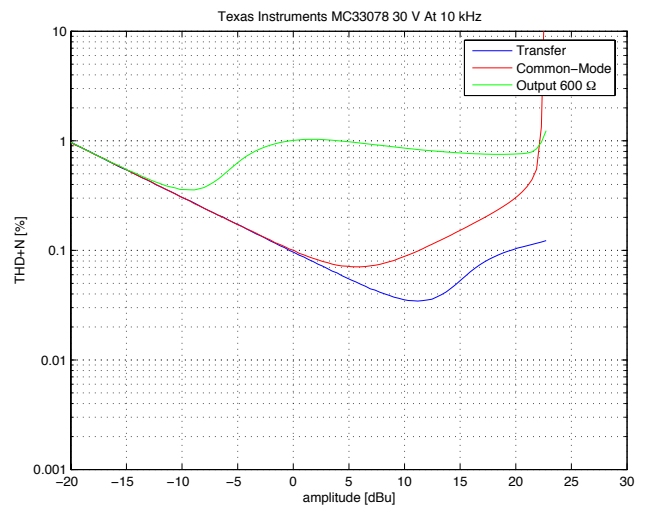
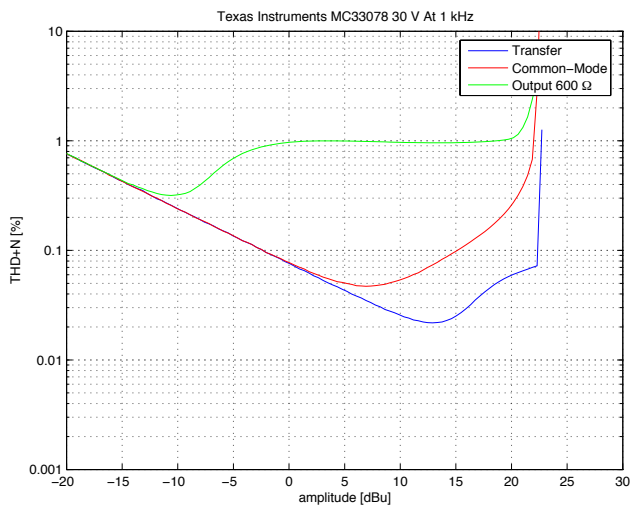
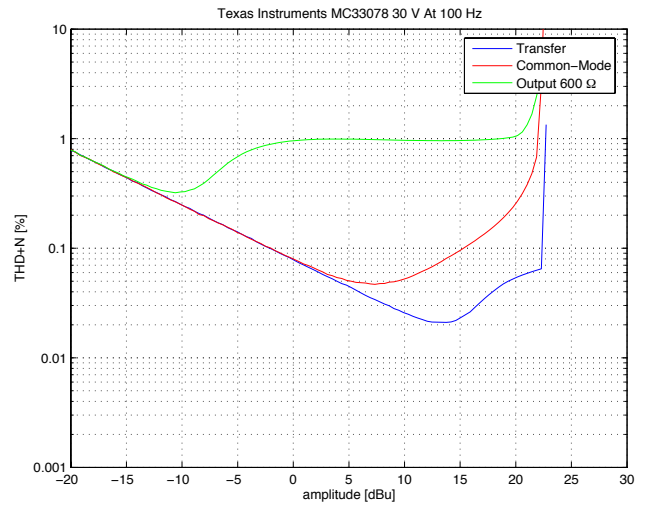
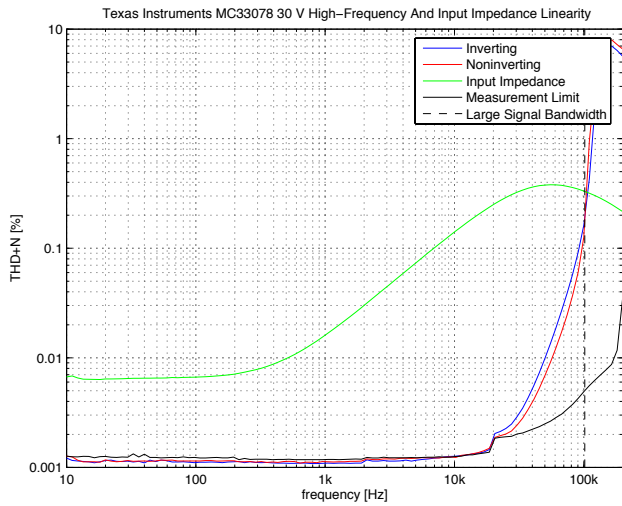
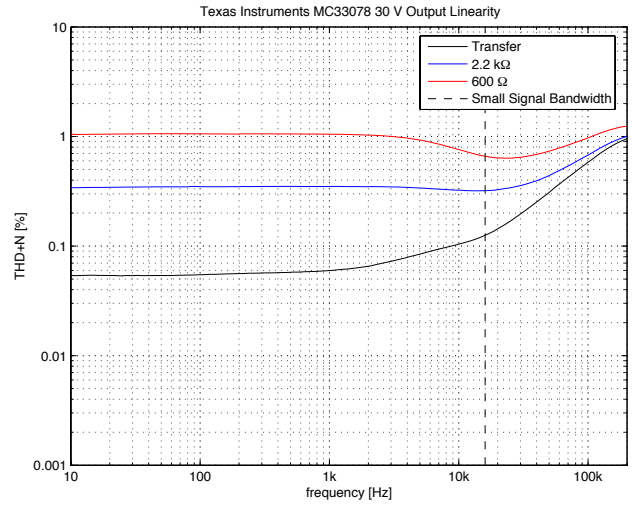
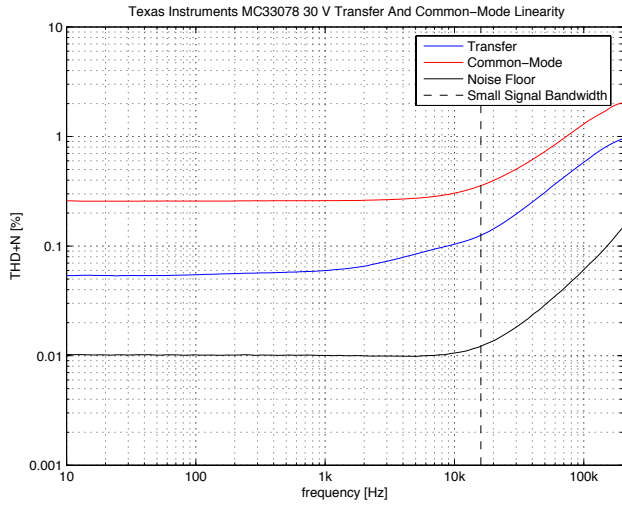
Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		0.15	2	mV
Input Bias Current		300	750	nA
Input Offset Current		25	150	nA
Gain Bandwidth Product	10	16		MHz
Slew-Rate	5	7		V/ $\mu$ S
Input Voltage Noise (f = 1 kHz)		4.5		nV/ $\sqrt{\text{Hz}}$
Input Current Noise (f = 1 kHz)		0.5		pA/ $\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 13$	$\pm 14$		V
Output Voltage Swing ( $R_L = 2 \text{ k}\Omega$ )	$\pm 13.2$	$+13.8/-13.7$		V
Output Voltage Swing ( $R_L = 600 \Omega$ )	$+10.7/-11.9$			V
Output Current	$+15/-20$	$+29/-37$		mA
Power Supply Voltage	$\pm 5$		$\pm 18$	V
Quiescent Current per Amplifier		2.05	2.5	mA

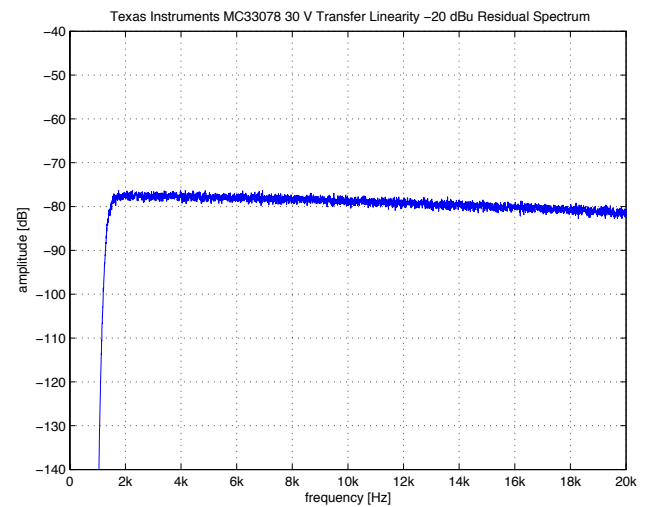
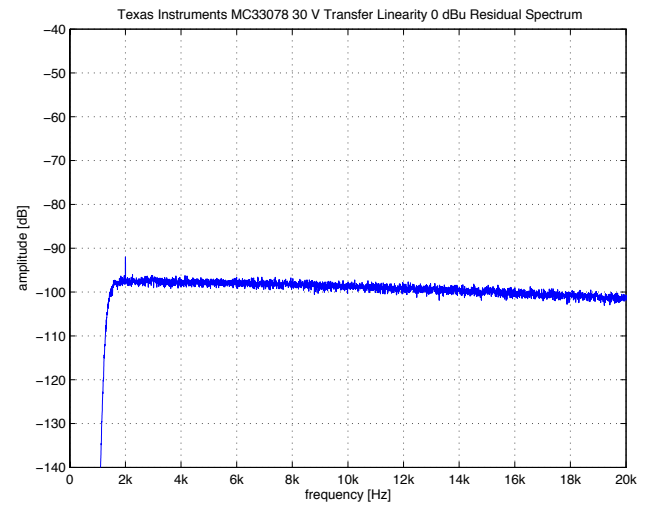
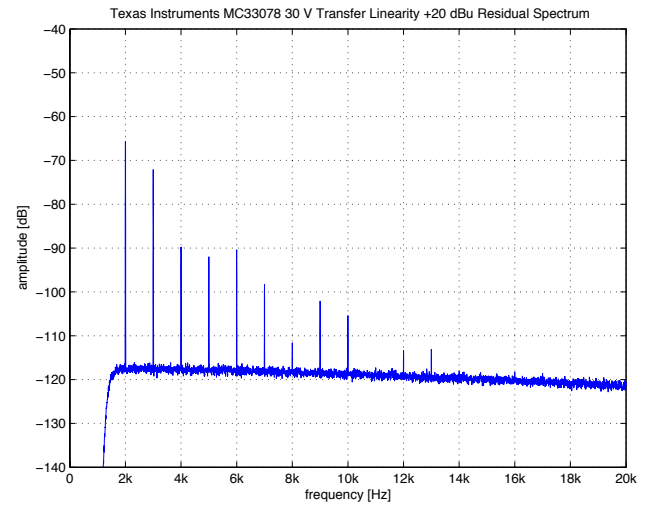
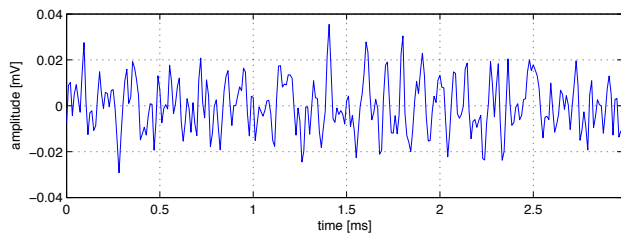
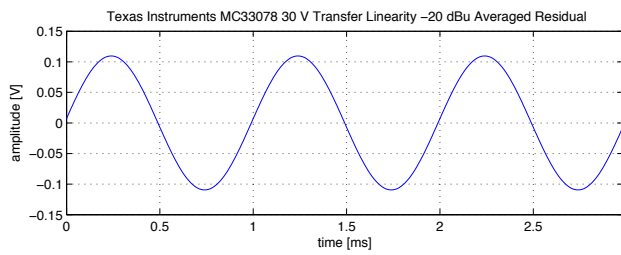
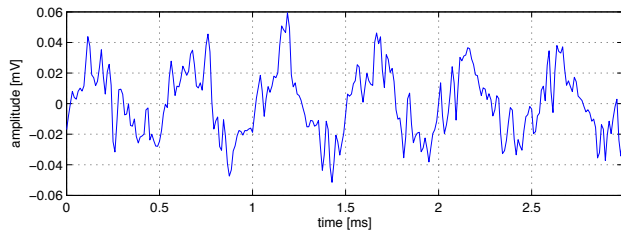
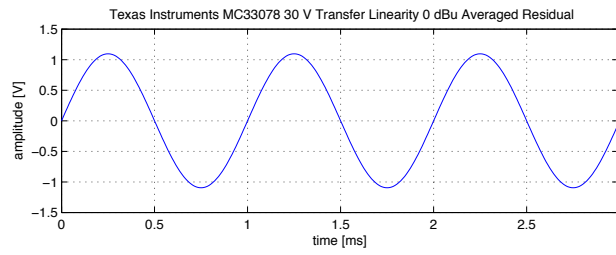
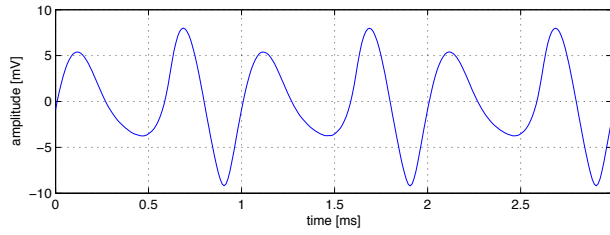
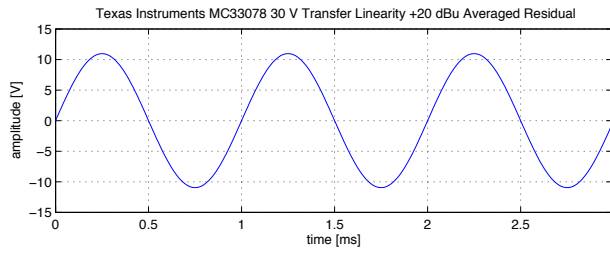
Table 3.19: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 15 \text{V}$ .

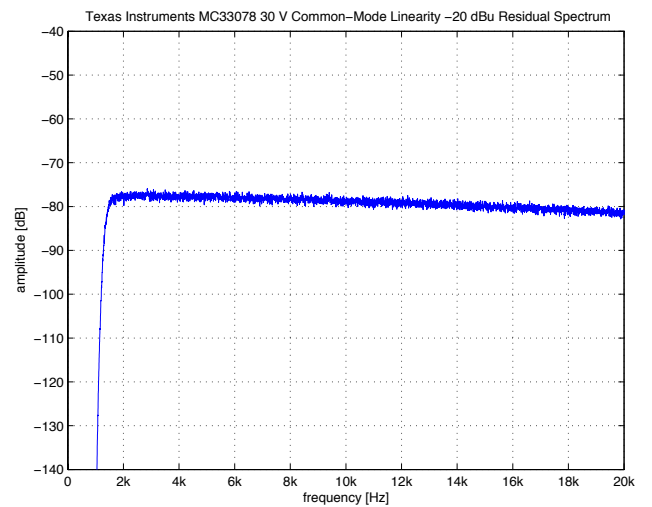
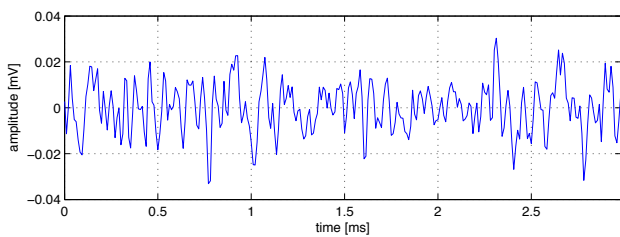
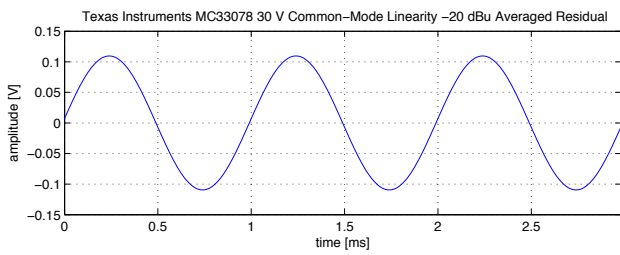
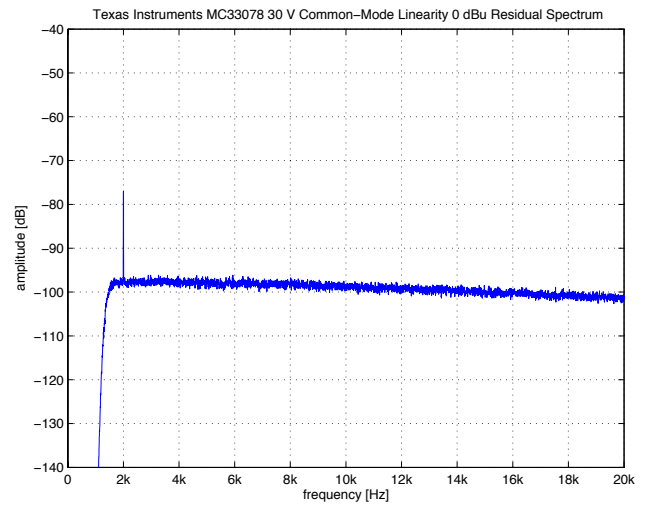
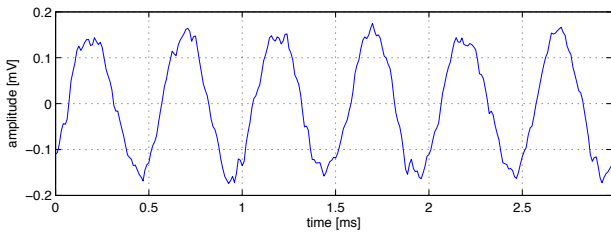
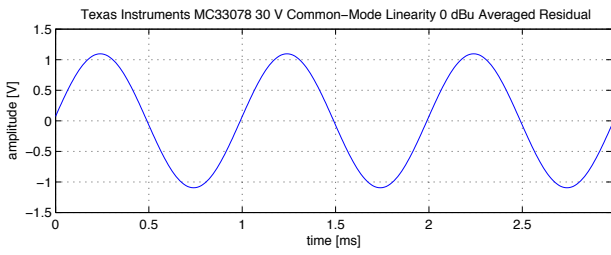
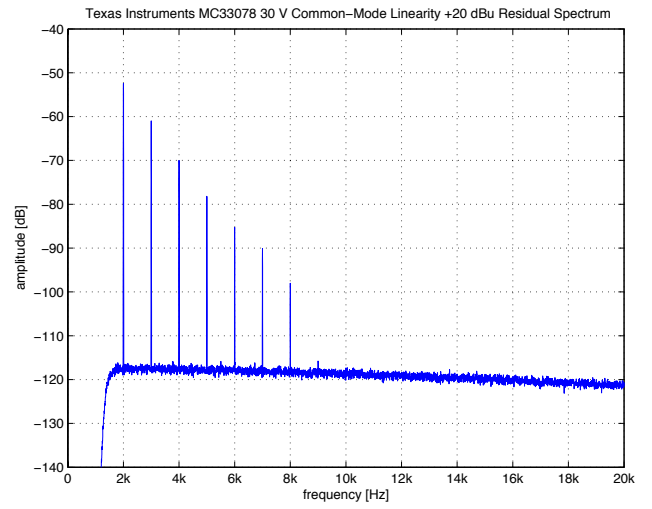
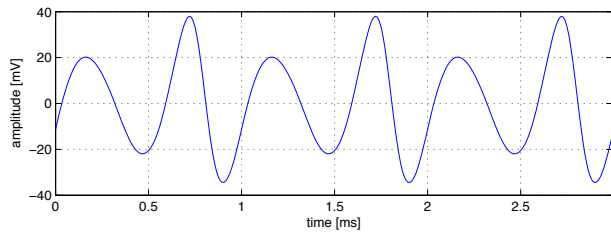
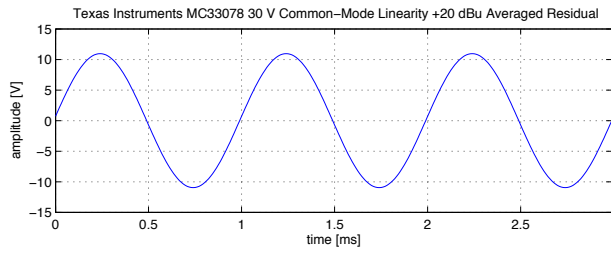
An opamp based on a standard two-stage topology and a BJT input stage. Noise performance is optimised for medium source impedances. Note the rather wide common-mode input range and that no input bias current cancellation is used.

The transfer linearity is modestly good and degrades at high frequencies due to the limited slew-rate. Both common-mode and input impedance linearity is not particularly good either. However, tremendously bad is the output linearity—distortion is measurable even at  $-20 \text{ dBu}$ .

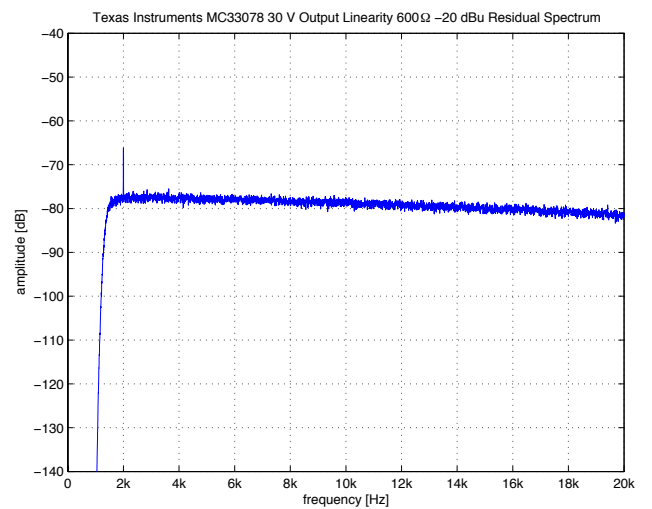
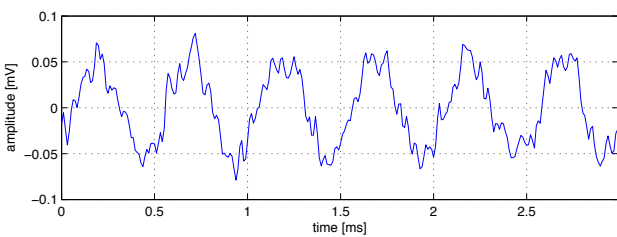
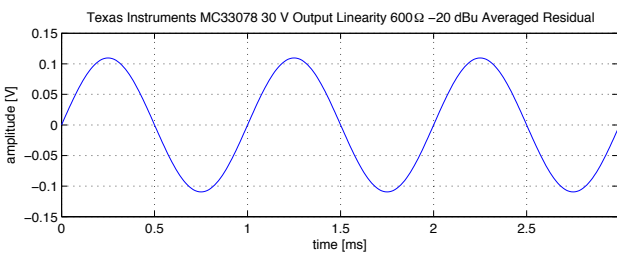
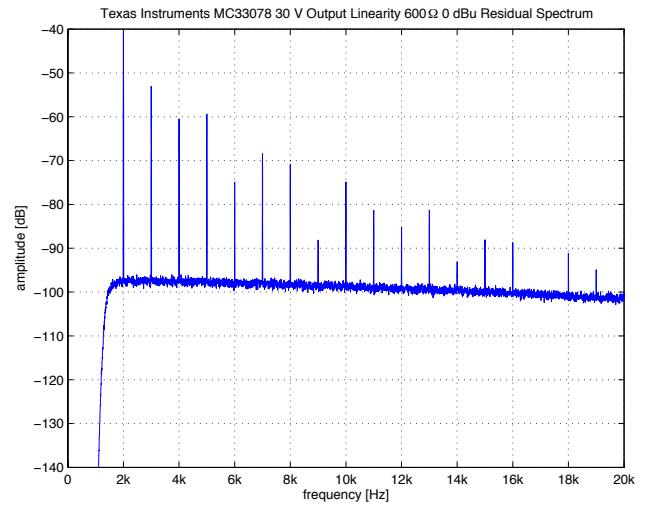
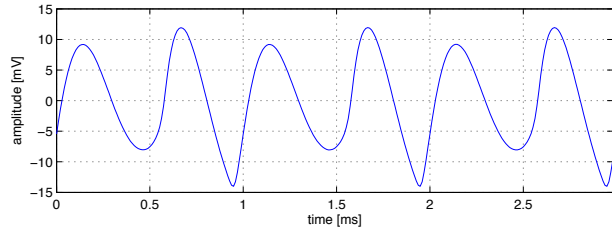
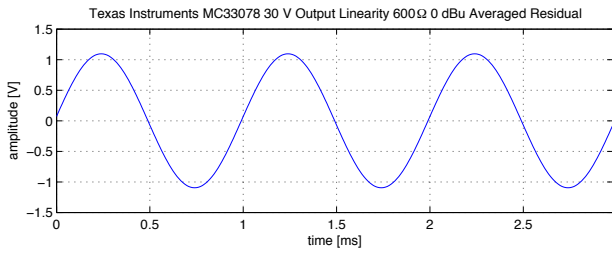
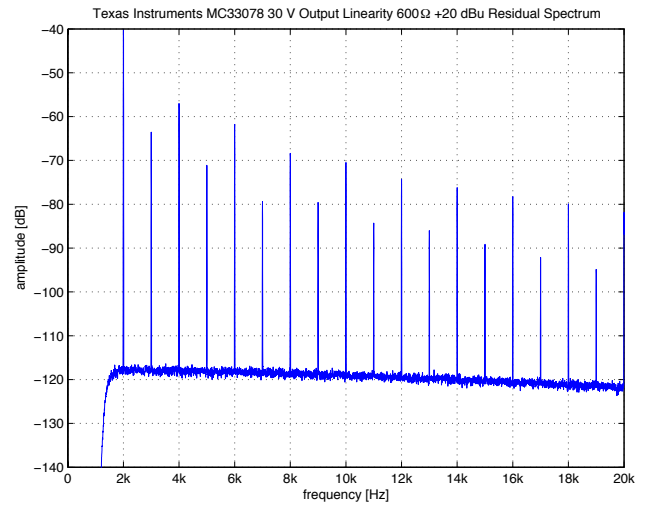
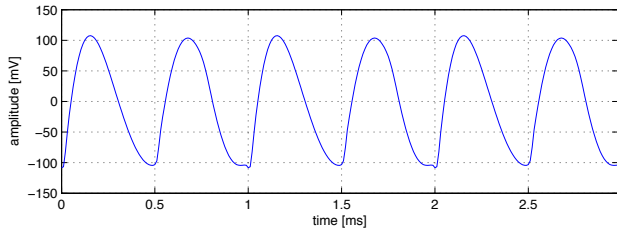
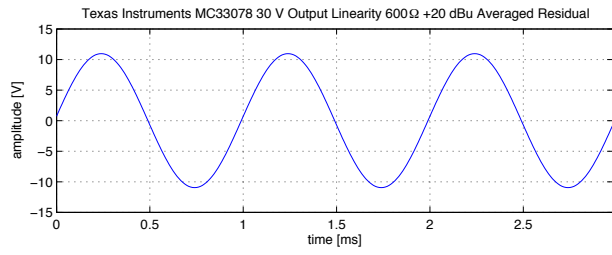
Reasonable performance with this opamp is only obtainable where output loading can be made negligible; there are similarly priced opamps with better performance available.











### 3.20 Texas Instruments NE5532

<b>Number of Channels</b>	2
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	0.18 US\$ at 1k units (July 2008)

Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		0.5	4	mV
Input Bias Current		200	800	nA
Input Offset Current		10	150	nA
Gain Bandwidth Product		22		MHz
Slew-Rate		9		V/ $\mu$ S
Input Voltage Noise (f = 1 kHz)		5		nV/ $\sqrt{\text{Hz}}$
Input Current Noise (f = 1 kHz)		0.7		pA/ $\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 12$	$\pm 13$		V
Output Voltage Swing ( $R_L = 600 \Omega$ )	$\pm 12$	$\pm 13$		V
Power Supply Voltage	$\pm 3$		$\pm 22$	V
Quiescent Current per Amplifier		4	8	mA

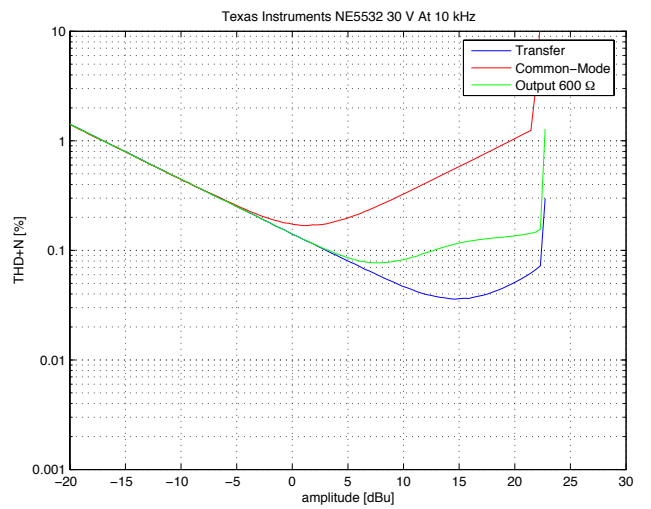
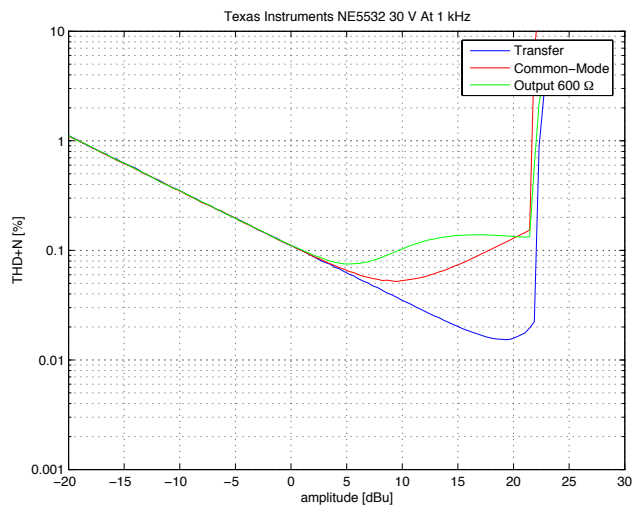
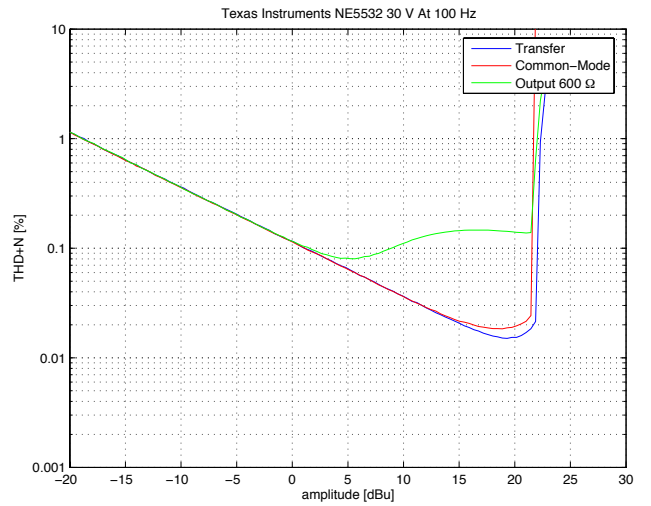
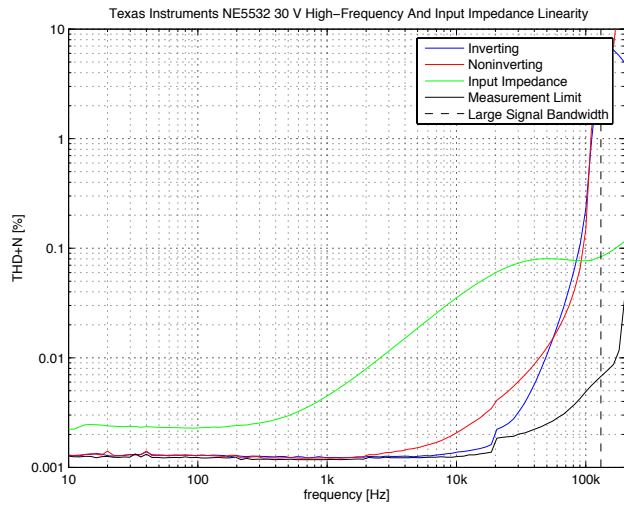
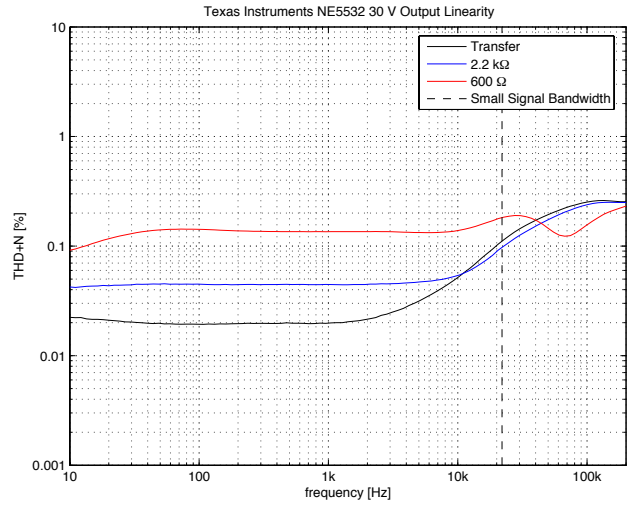
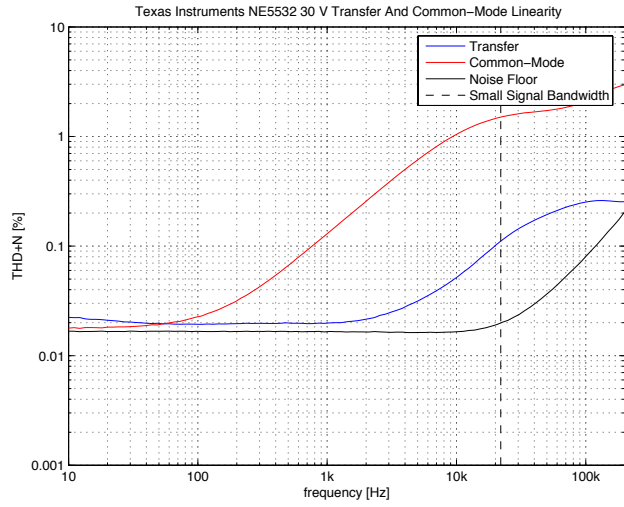
Table 3.20: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 15 \text{V}$ .

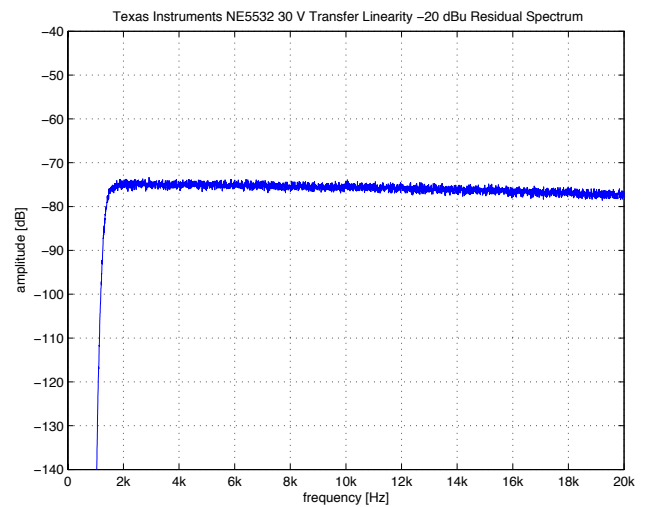
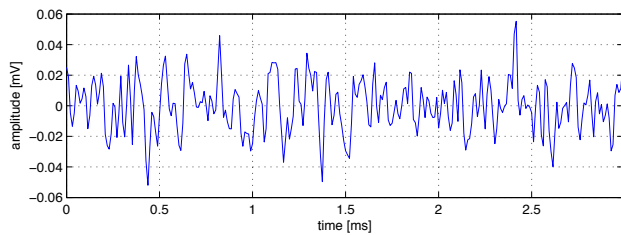
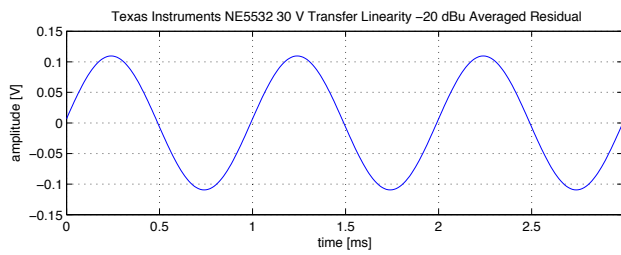
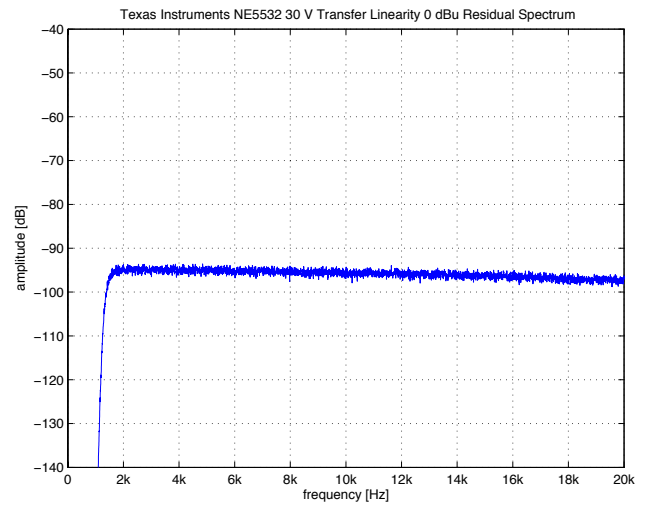
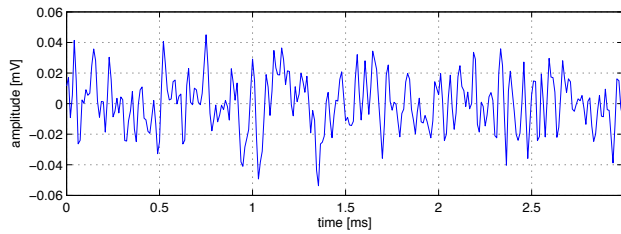
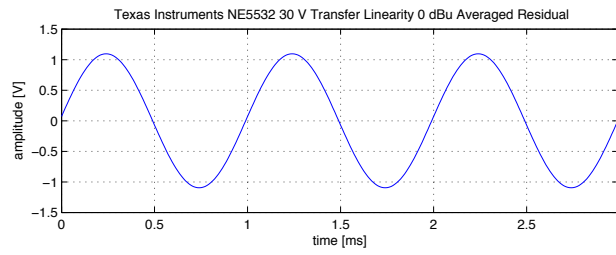
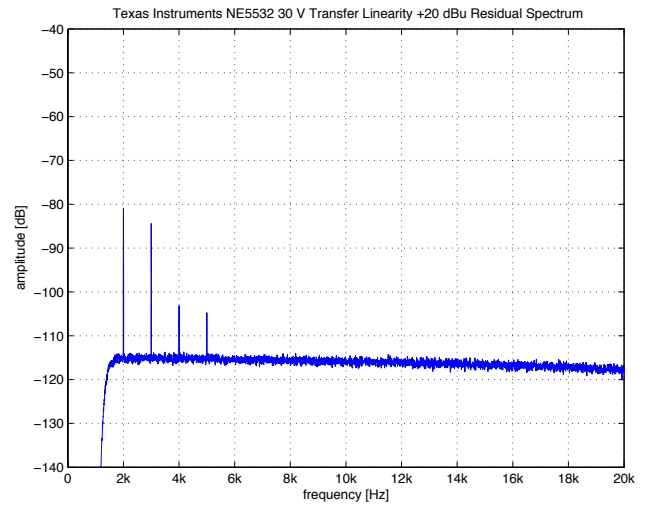
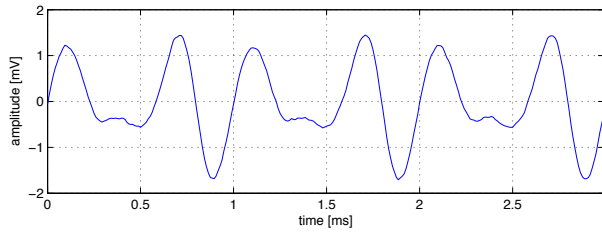
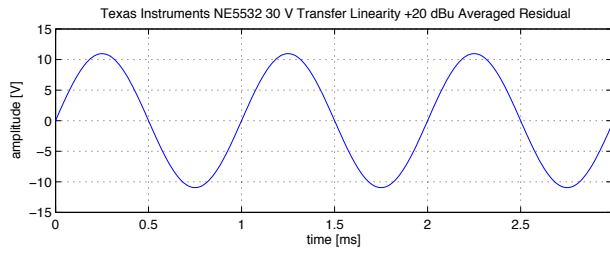
A widely used standard dual audio operational amplifier with BJT input. The design is based on a three-stage architecture as many precision amplifiers. The noise figure is pretty good for medium-low source impedances around a few  $\text{k}\Omega$  and it can operate up to unusually high supply voltages. An externally compensated version (NE5534, see page 157) with lower voltage noise<sup>7</sup> is available.

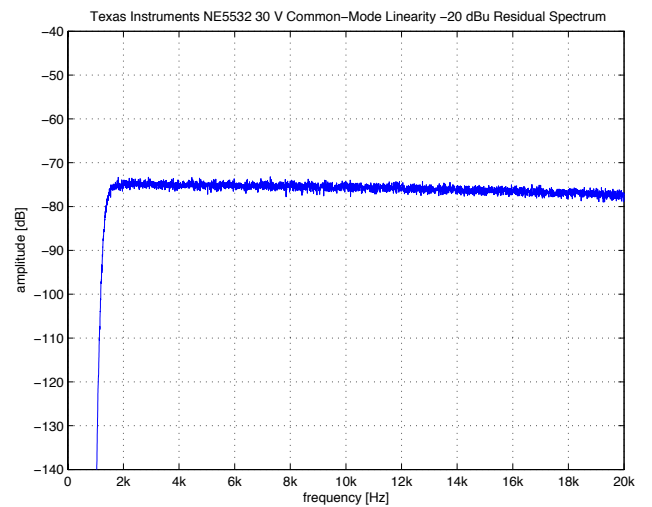
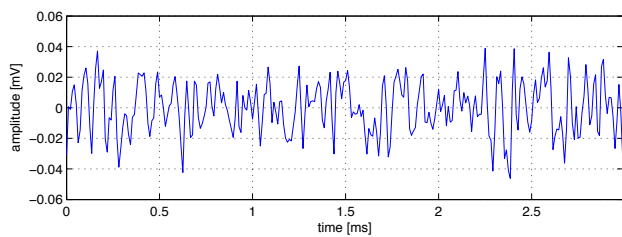
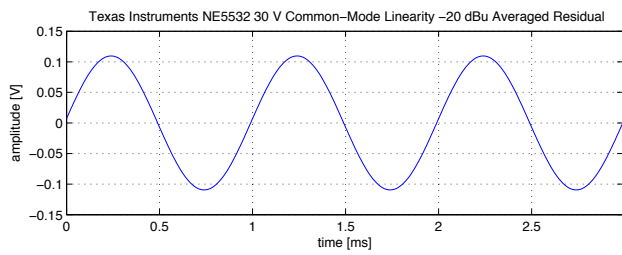
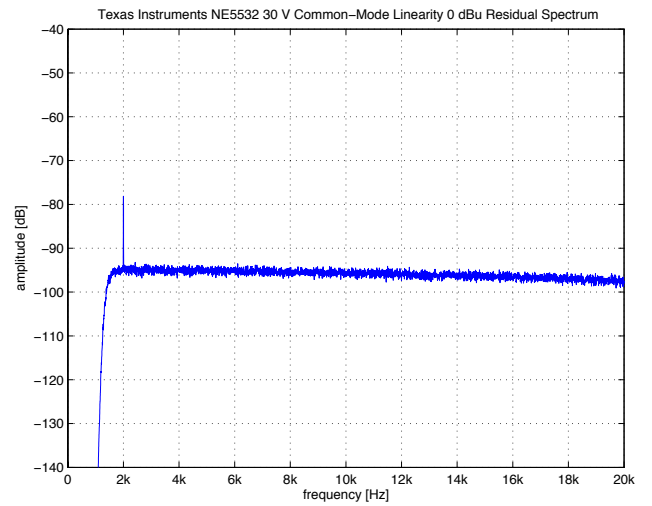
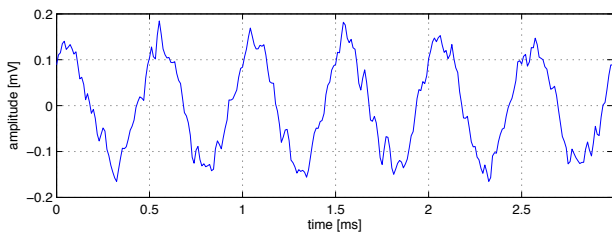
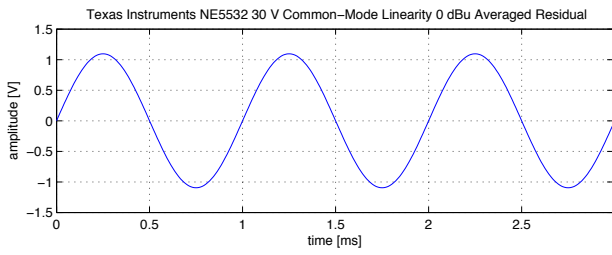
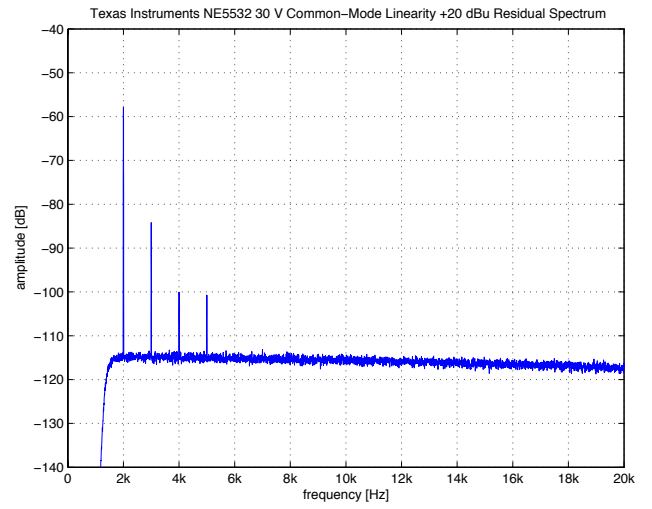
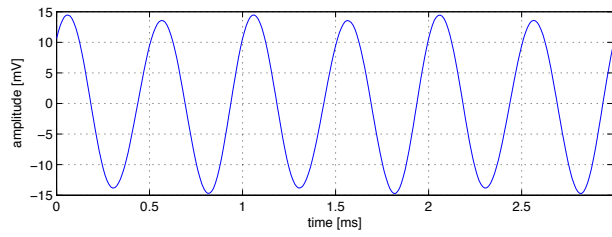
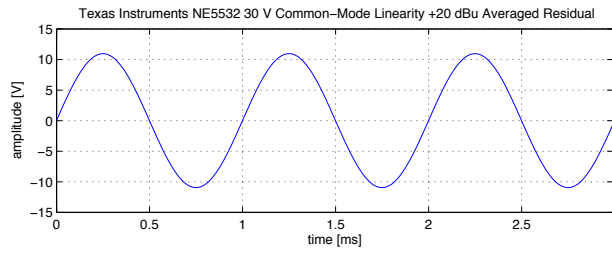
The transfer linearity is—despite the age of this IC design—rather good up to the upper end of the audio frequency range. However common-mode and output loading distortion will severely degrade performance. High-frequency distortion is limited by the relatively low slew-rate. Note the thermal effects which cancel some other distortion products at very low frequencies. Higher supply voltages seem not to help performance here, except for the input impedance modulation. Common-mode distortion at low frequencies even got worse with the supplies risen to  $\pm 22 \text{V}$ .

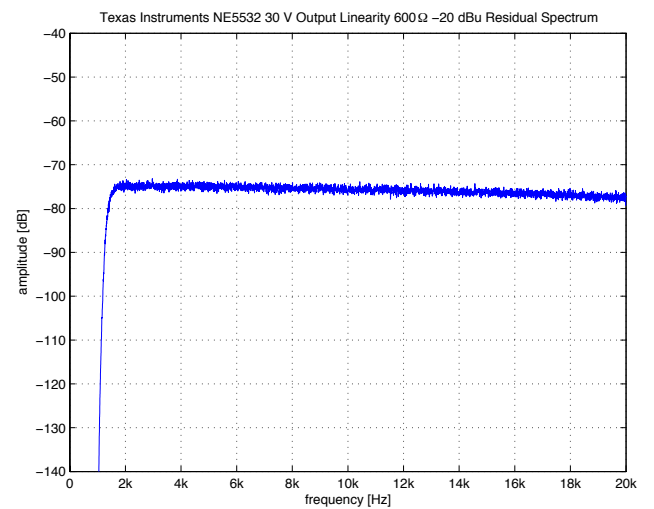
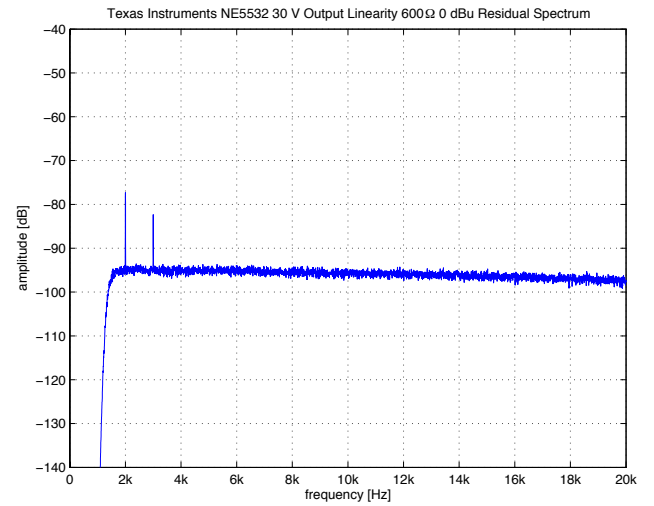
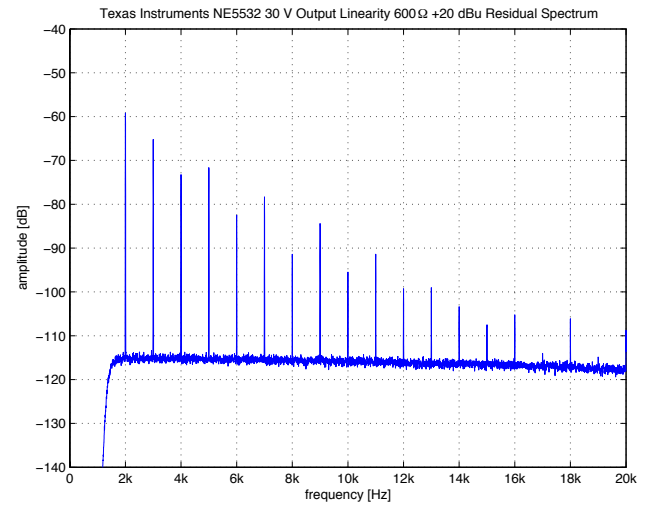
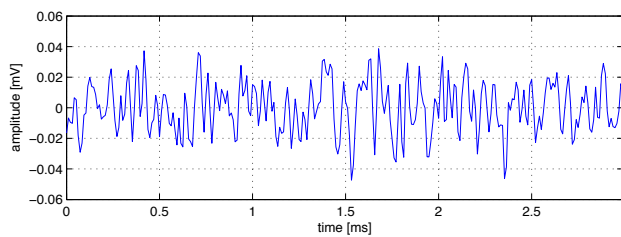
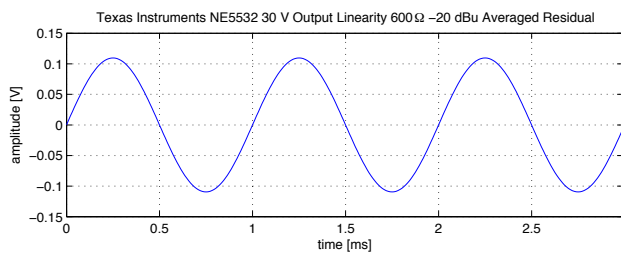
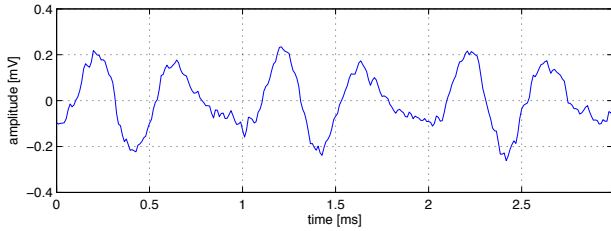
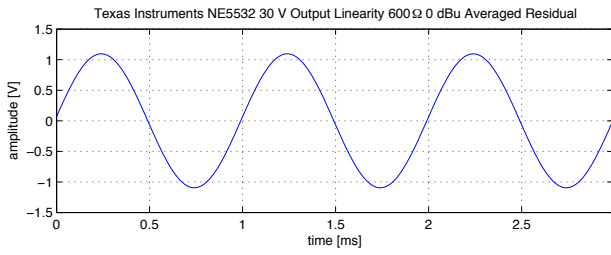
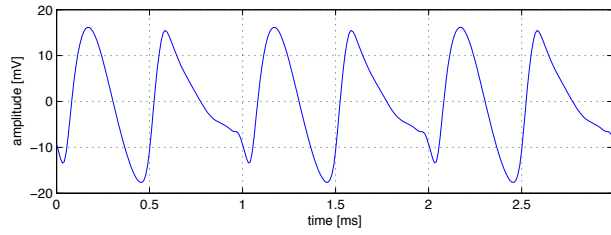
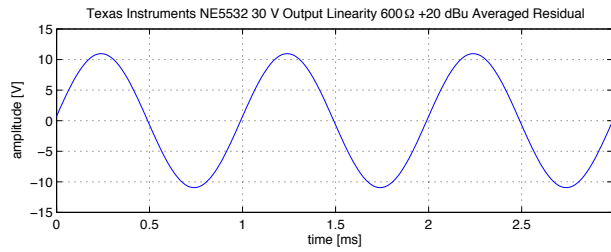
There are better opamps available nowadays but for less demanding applications still a valid option if common-mode and output loading effects can be addressed. Cost-performance ratio is very good considering the low price tag.

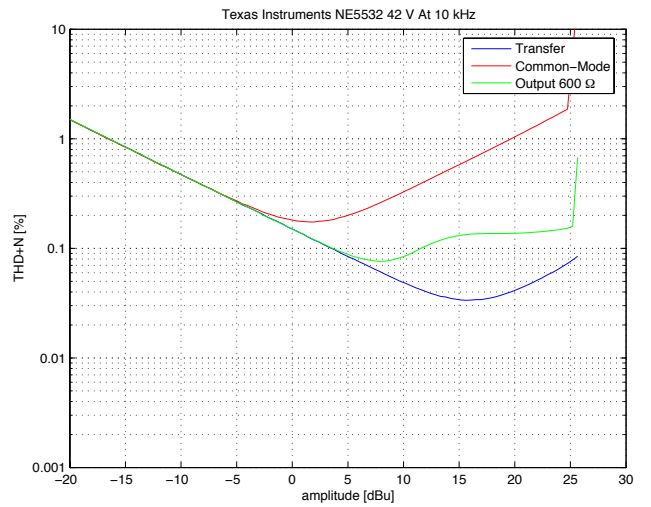
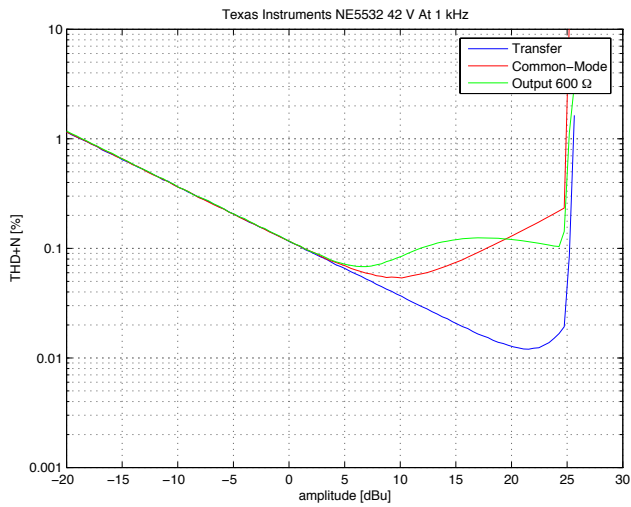
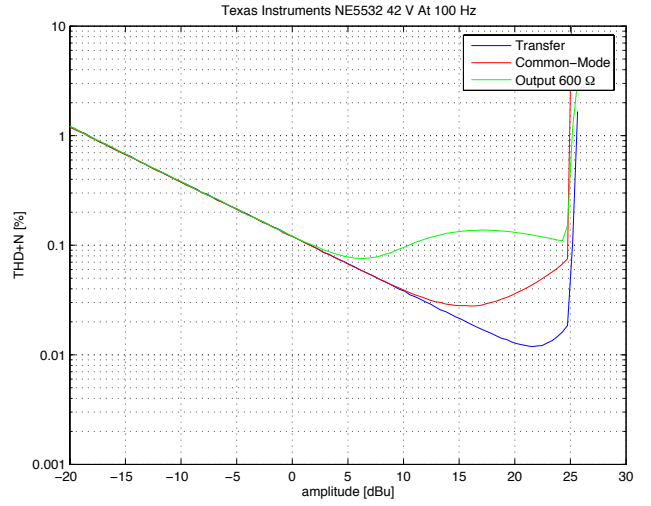
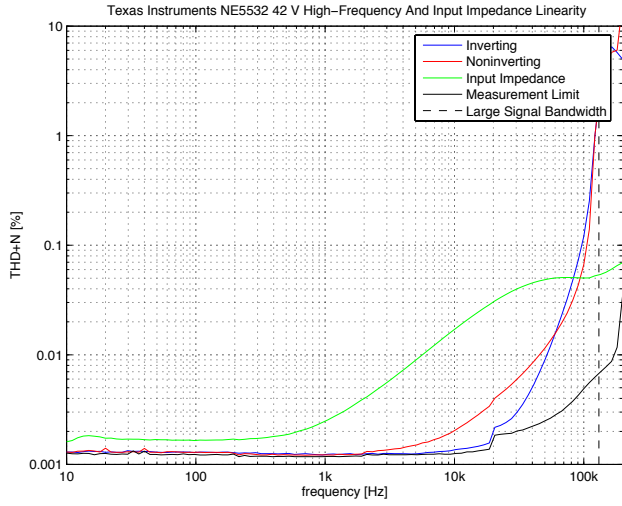
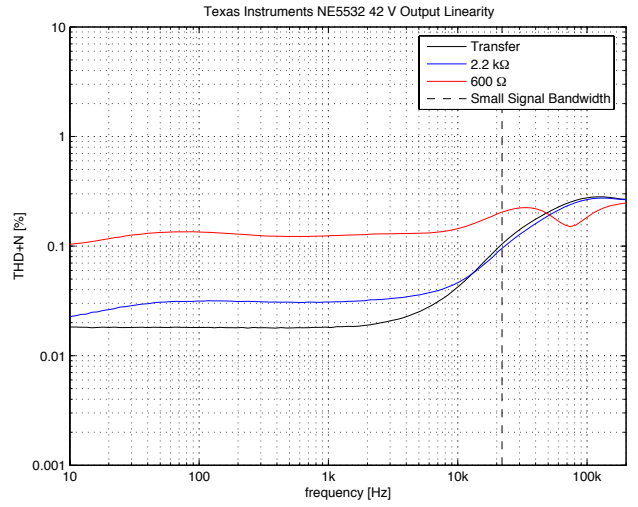
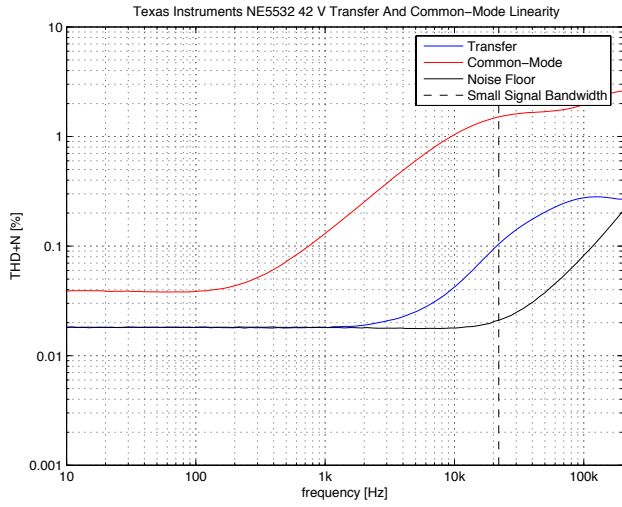
<sup>7</sup>Current noise is specified as almost equivalent though, which suggests that the NE5532 uses a degenerated input stage. This is confirmed by the higher slew-rate compared with a unity-gain compensated NE5534.

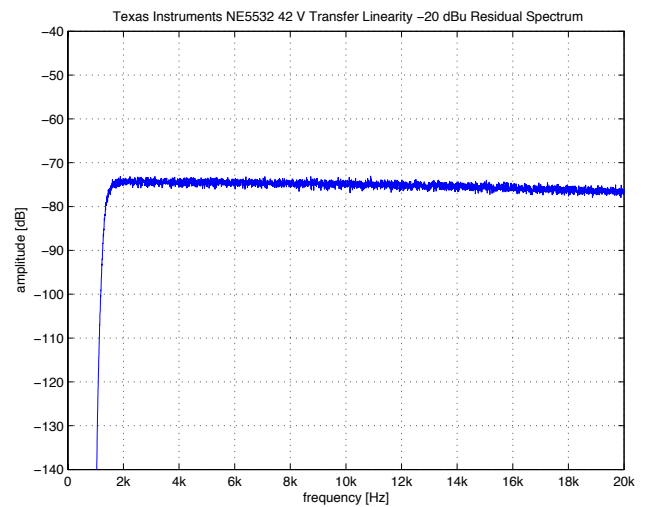
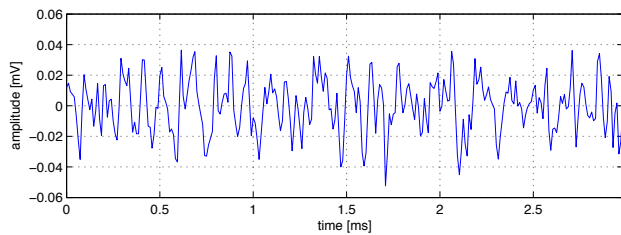
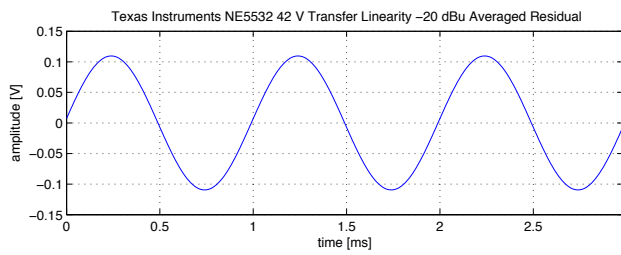
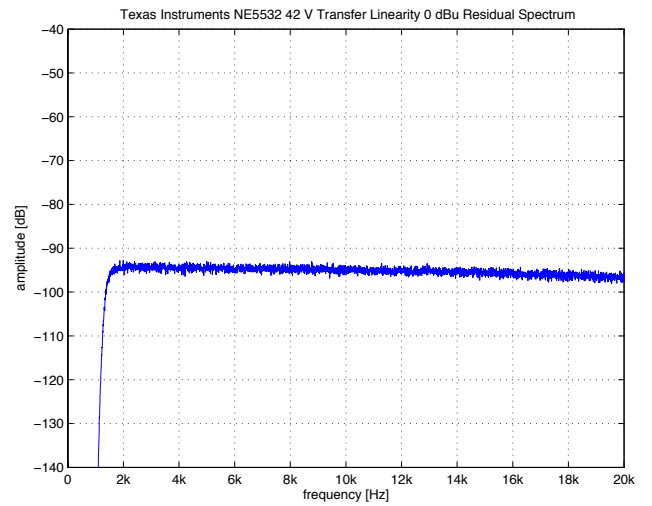
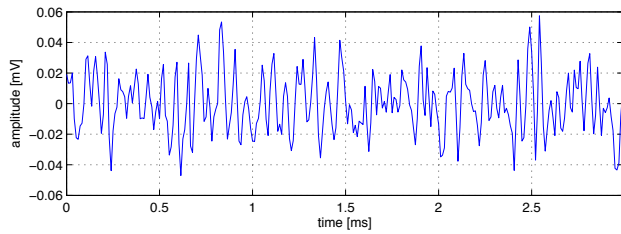
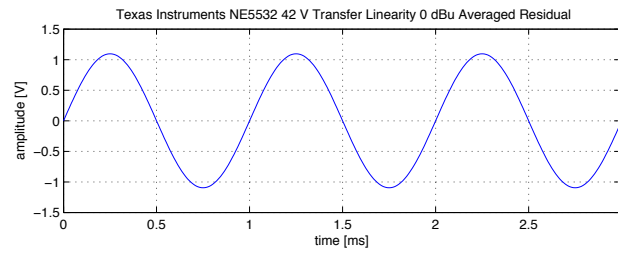
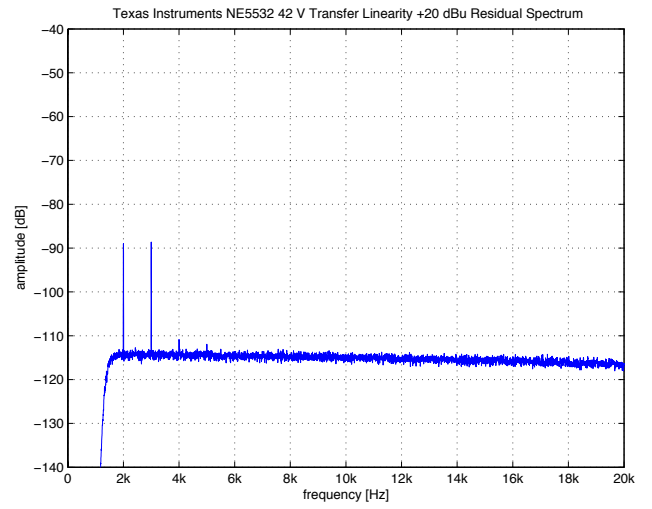
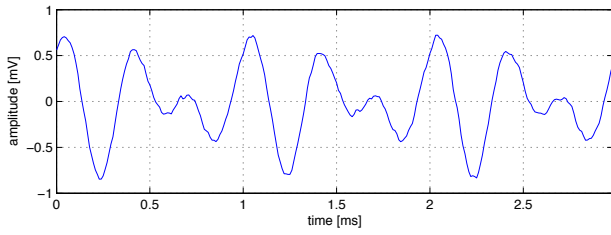
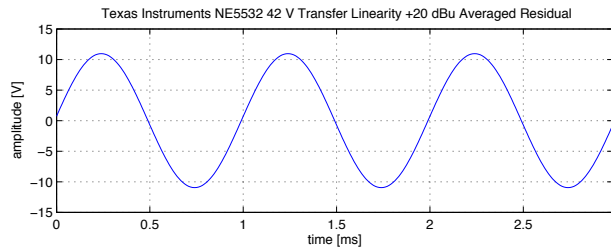




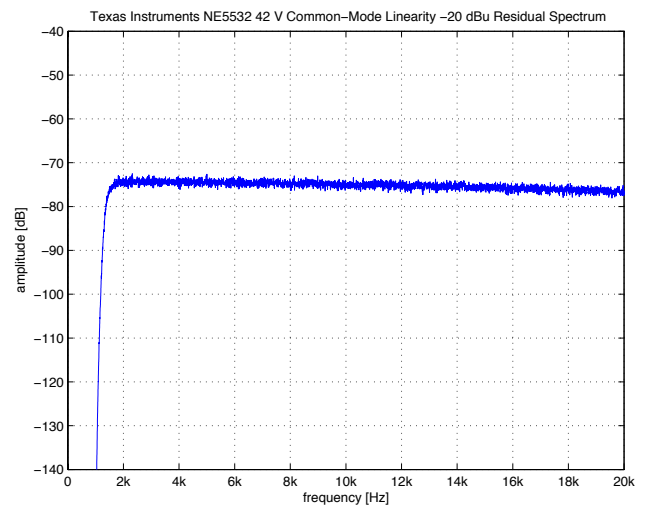
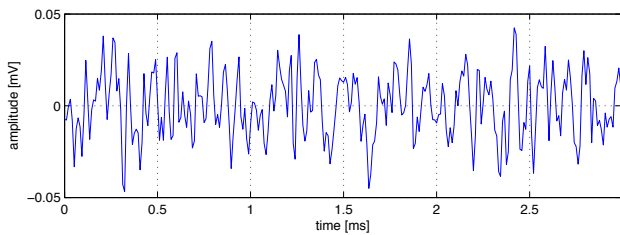
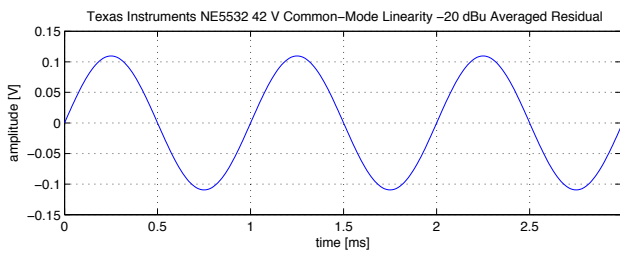
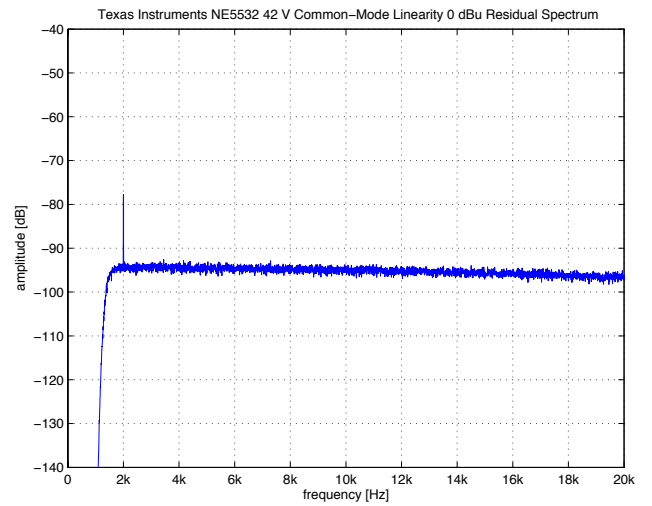
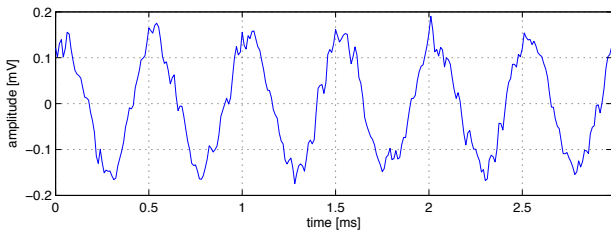
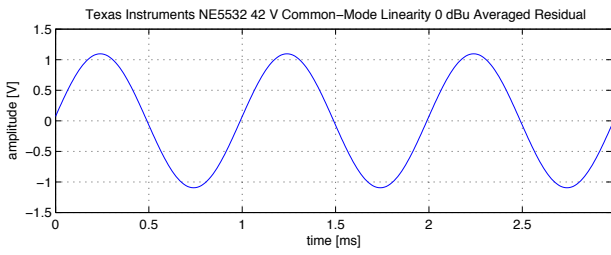
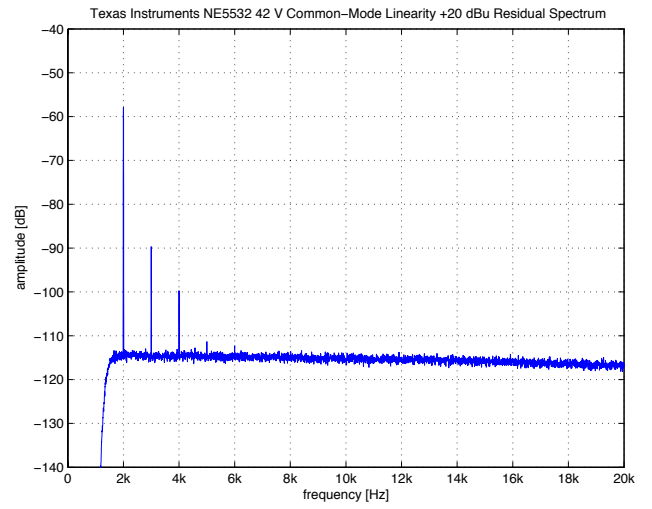
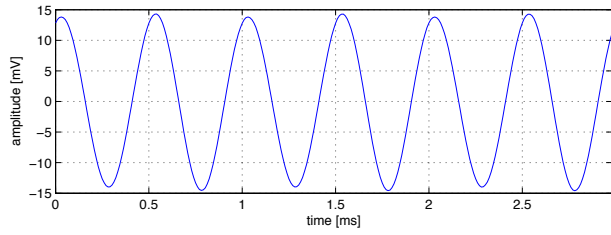
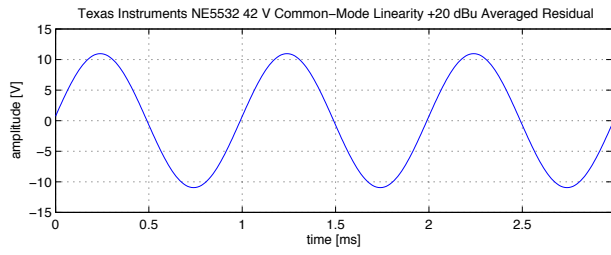


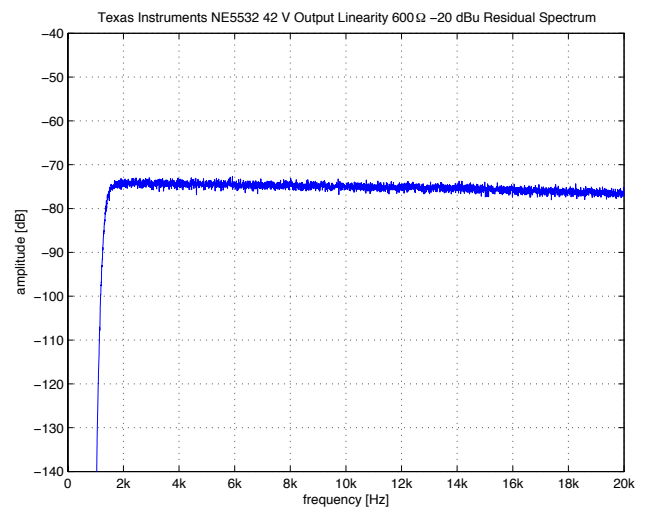
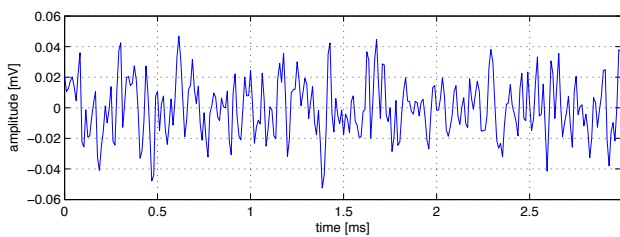
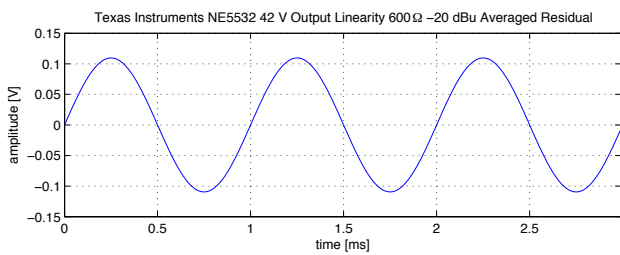
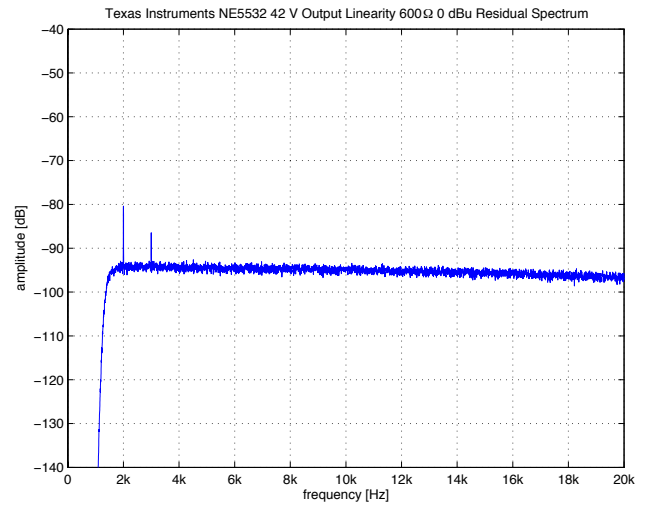
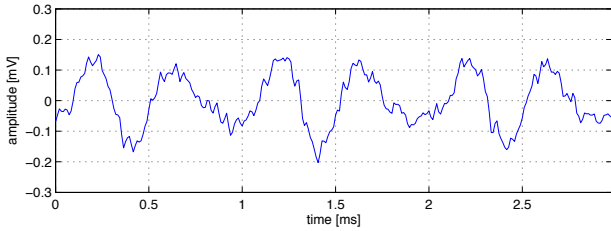
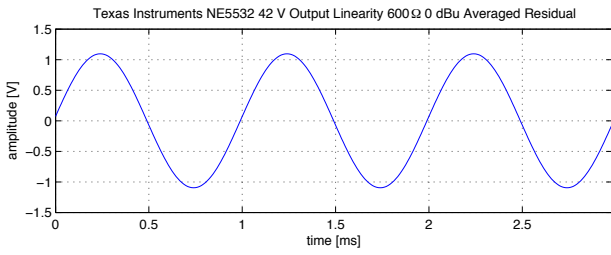
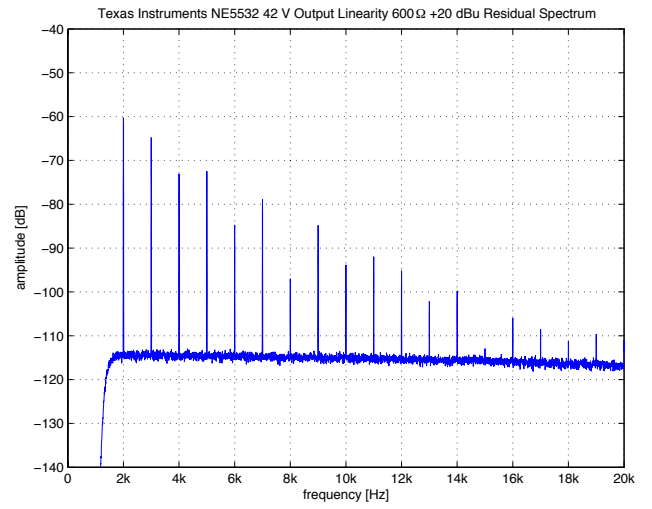
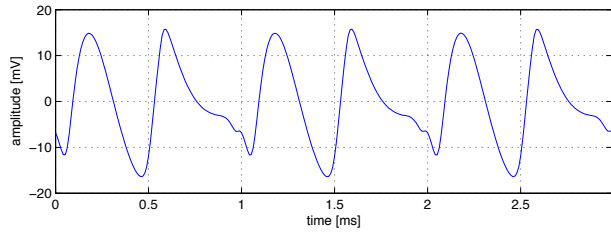
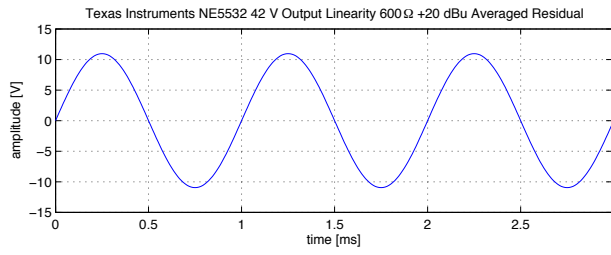












### 3.21 Texas Instruments NE5534

<b>Number of Channels</b>	1
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	0.58 US\$ at 1k units (August 2008)

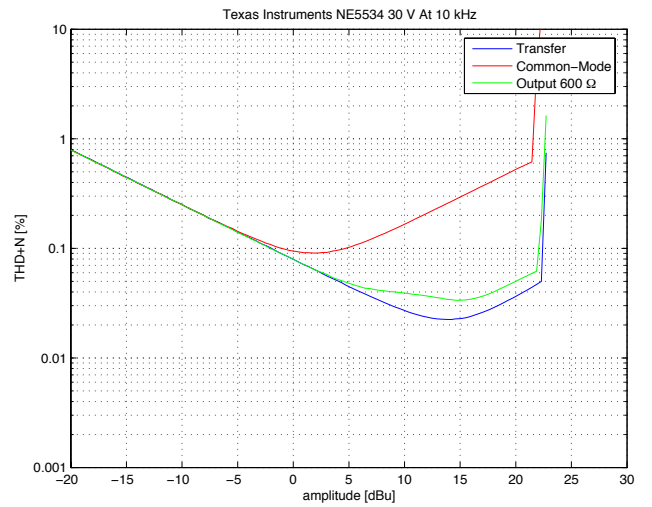
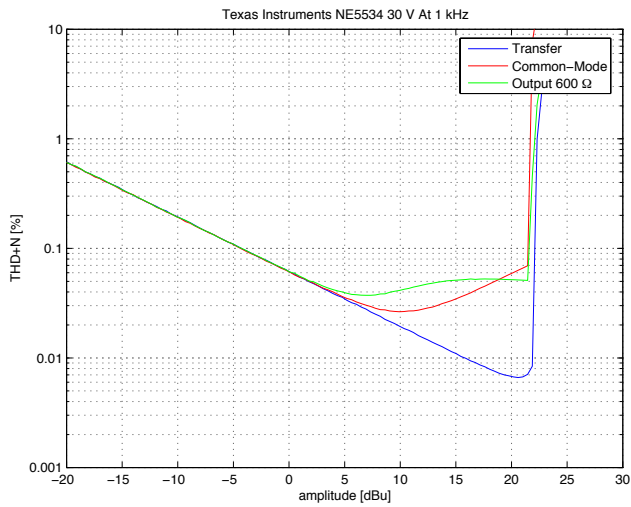
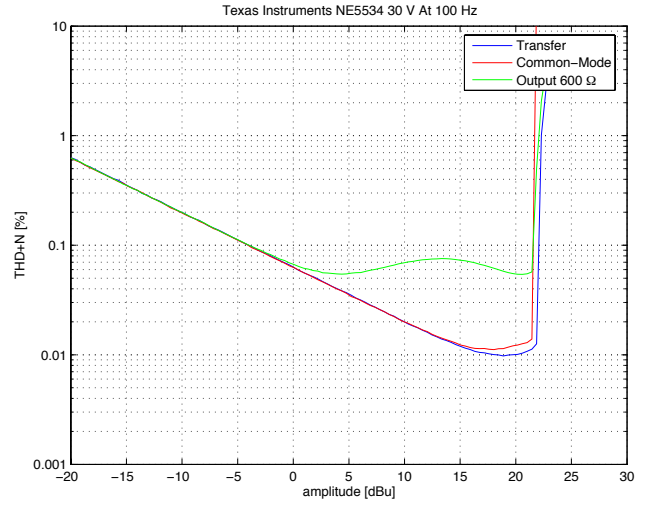
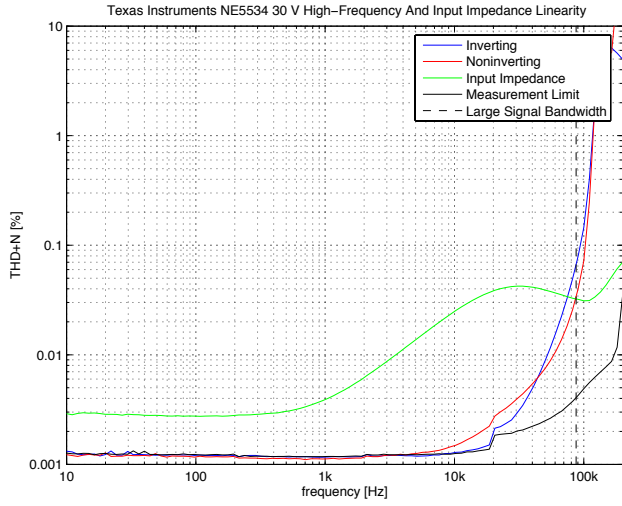
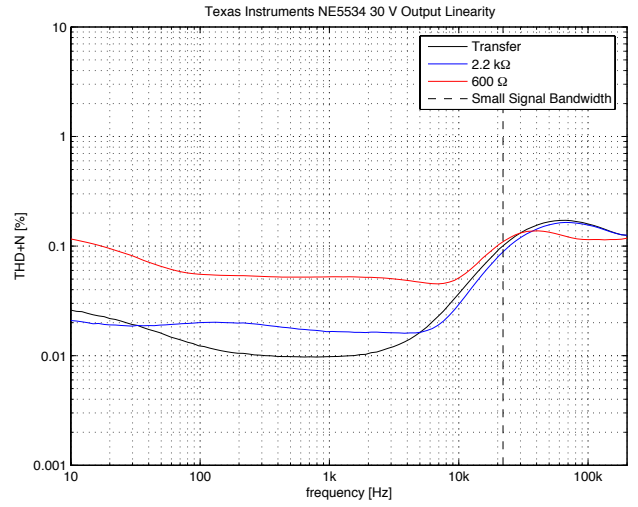
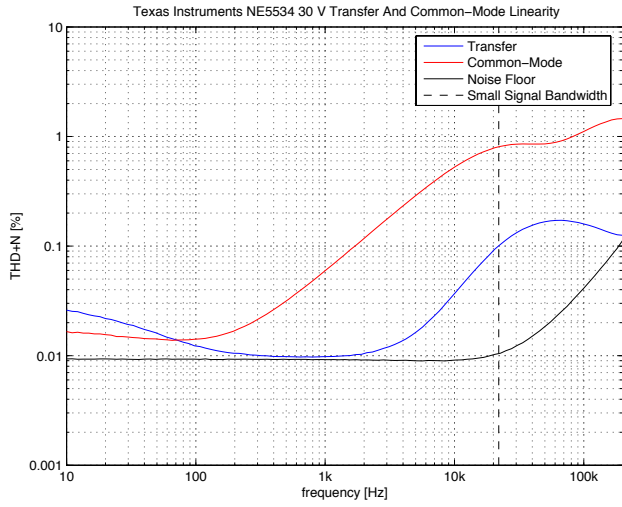
Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		0.5	4	mV
Input Bias Current		500	1500	nA
Input Offset Current		20	300	nA
Gain Bandwidth Product		22		MHz
Slew-Rate		6		V/ $\mu$ S
Input Voltage Noise (f = 1 kHz)		4		nV/ $\sqrt{\text{Hz}}$
Input Current Noise (f = 1 kHz)		0.6		pA/ $\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 12$	$\pm 13$		V
Output Voltage Swing ( $R_L = 600 \Omega$ )	$\pm 12$	$\pm 13$		V
Power Supply Voltage	$\pm 3$		$\pm 22$	V
Quiescent Current per Amplifier		4	8	mA

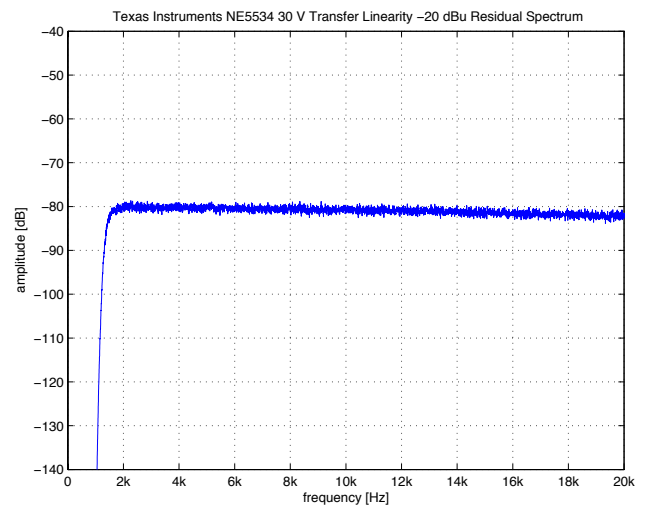
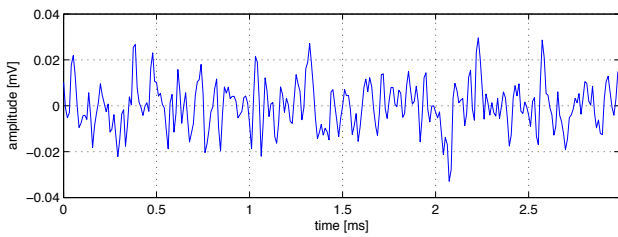
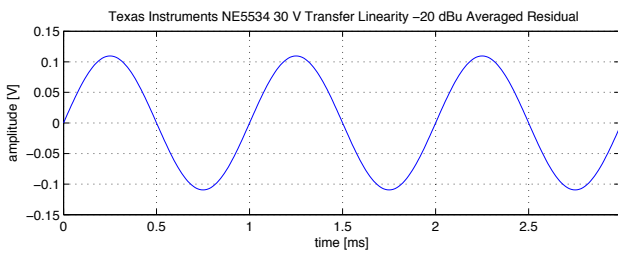
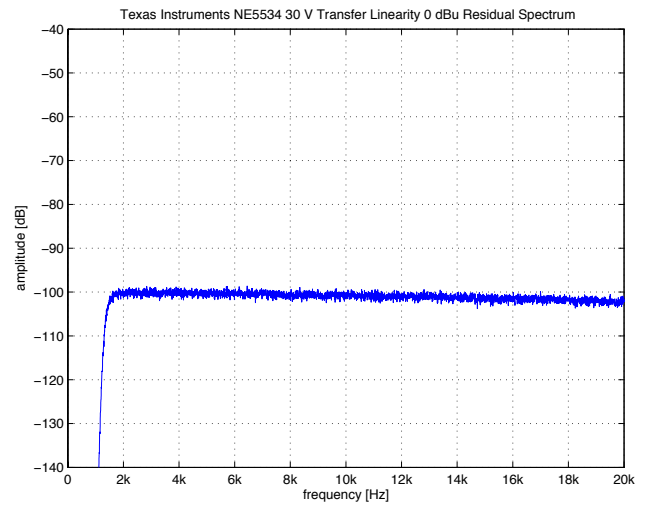
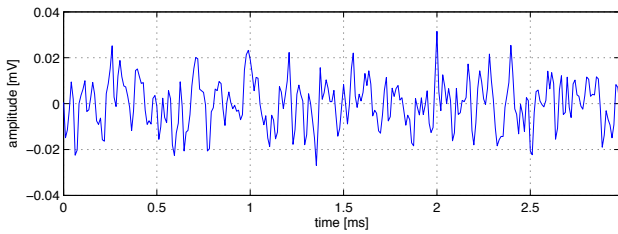
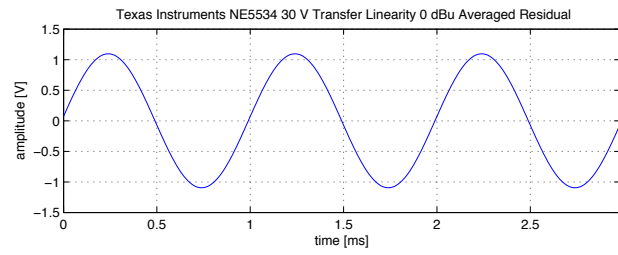
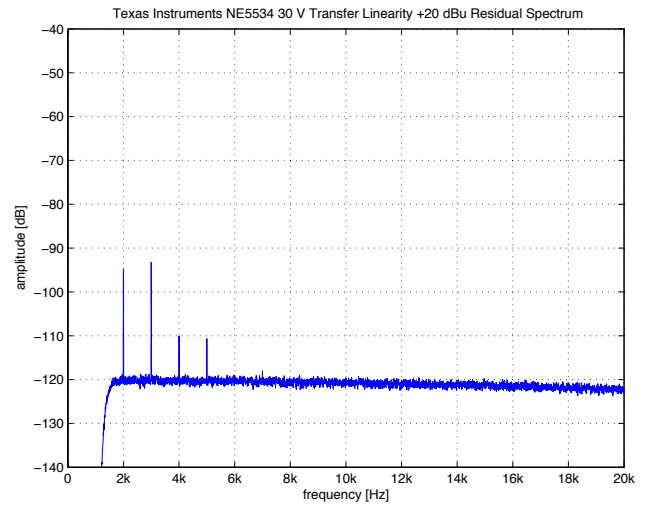
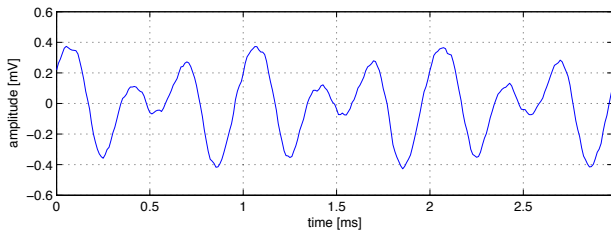
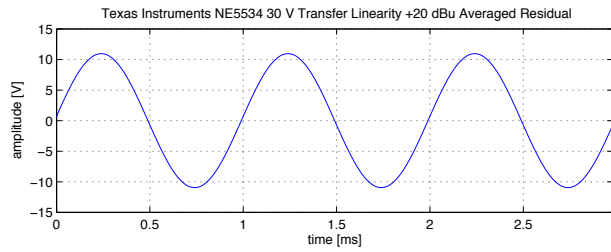
Table 3.21: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 15 \text{V}$  and  $C_{\text{COMP}} = 22 \text{pF}$ .

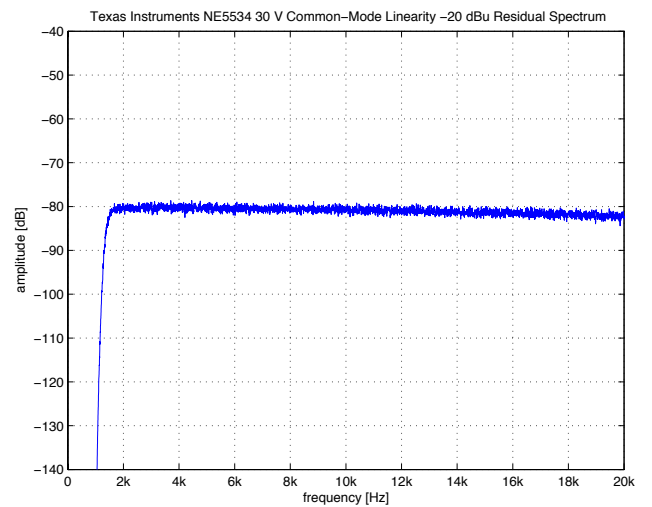
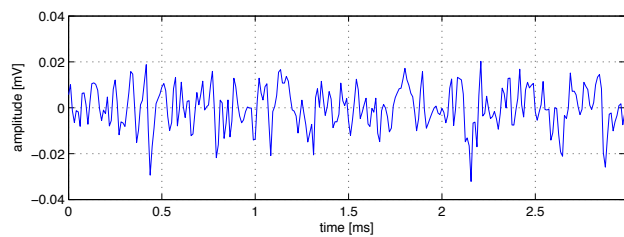
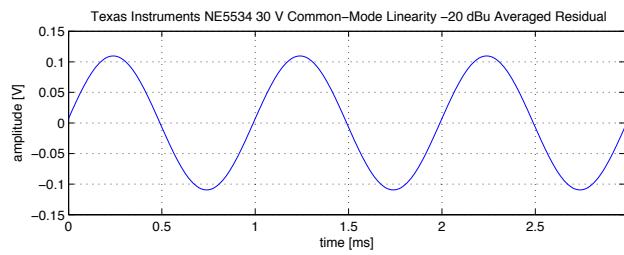
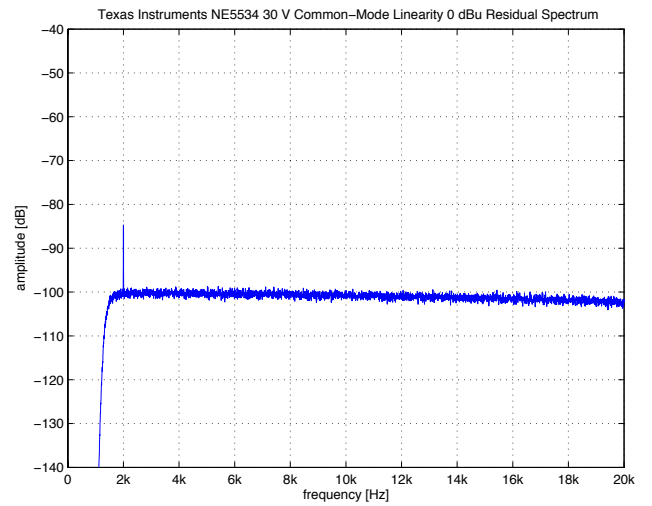
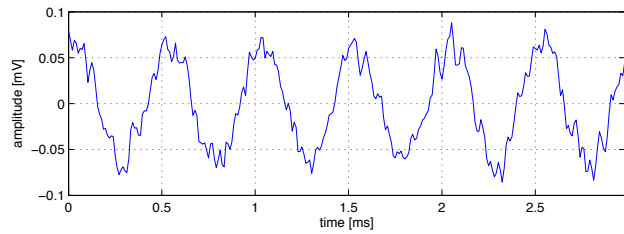
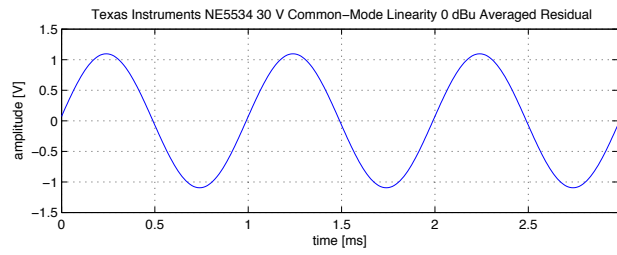
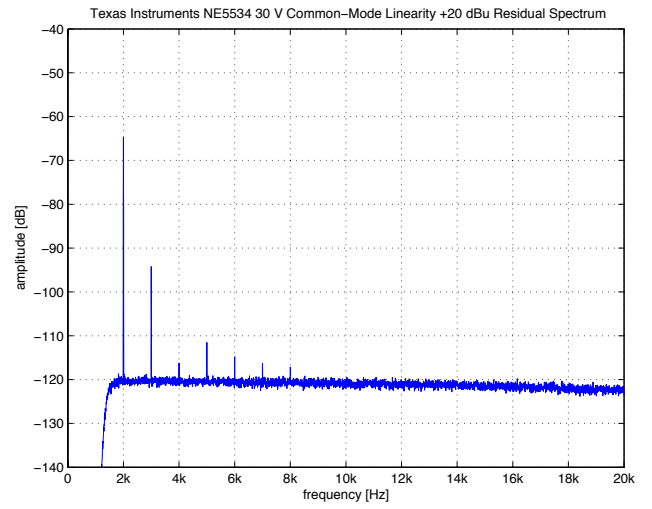
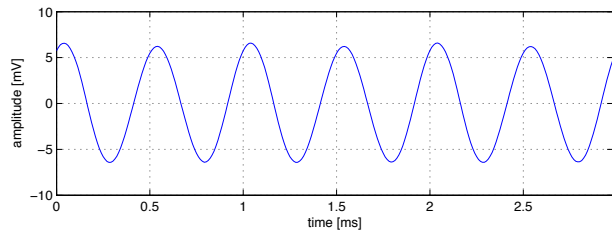
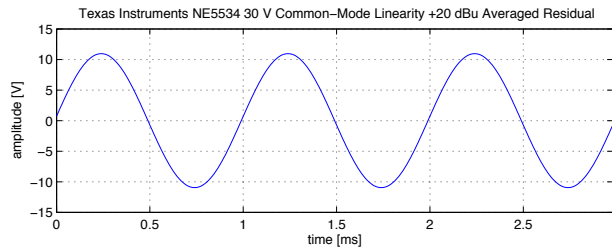
An externally compensated amplifier based on a three-stage topology with bipolar input stage. An equivalent internally compensated dual amplifier is available as NE5532 (see page 148). Voltage noise is comparatively low, at medium-low current noise. Trimming pins are available.

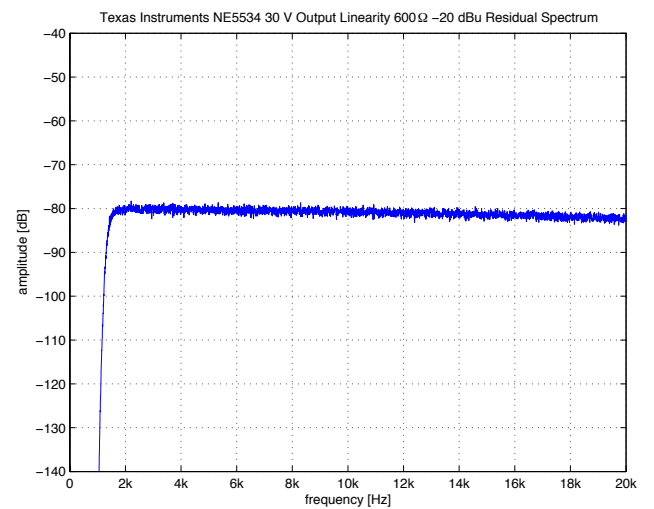
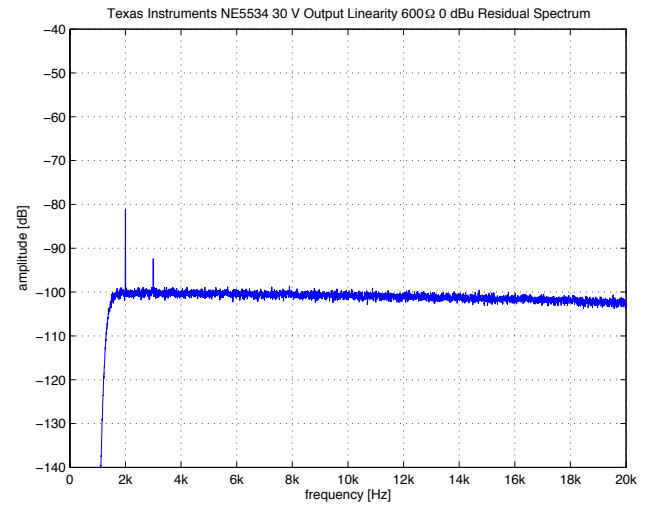
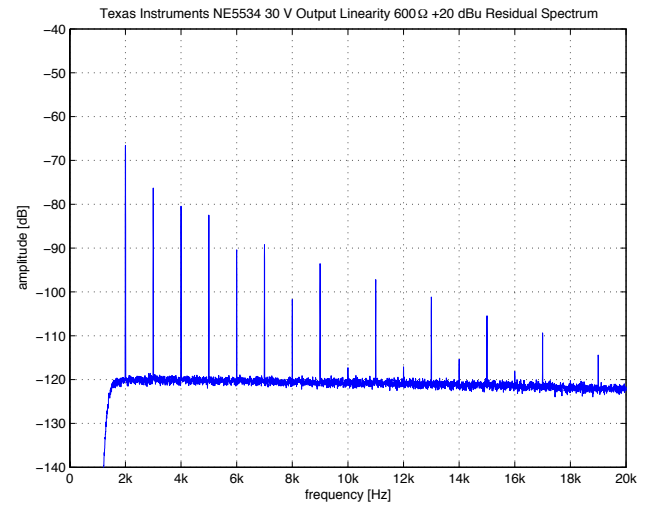
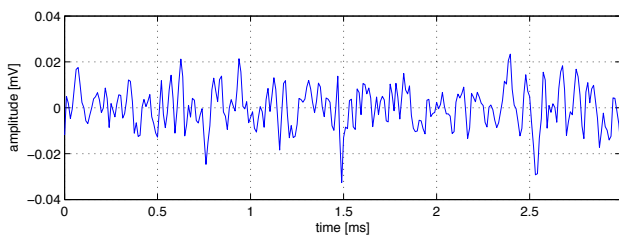
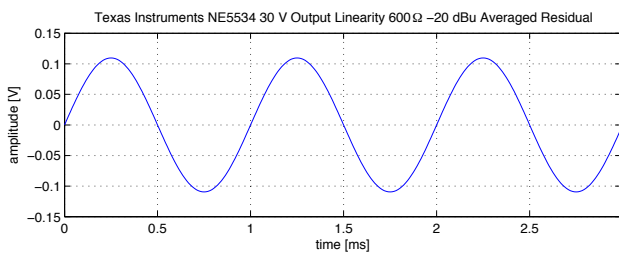
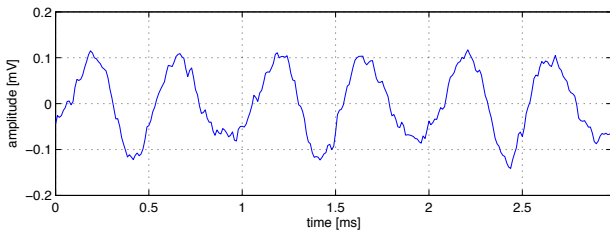
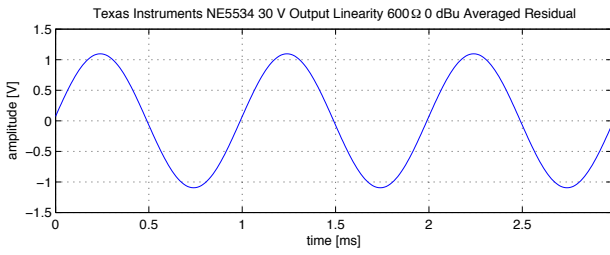
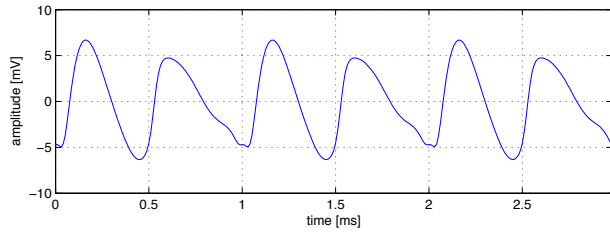
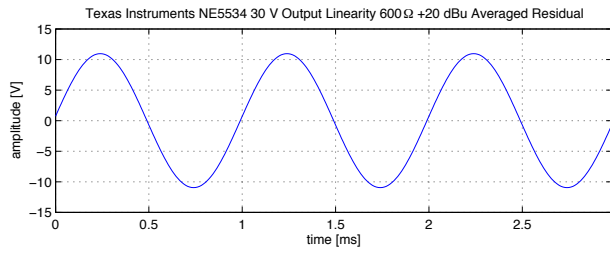
The distortion performance is similar to the NE5532; noticeable exceptions are the somewhat better high frequency distortion (although the NE5532 has a higher slew-rate specification) and the unconventional low-frequency rise in transfer distortion. Higher supply voltages do not help performance, except for the input impedance linearity.

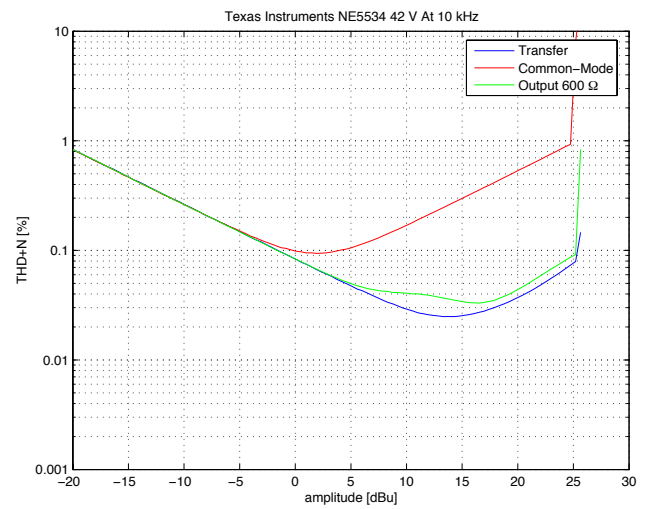
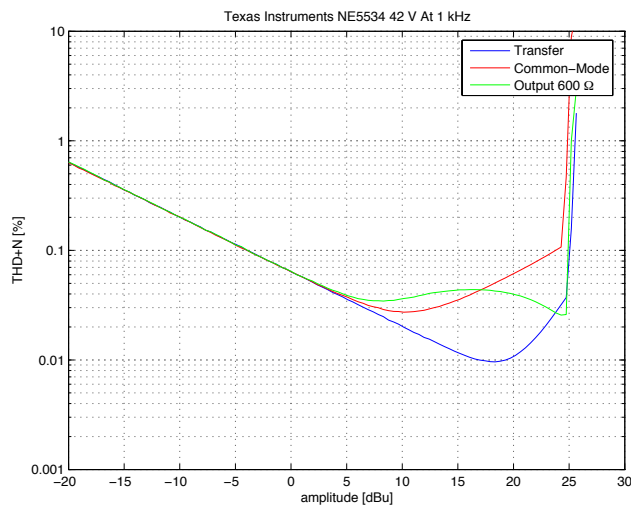
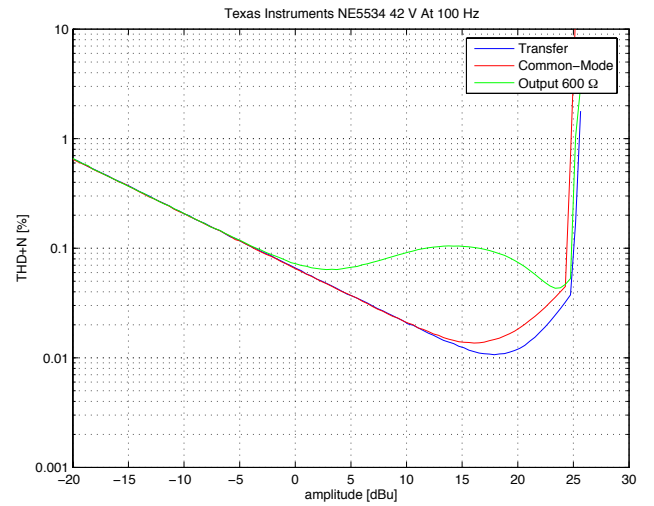
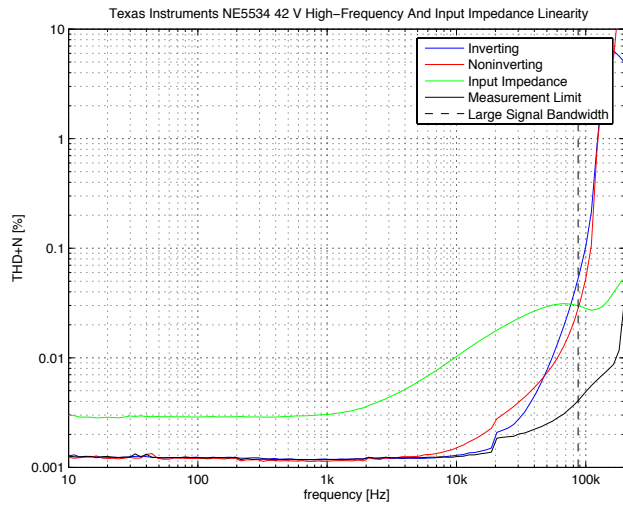
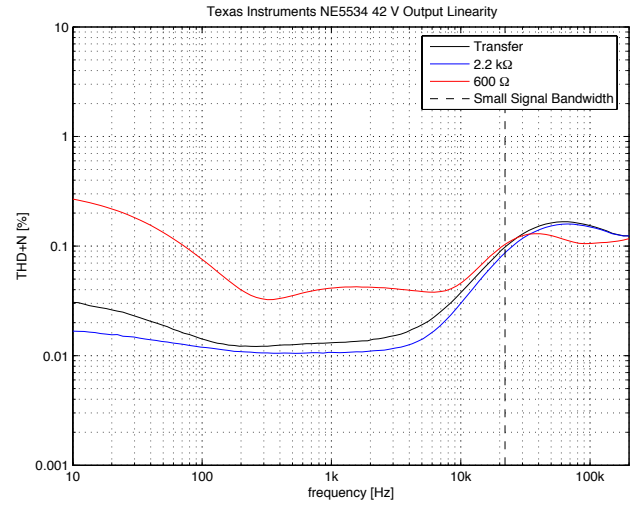
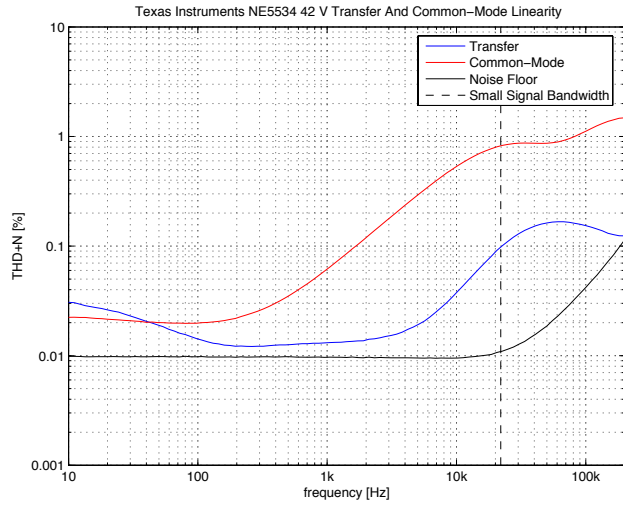
As the cost of the NE5534 is more than twice that of a dual NE5532 its use will usually only be justified for applications where the lower noise, the external compensation or the trimming feature decisively improves system performance.



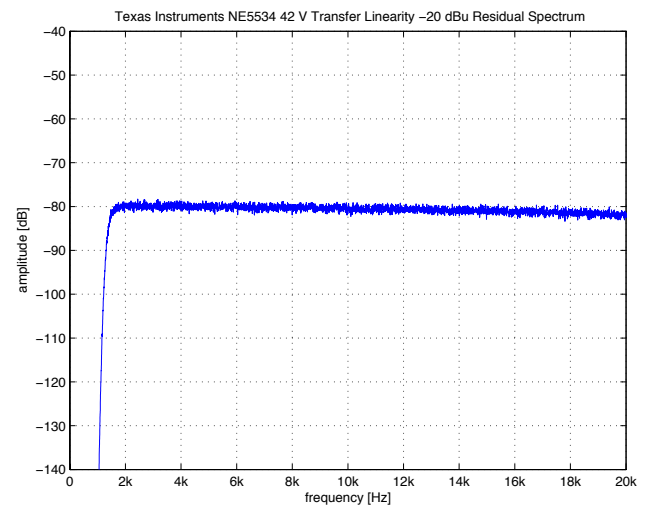
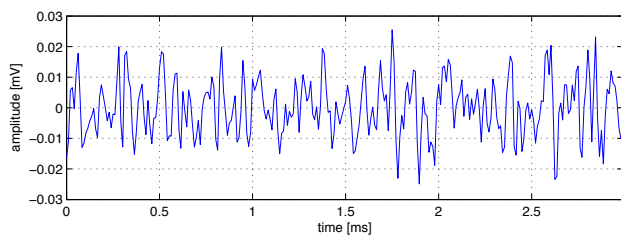
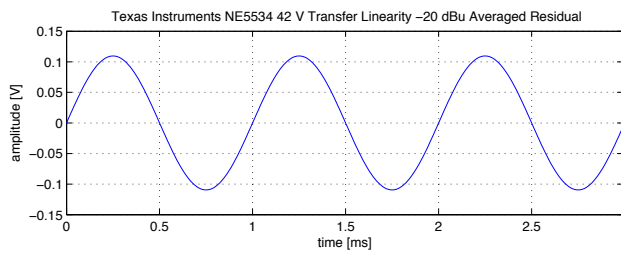
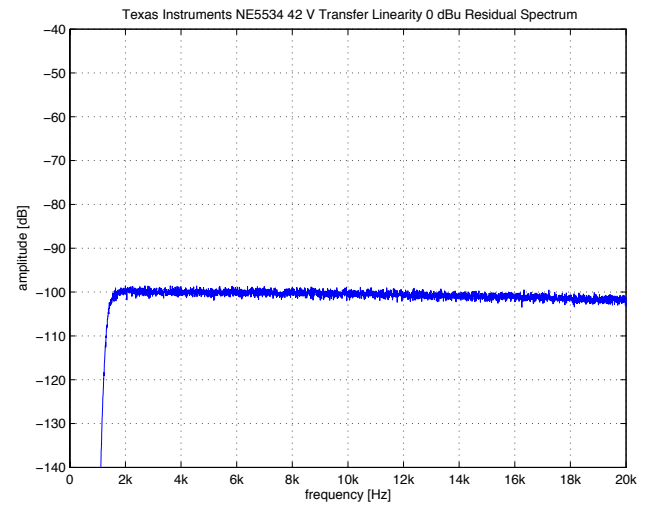
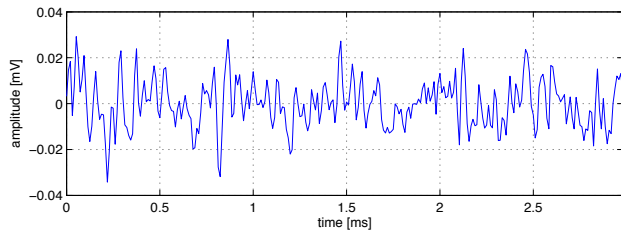
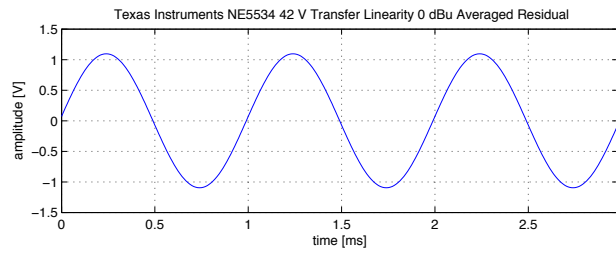
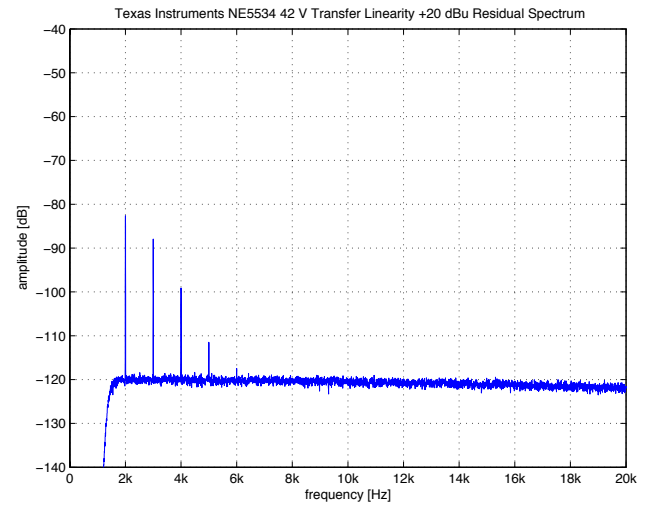
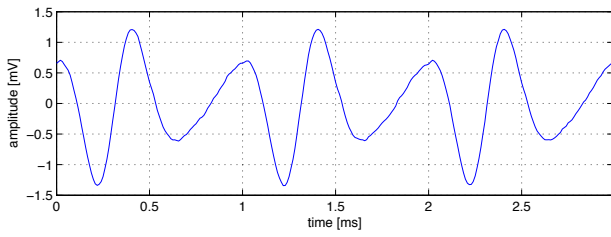
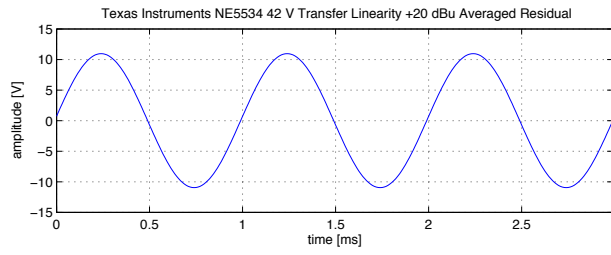


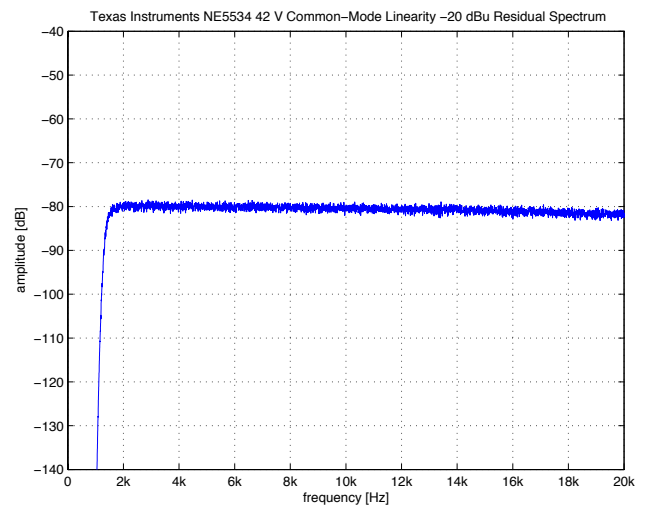
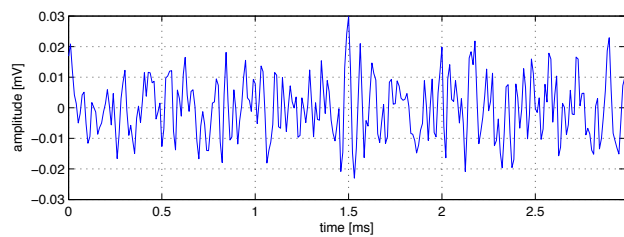
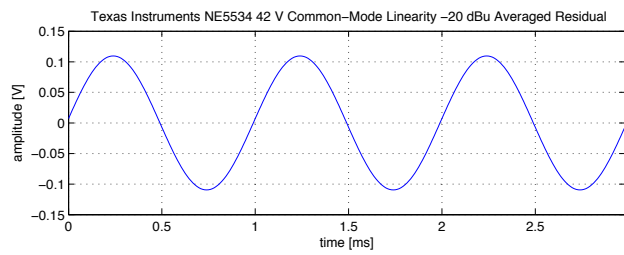
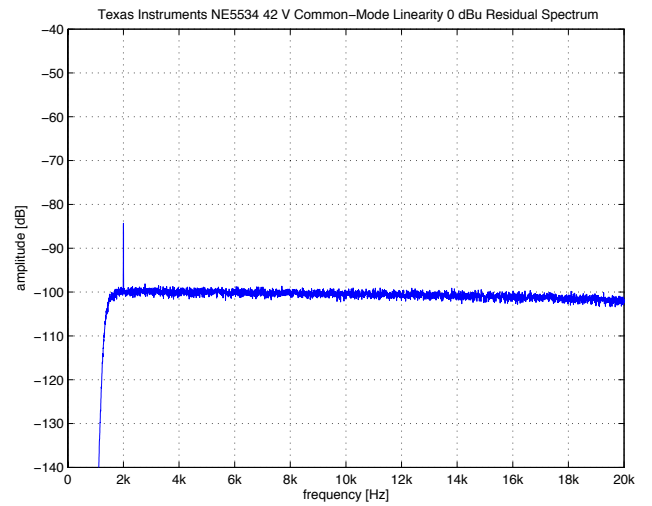
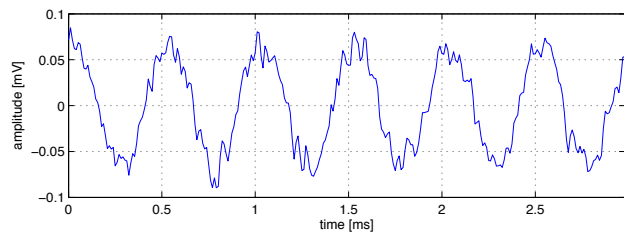
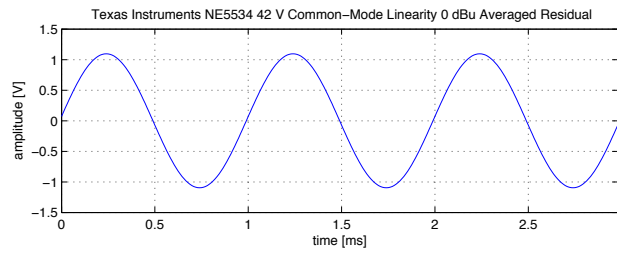
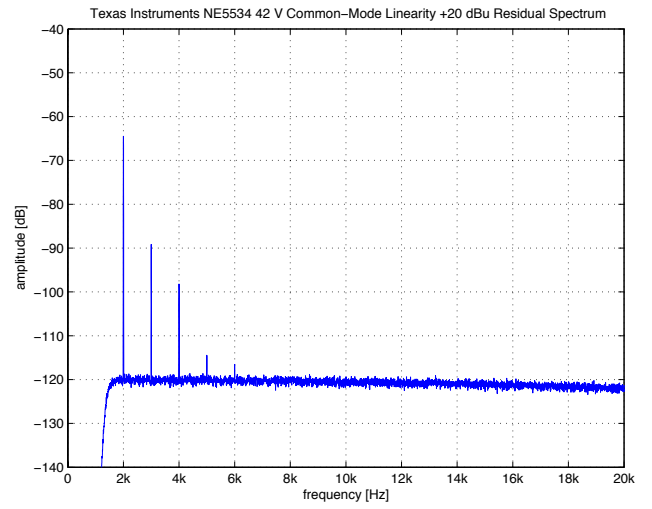
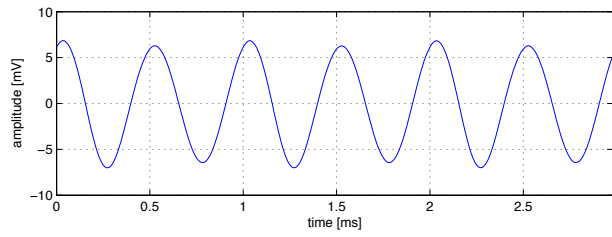
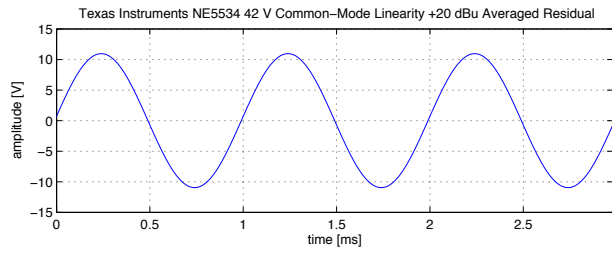


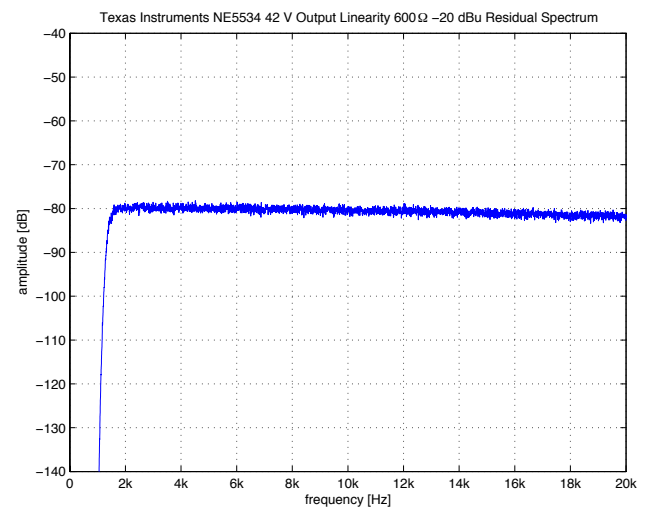
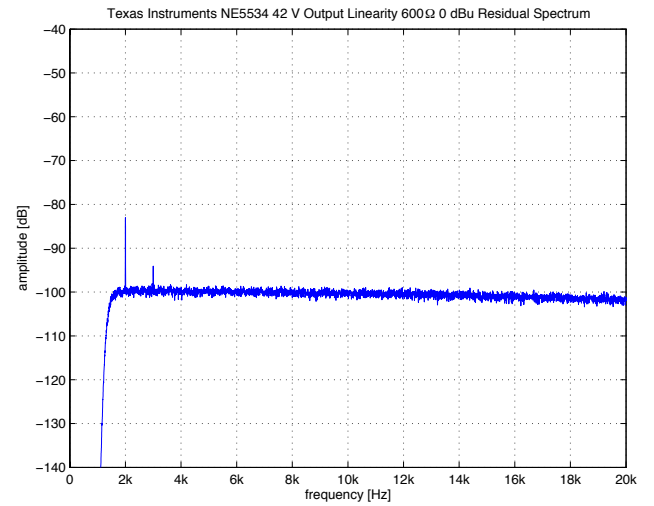
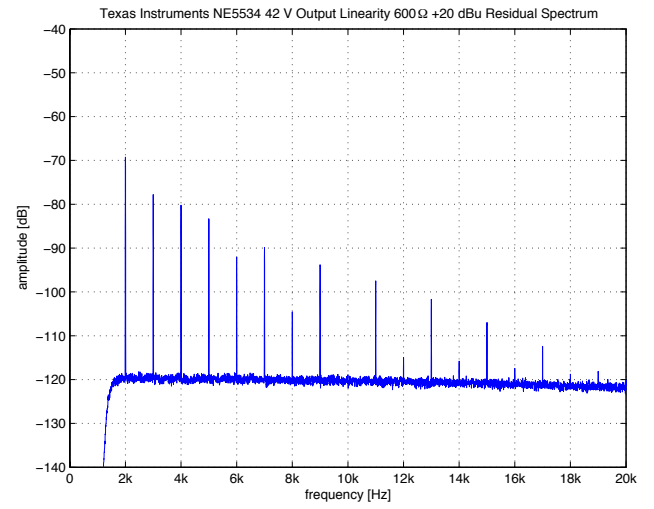
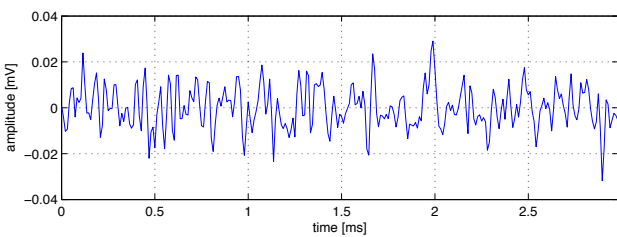
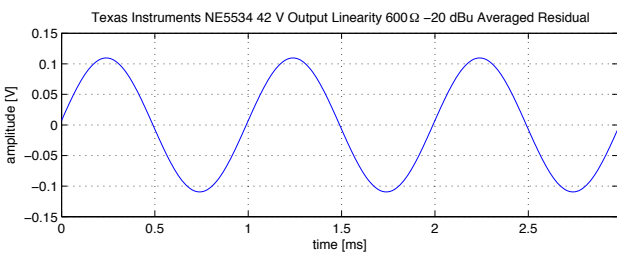
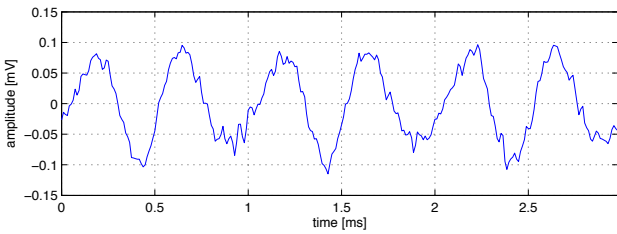
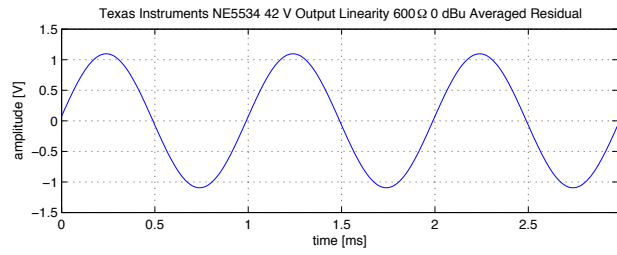
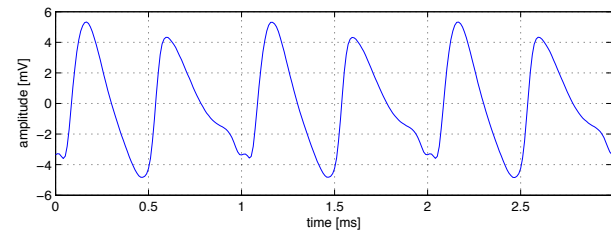
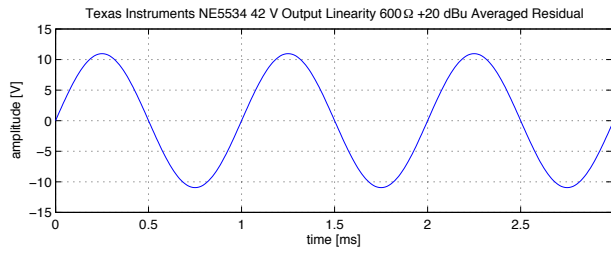












### 3.22 Texas Instruments OPA551

<b>Number of Channels</b>	1
<b>Packages</b>	DIP, SOIC, DPAK
<b>Cost per Amplifier</b>	1.90 US\$ at 1k units (August 2008)

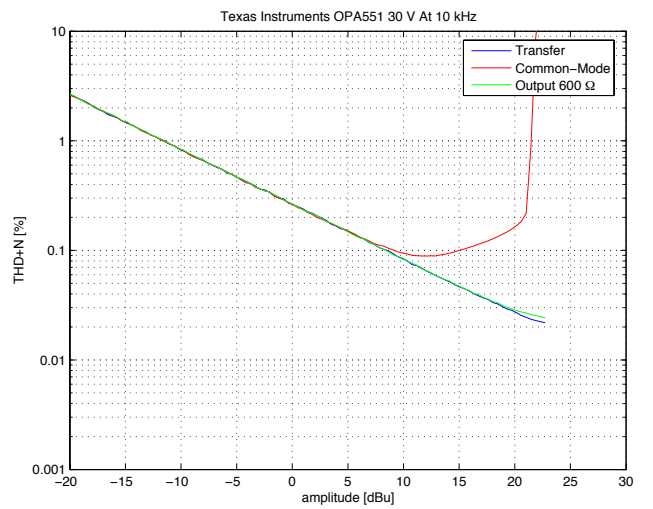
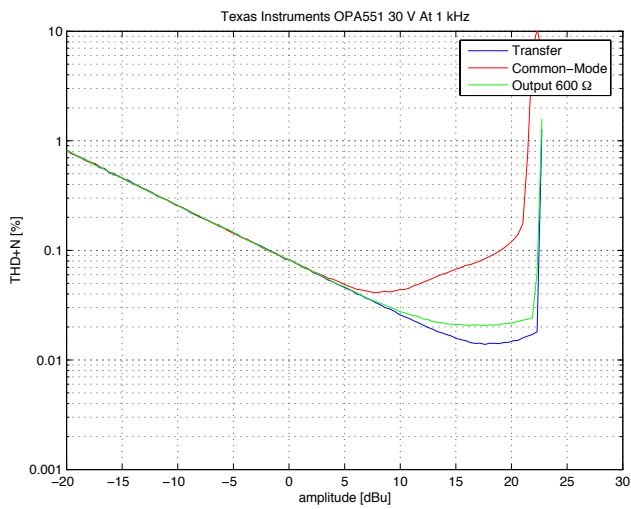
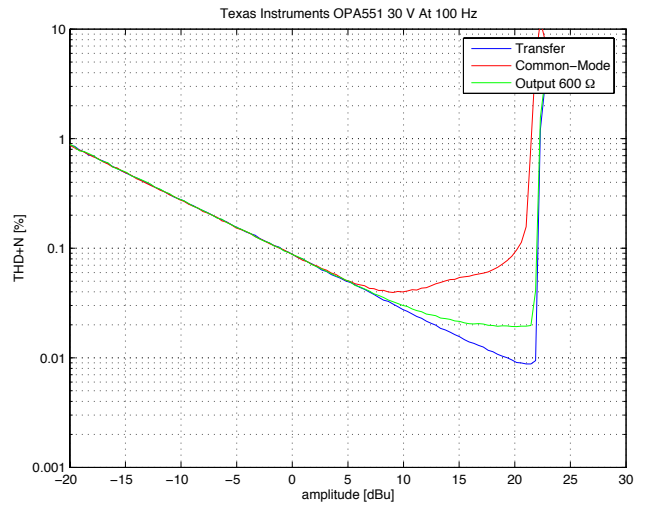
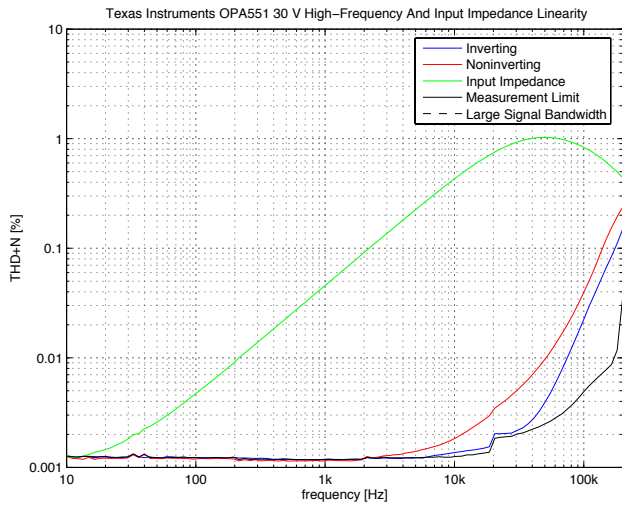
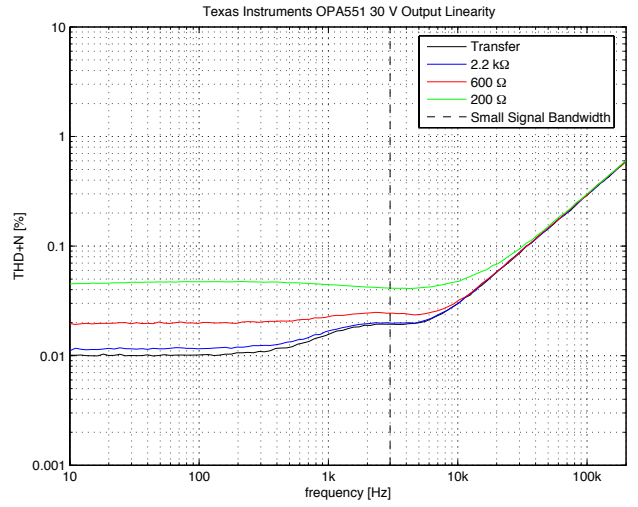
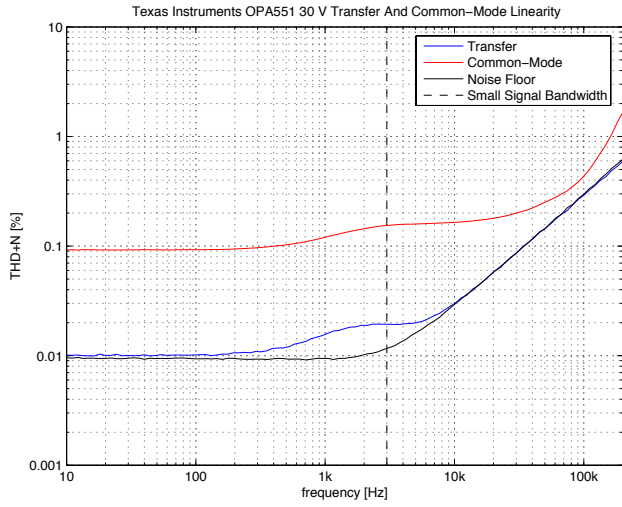
Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		1	3	mV
Input Bias Current		20	100	pA
Input Offset Current		3	100	pA
Gain Bandwidth Product		3		MHz
Slew-Rate		15		V/ $\mu$ S
Input Voltage Noise (f = 1 kHz)		14		nV/ $\sqrt{\text{Hz}}$
Input Current Noise (f = 1 kHz)		3.5		fA/ $\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 27.5$			V
Output Voltage Swing ( $I_{\text{OUT}} = 200$ mA)	$\pm 27$			V
Output Current	$\pm 200$			mA
Power Supply Voltage	$\pm 4$		$\pm 30$	V
Quiescent Current per Amplifier		7	8.5	mA

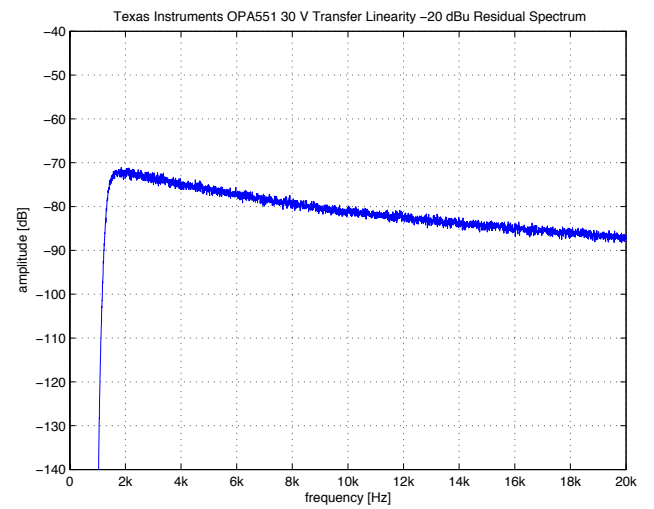
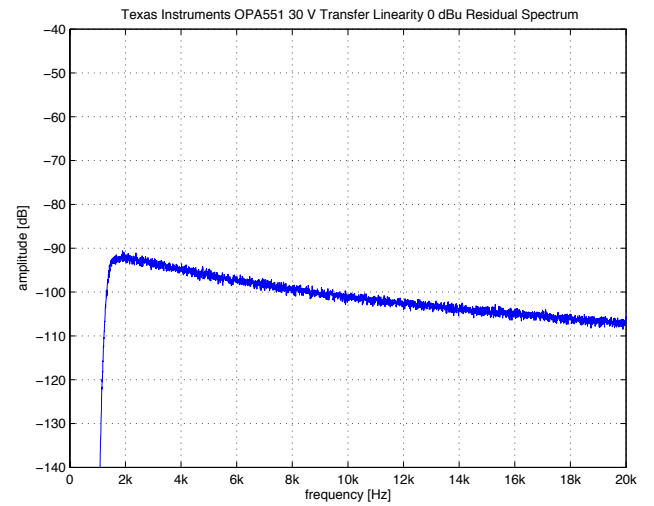
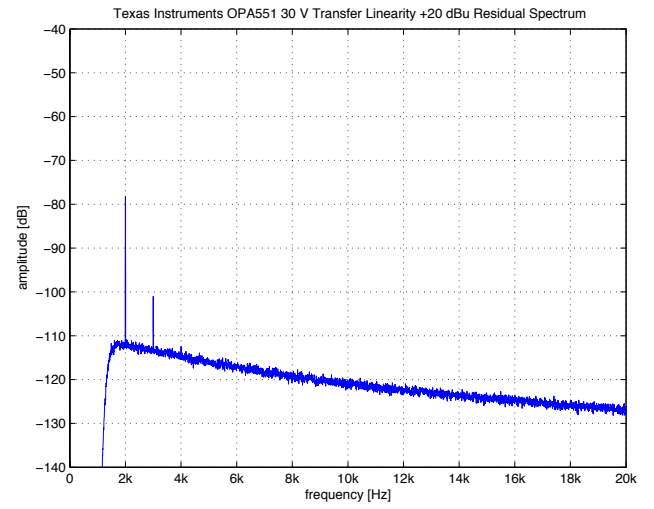
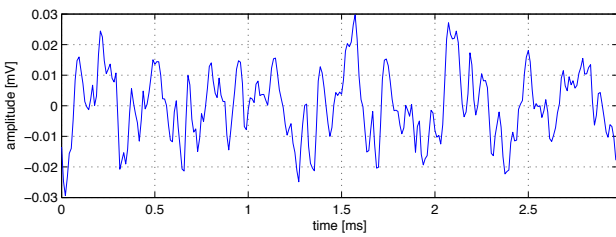
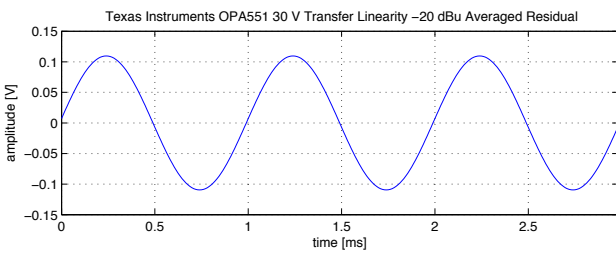
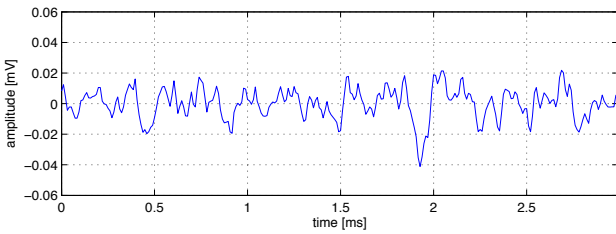
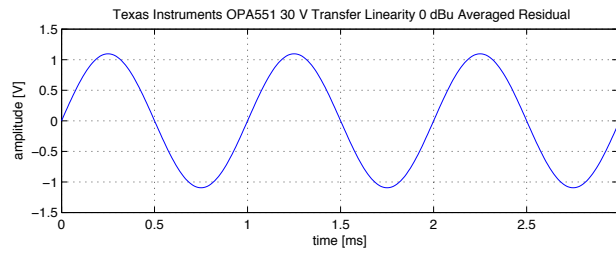
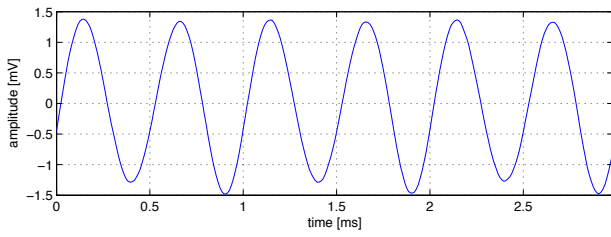
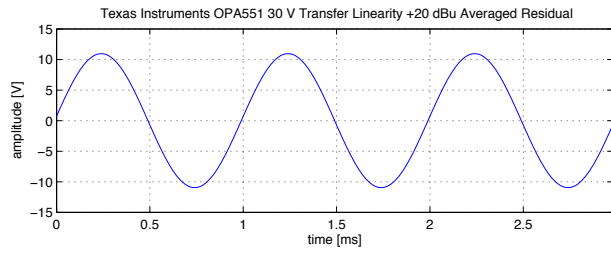
Table 3.22: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 30 \text{V}$ .

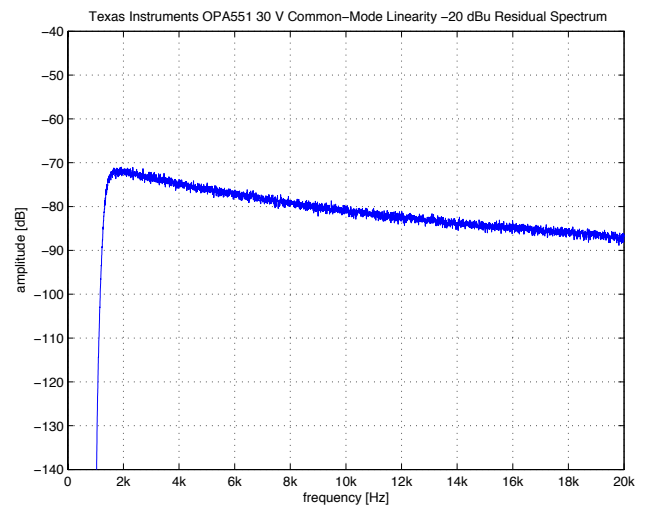
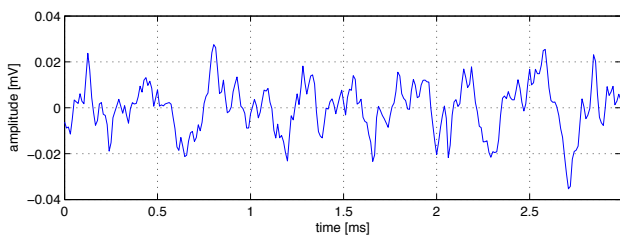
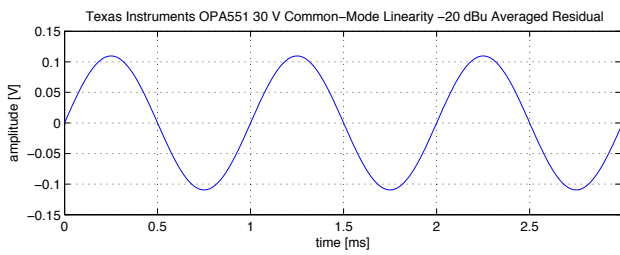
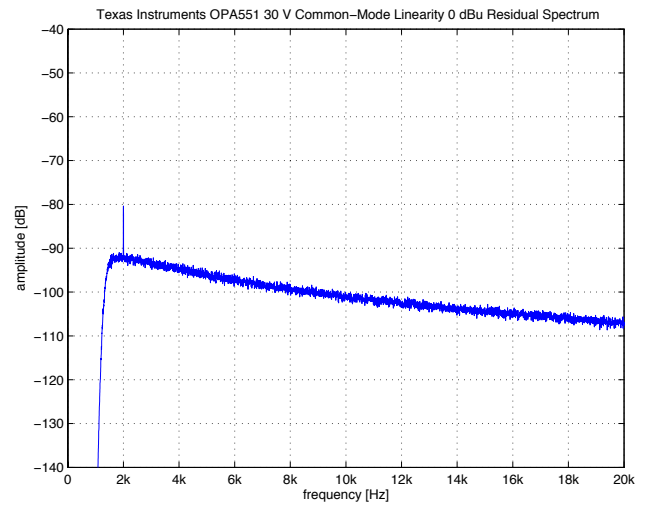
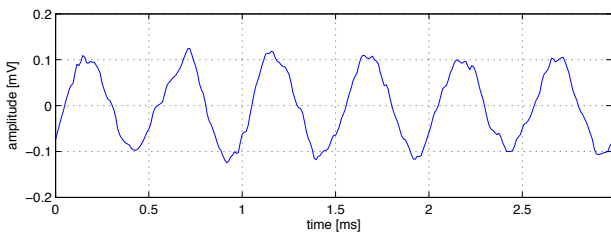
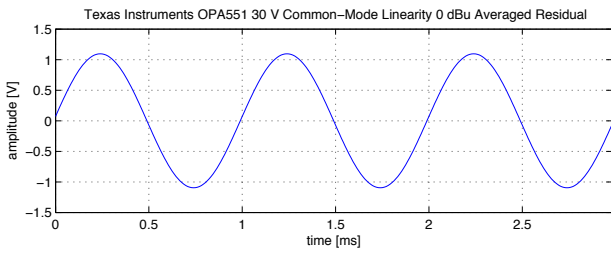
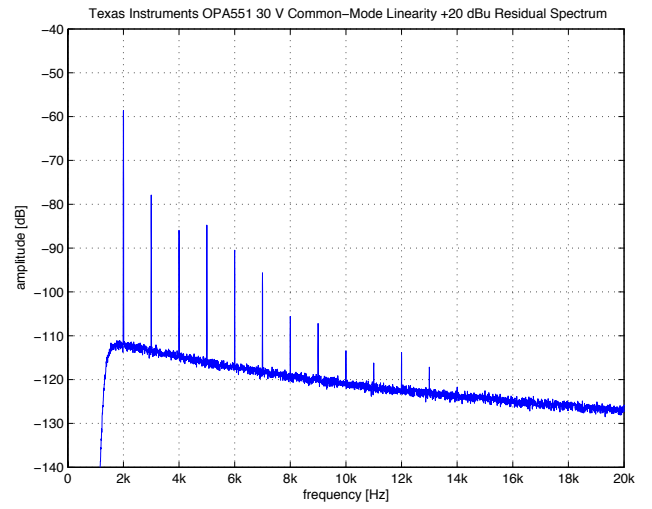
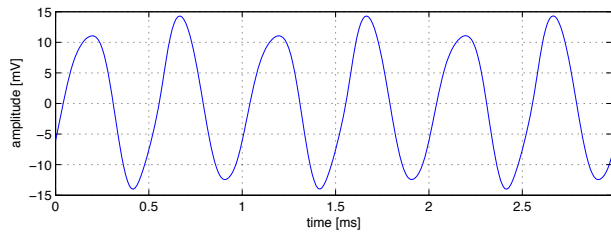
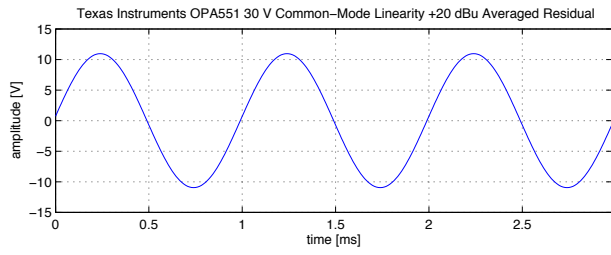
A single operational amplifier offering high maximum supply voltages and good load driving capabilities. No details on the architecture are published but the specifications show that JFET inputs must be used. Although the gain bandwidth product is rather low slew-rate is relatively high. Note weak voltage noise performance and high quiescent current. Thermal shut-down is indicated with a flag pin. A decompensated version (OPA552) is available.

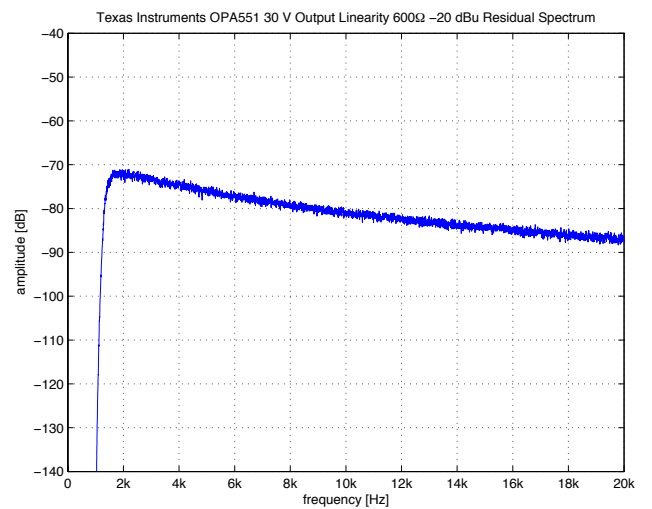
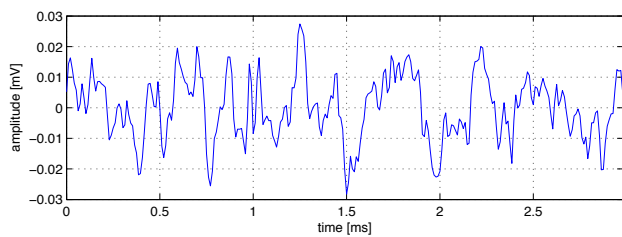
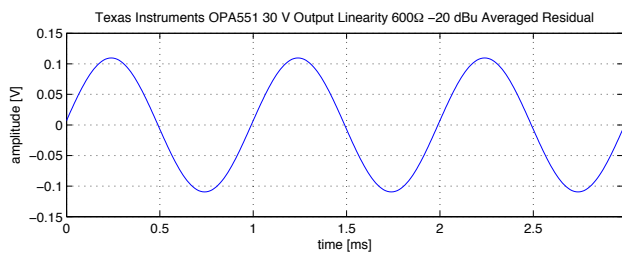
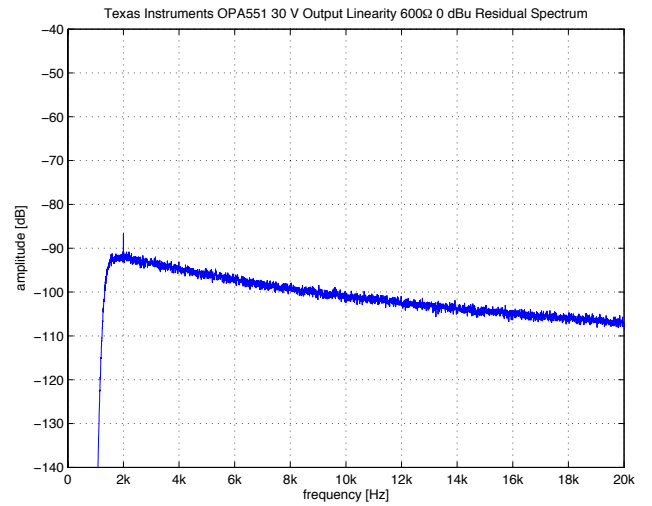
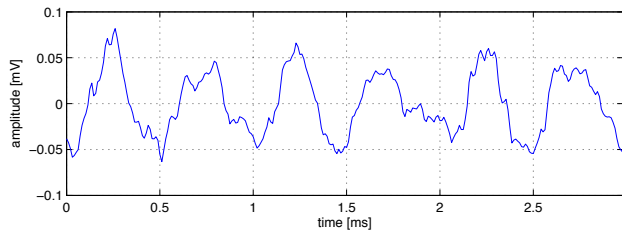
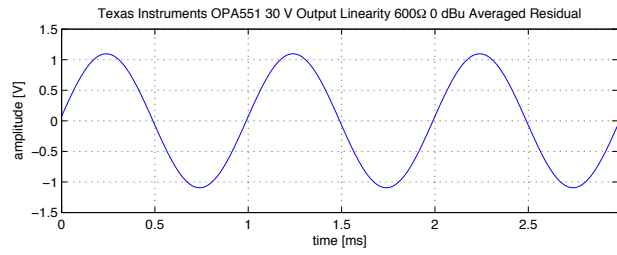
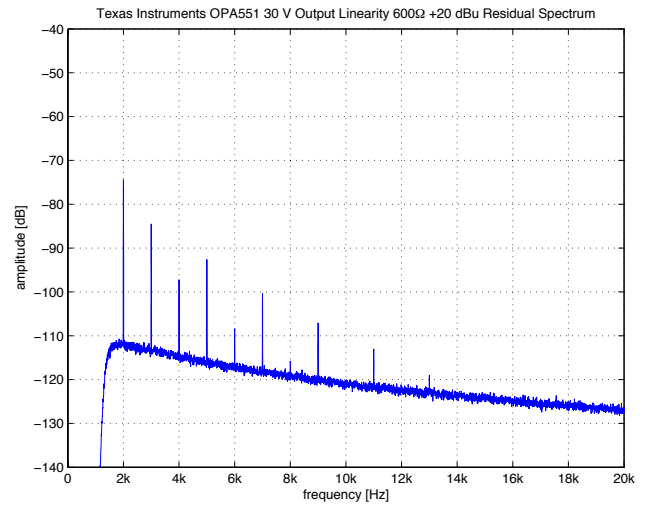
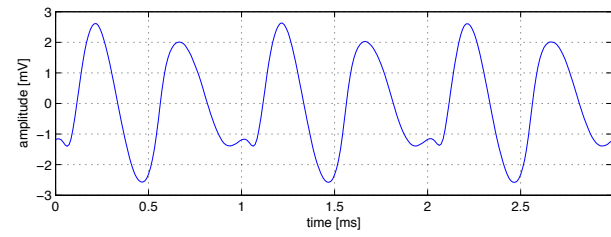
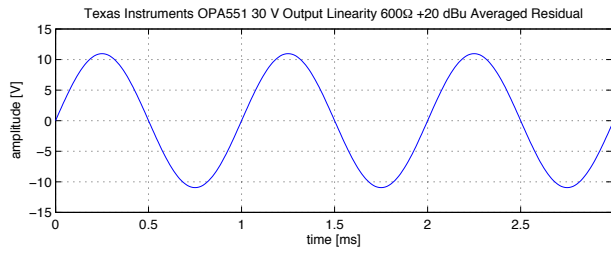
The basic transfer linearity is good within the audio band—some slew-induced high-frequency distortion is observable however. Distortion from output loading is remarkably low, especially considering the low gain bandwidth product; this suggests the use of some special technique such as error correction or nested feedback. The input impedance linearity shows the for JFET inputs typical high capacitive effects. Note that the THD+N vs. amplitude plots at 10 kHz are above the small-signal bandwidth of the test setup and hence of little significance.

A reasonably priced solution for applications with high output current and/or high supply voltages.

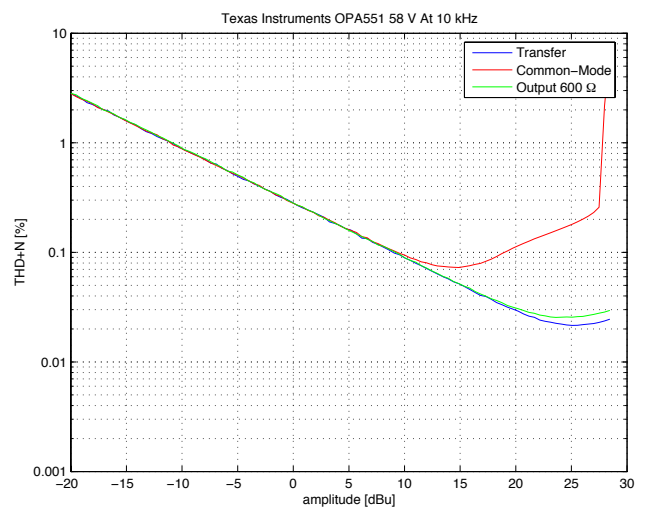
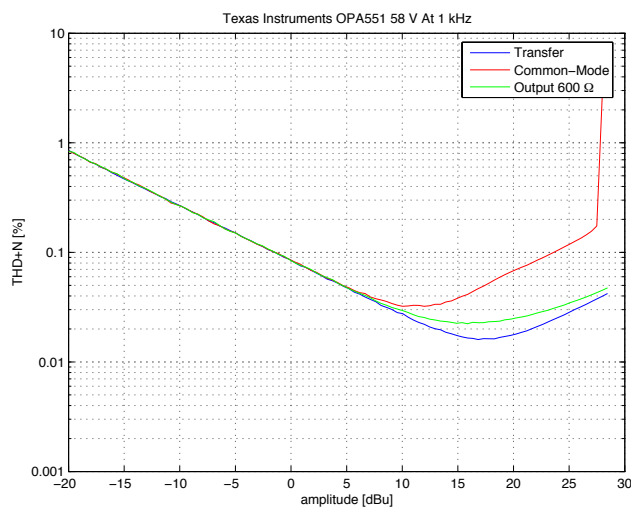
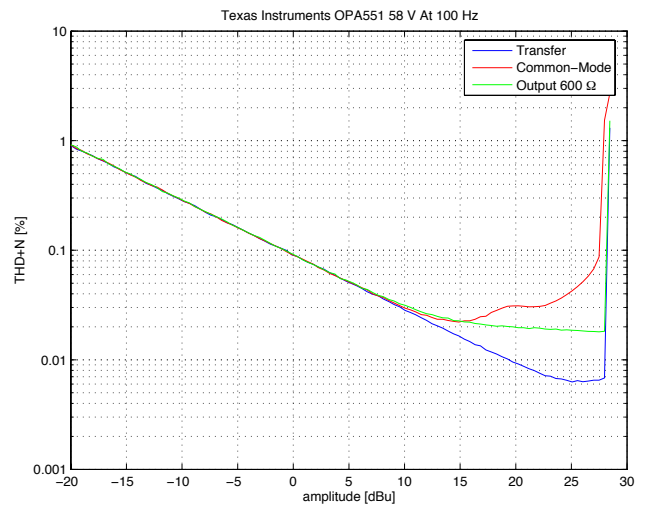
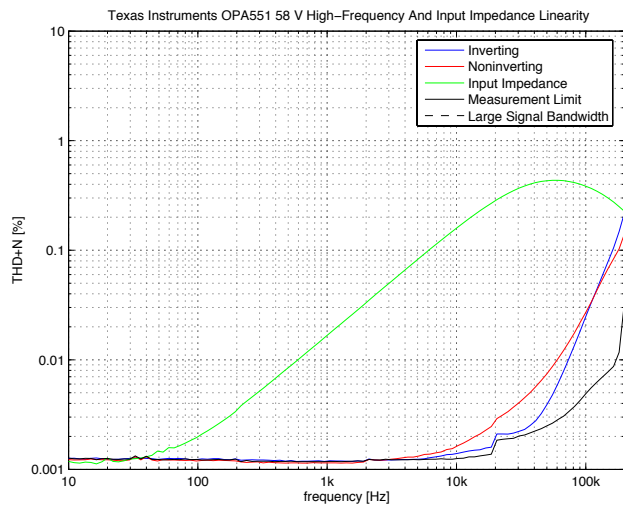
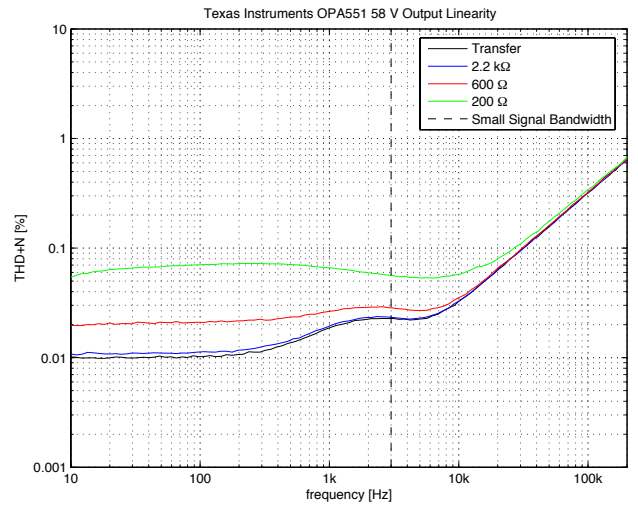
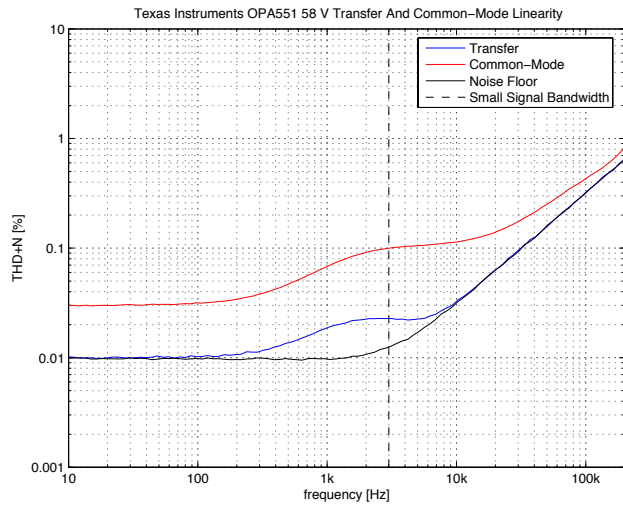


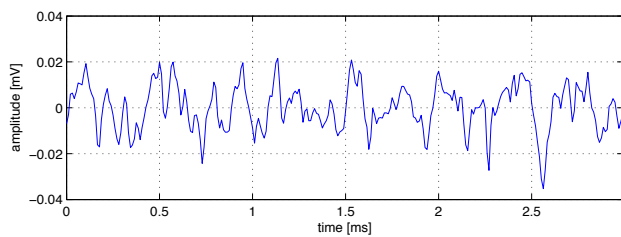
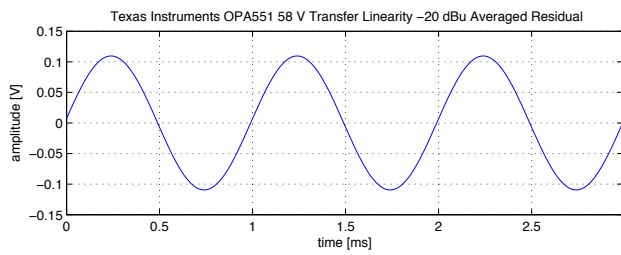
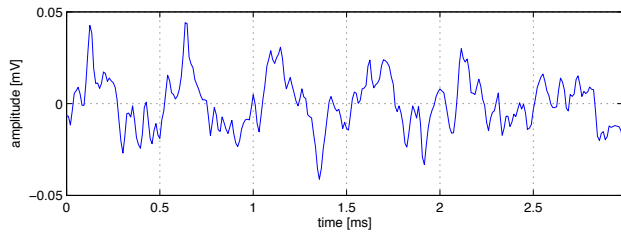
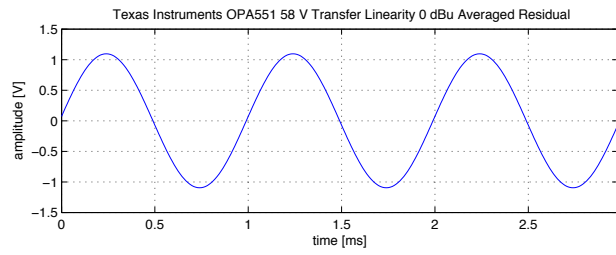
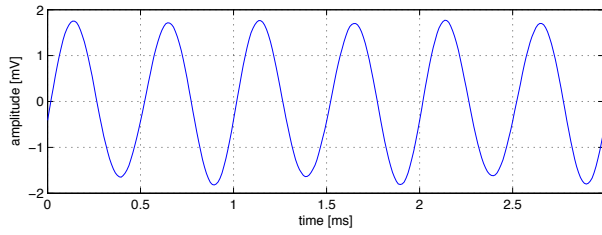
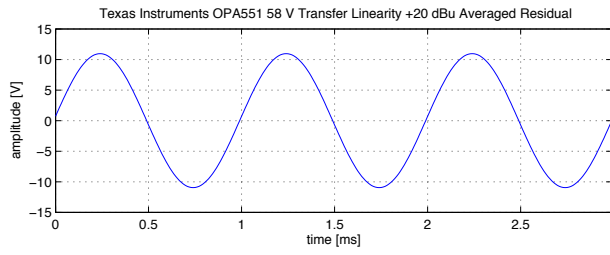


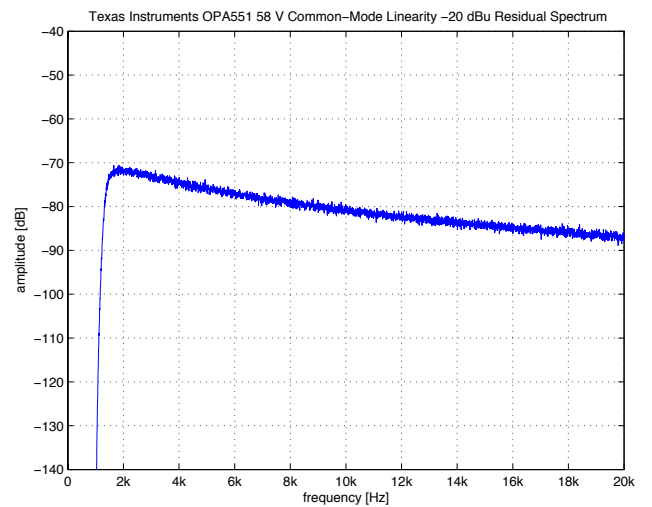
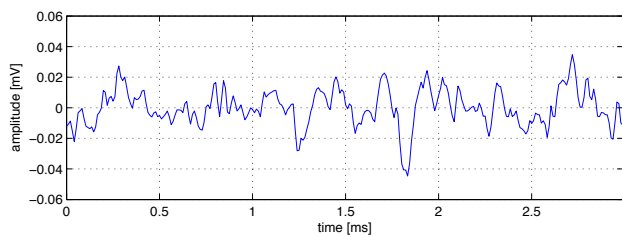
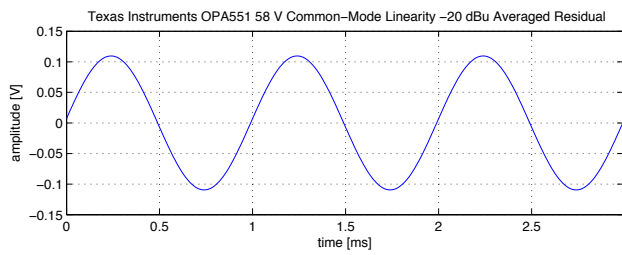
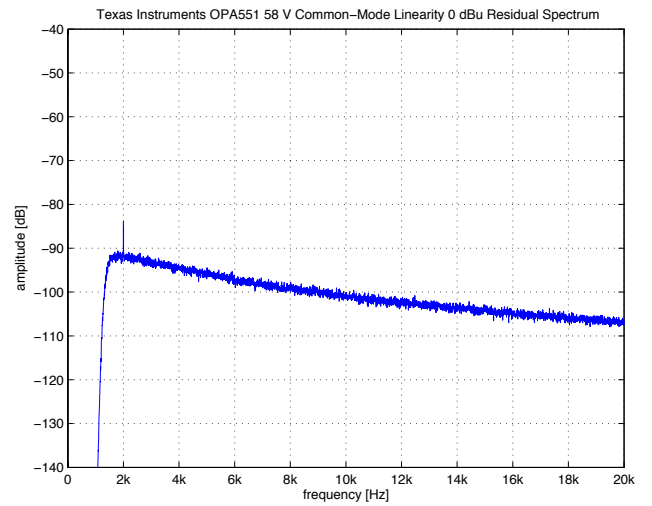
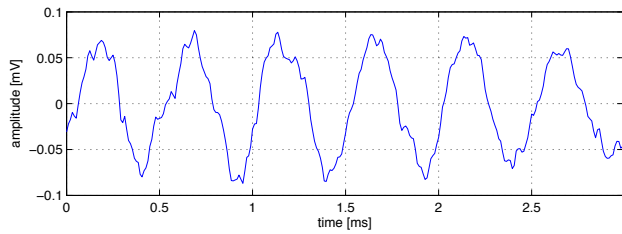
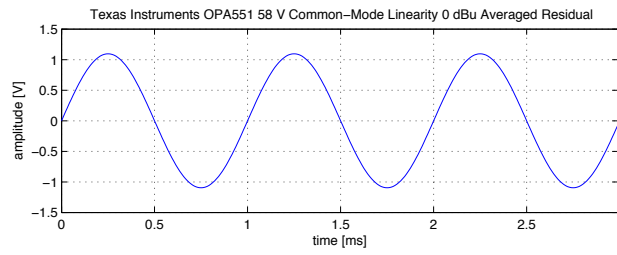
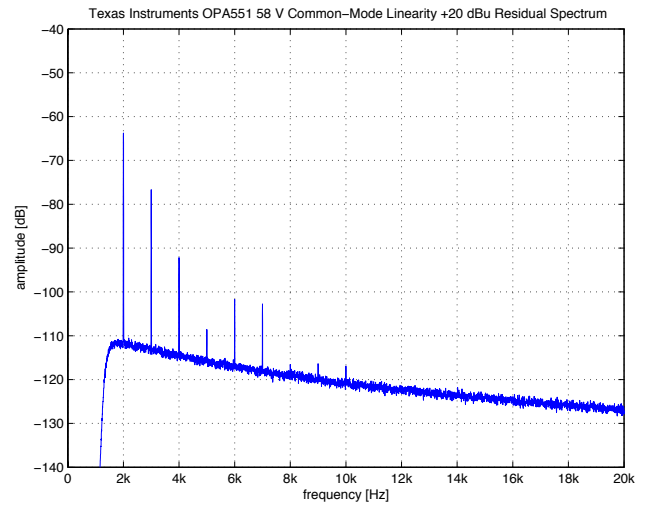
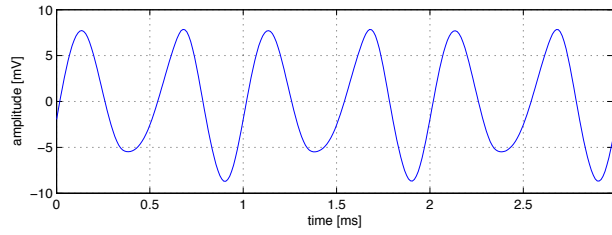
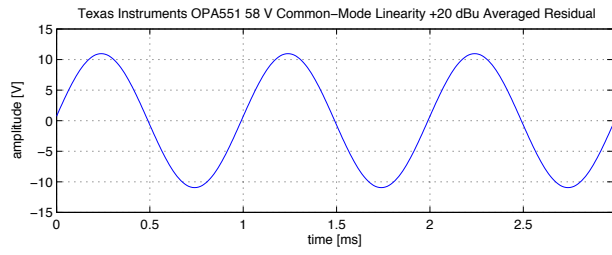


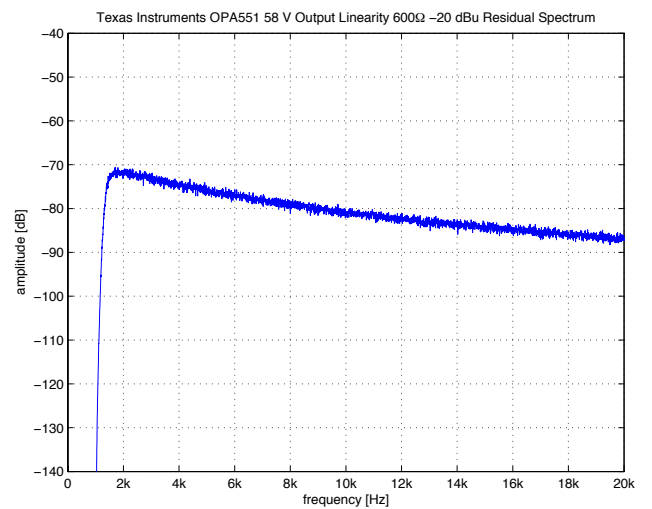
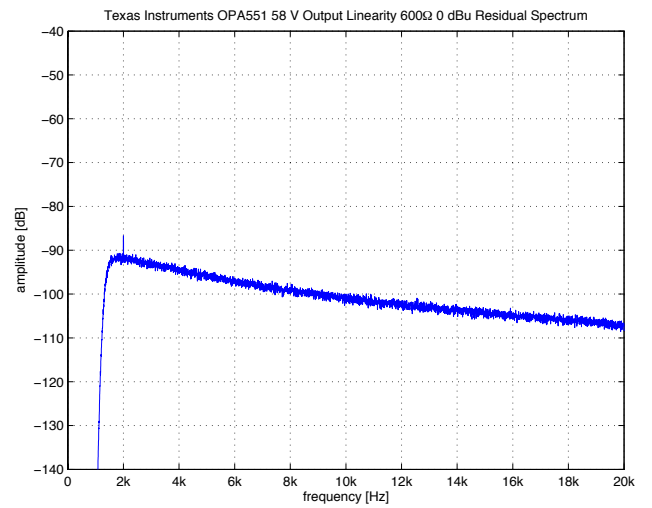
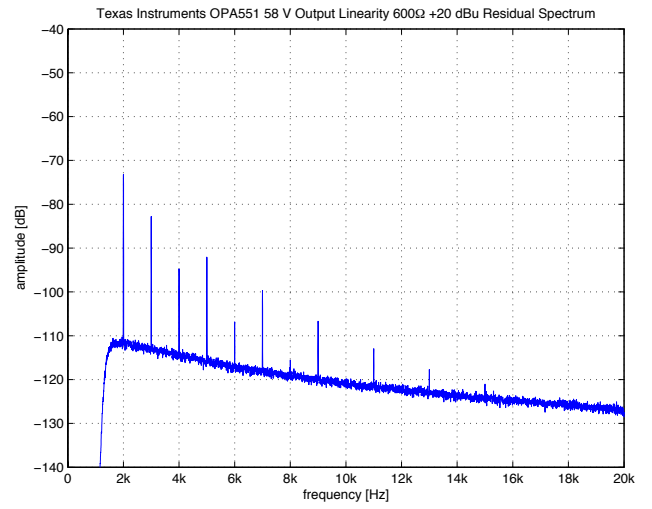
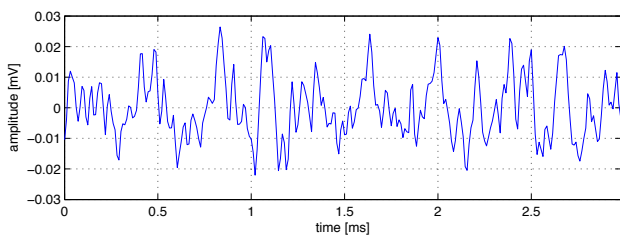
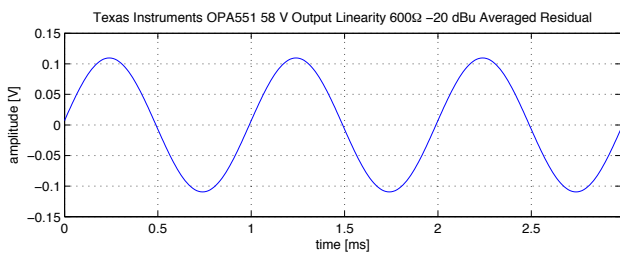
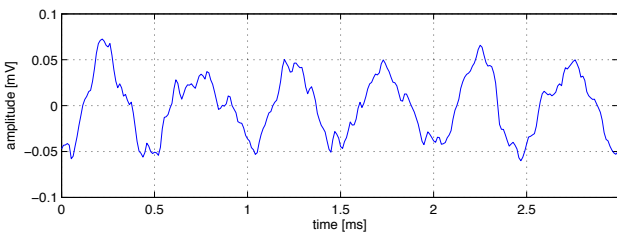
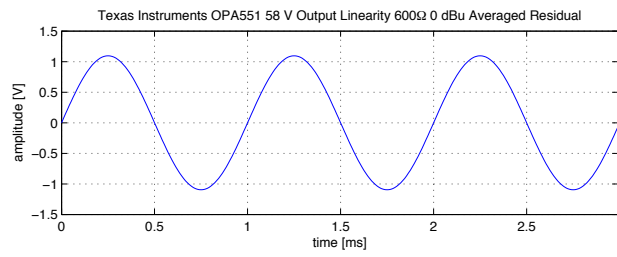
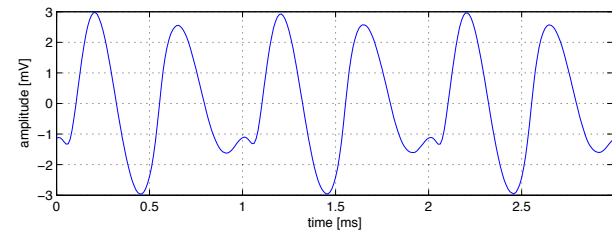
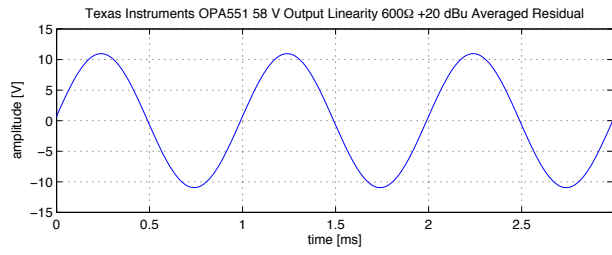












### 3.23 Texas Instruments OPA627

<b>Number of Channels</b>	1
<b>Packages</b>	DIP, SOIC, TO-99
<b>Cost per Amplifier</b>	12.25 US\$ at 1k units (July 2008)

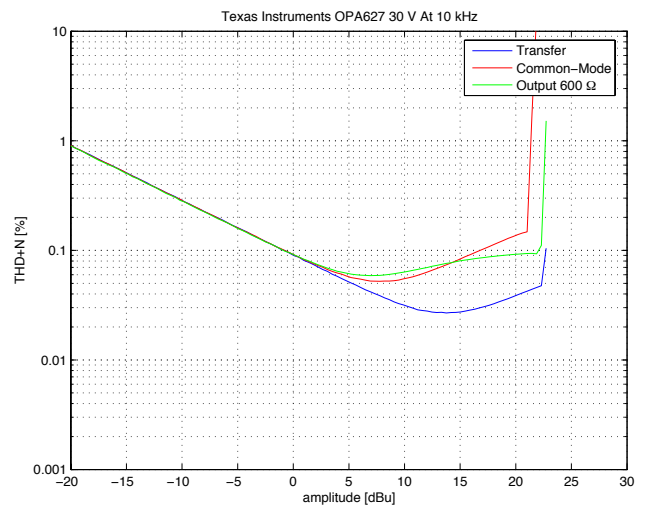
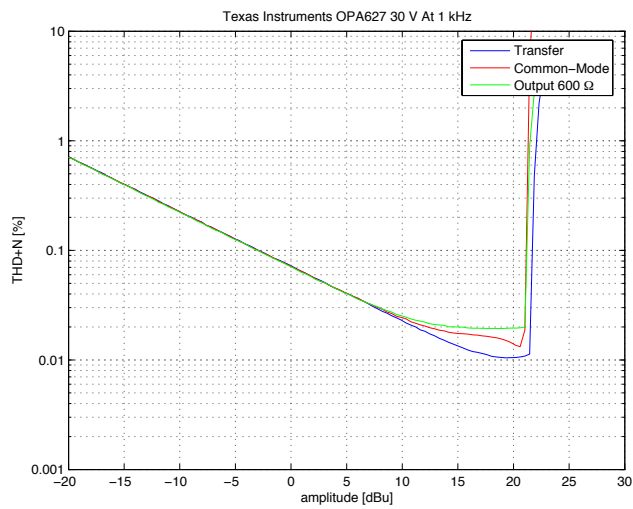
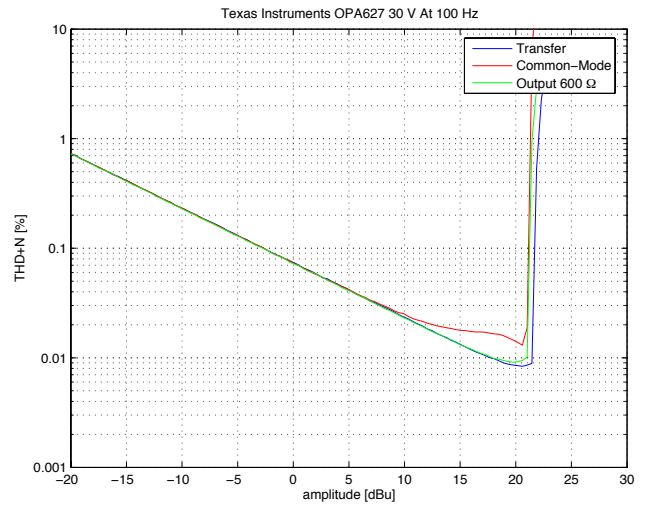
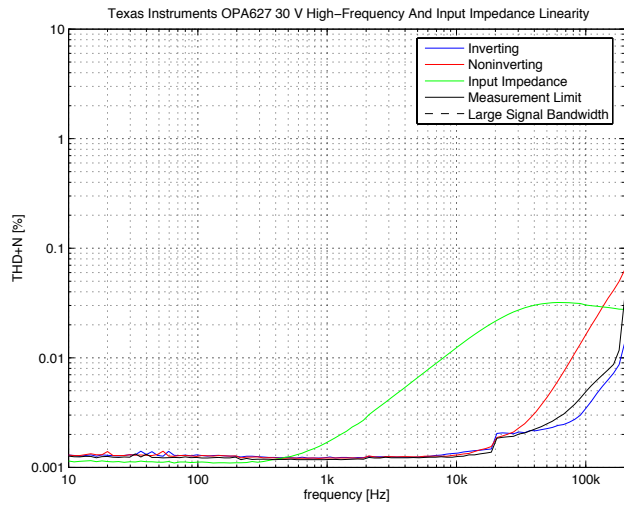
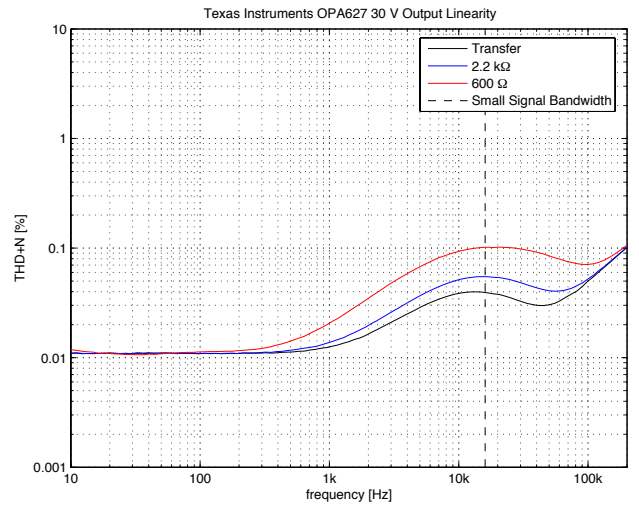
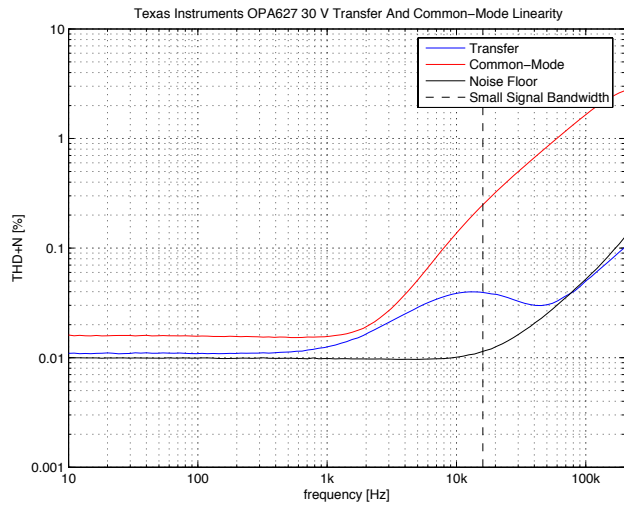
Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		280	500	$\mu\text{V}$
Input Bias Current		2	10	pA
Input Offset Current		1	10	pA
Gain Bandwidth Product		16		MHz
Slew-Rate	40	55		V/ $\mu\text{S}$
Input Voltage Noise (f = 1 kHz)		5.6		nV/ $\sqrt{\text{Hz}}$
Input Current Noise (f = 1 kHz)		2.5		fA/ $\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 11$	$\pm 11.5$		V
Output Voltage Swing ( $R_L = 1 \text{ k}\Omega$ )	$\pm 11.5$	$\pm 12.3$		V
Output Current		$\pm 45$		mA
Power Supply Voltage	$\pm 4.5$		$\pm 18$	V
Quiescent Current per Amplifier		7	7.5	mA

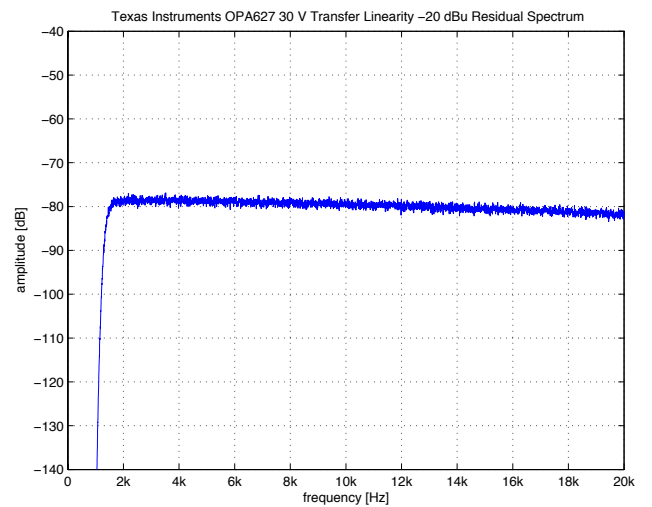
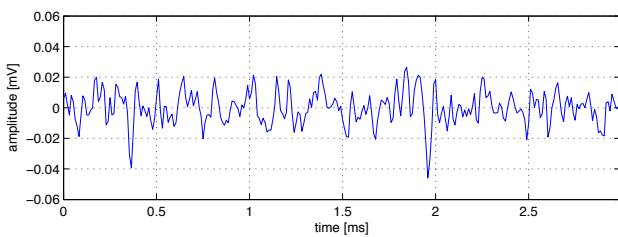
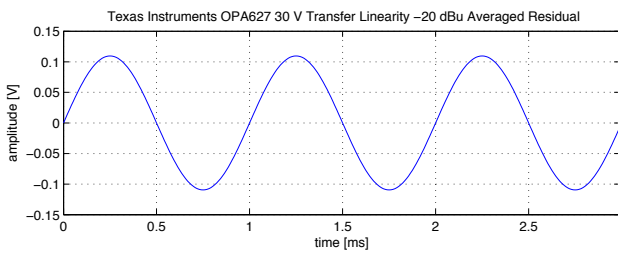
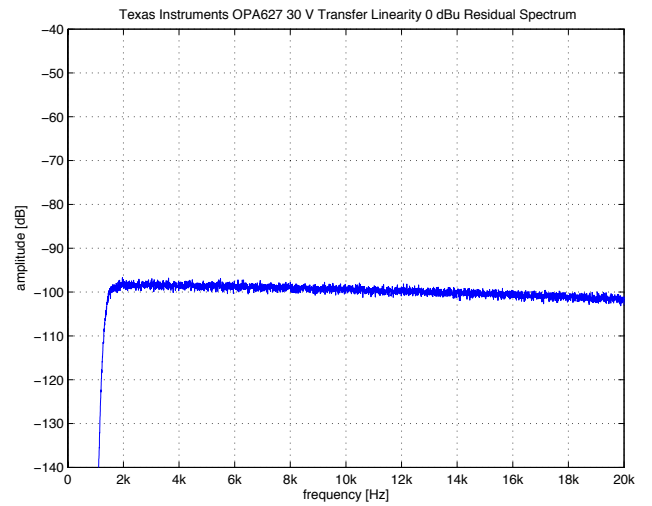
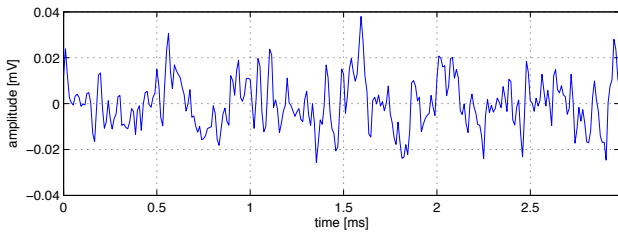
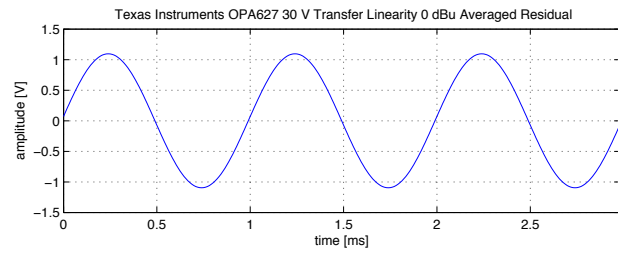
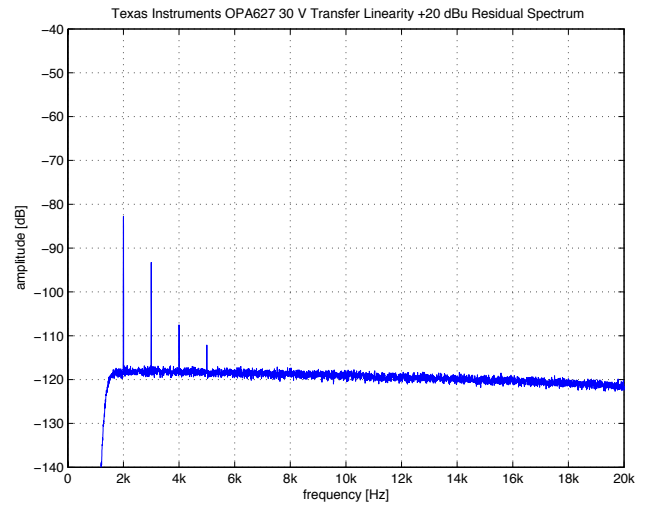
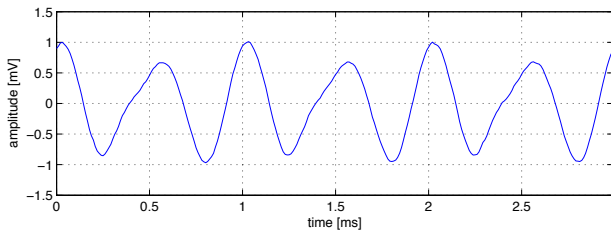
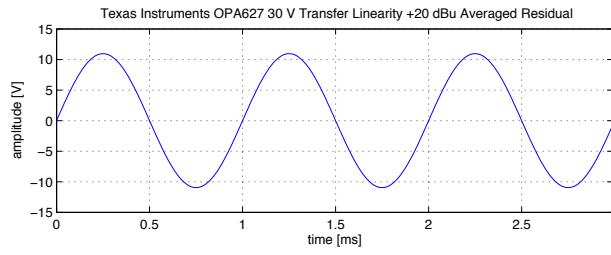
Table 3.23: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 15 \text{V}$ .

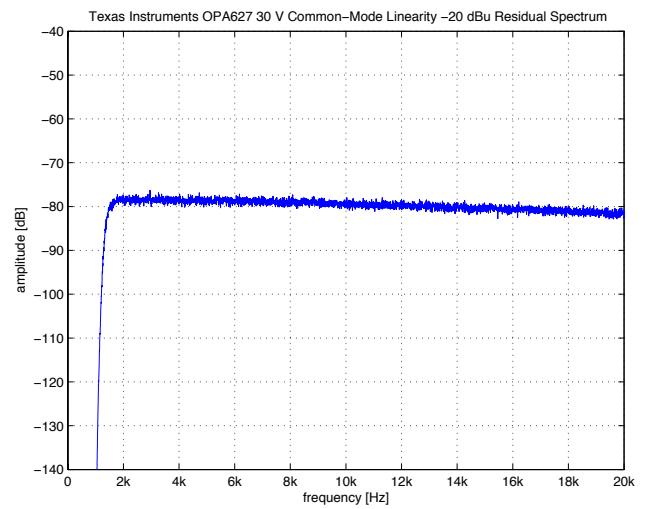
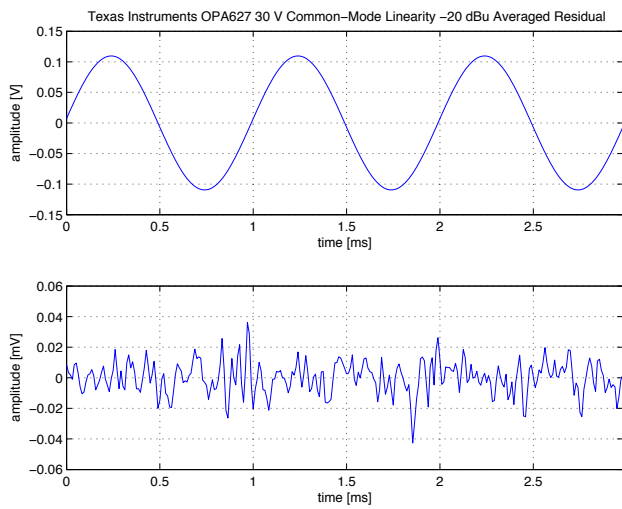
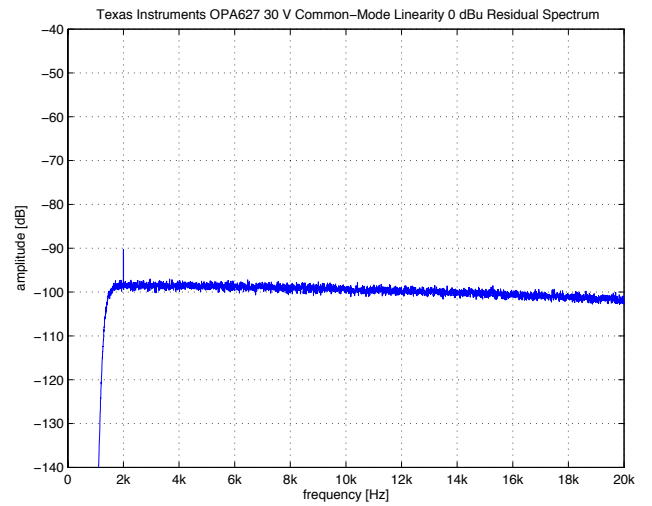
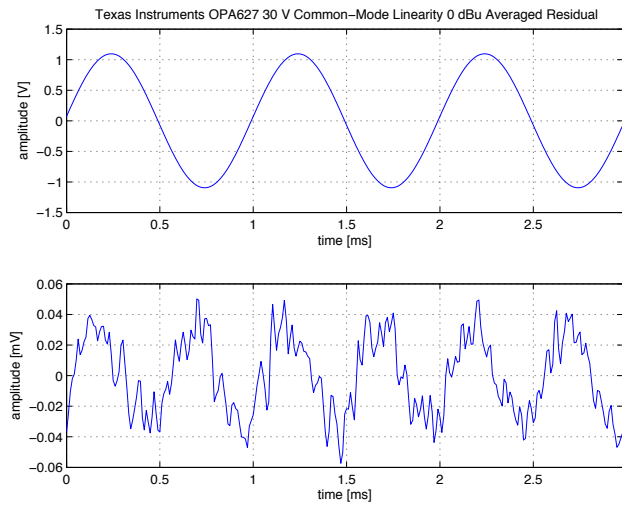
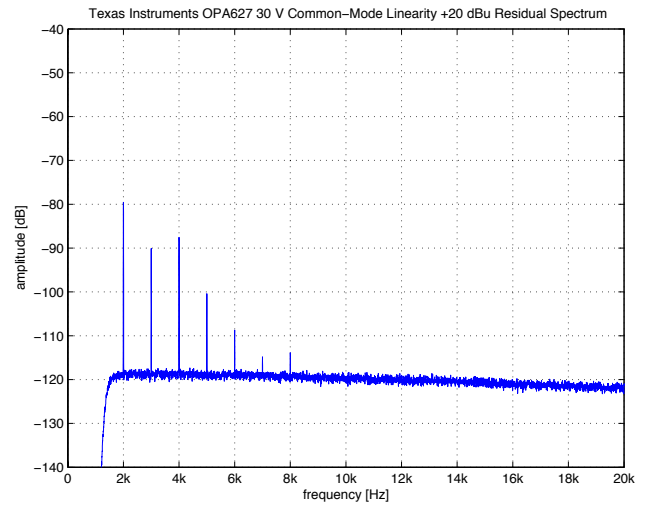
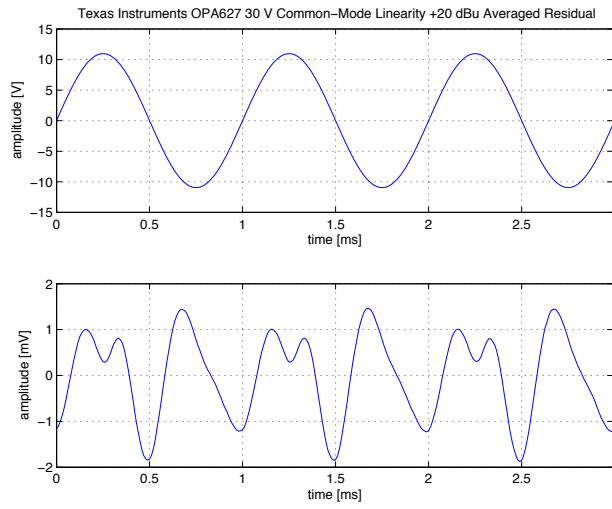
A JFET input opamp combining good DC precision, low input bias current/current noise and high bandwidth/slew-rate. Based on a two-stage topology. A decompensated version (OPA637) is available for applications with higher noise gain.

Low basic transfer and slew-induced distortion. Common-mode distortion is relatively well controlled for a JFET input amplifier—mainly a result from the use of a bootstrapping circuit for the input transistors; it causes a substantial decrease in overall distortion performance at higher frequencies nonetheless. Mainly at higher frequencies increased output loading causes an easily measurable though still relatively modest increase in distortion.

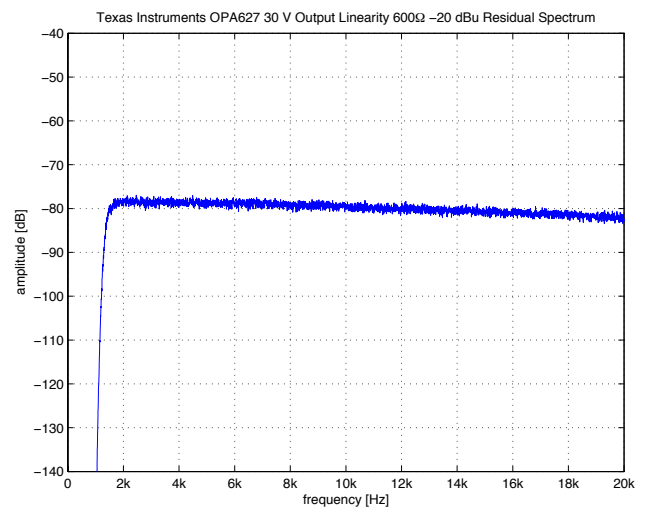
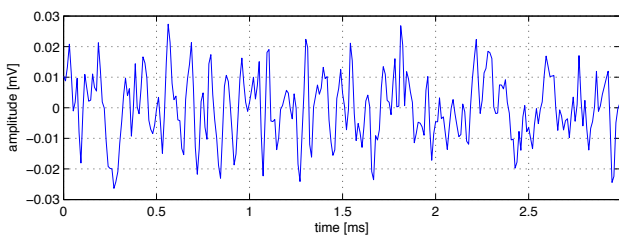
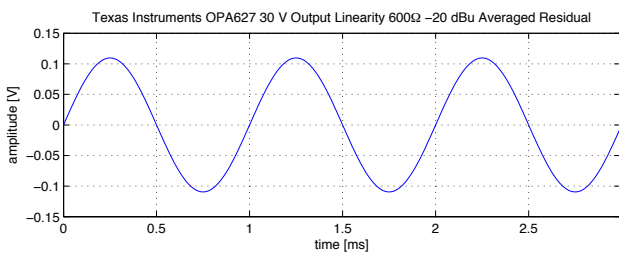
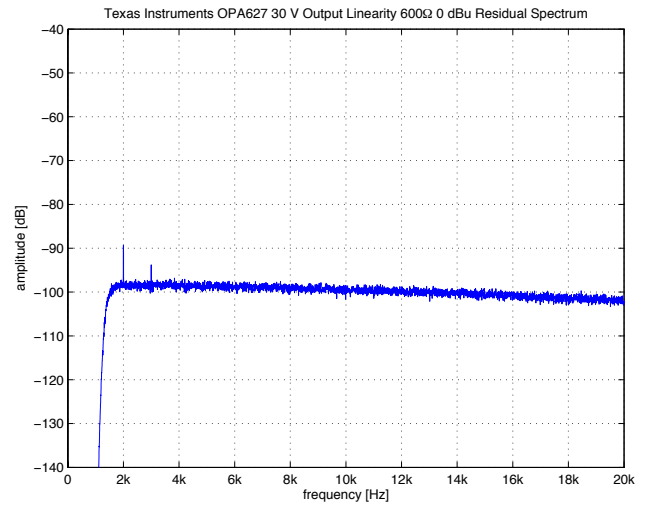
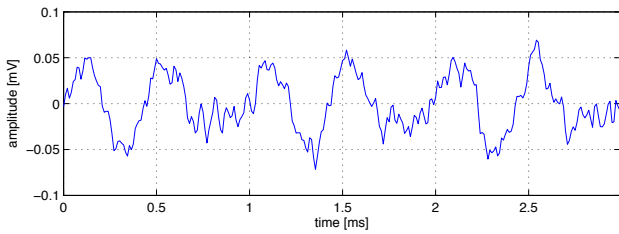
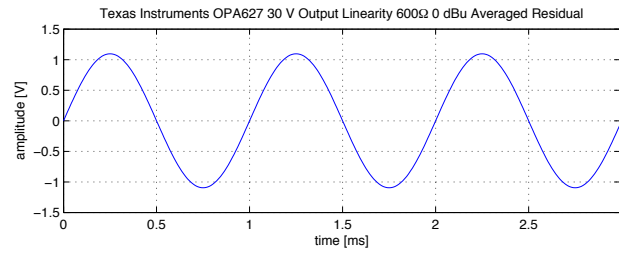
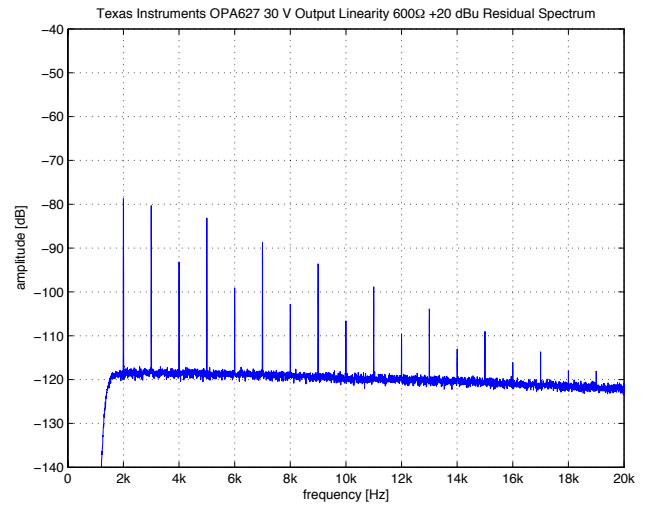
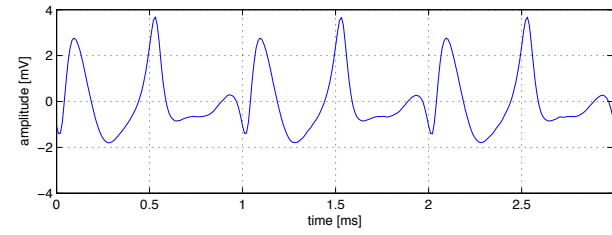
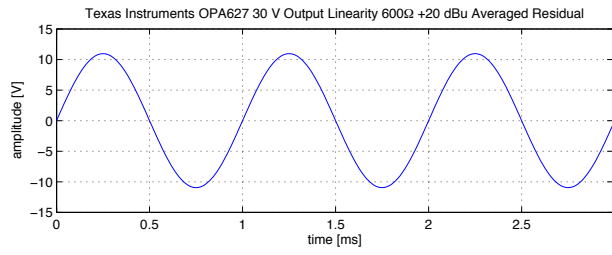
A good though very costly choice for low distortion applications requiring JFET inputs.











### 3.24 Texas Instruments OPA2132

<b>Number of Channels</b>	2
<b>Packages</b>	DIP, SO-8
<b>Cost per Amplifier</b>	1.20 US\$ at 1k units (July 2008)

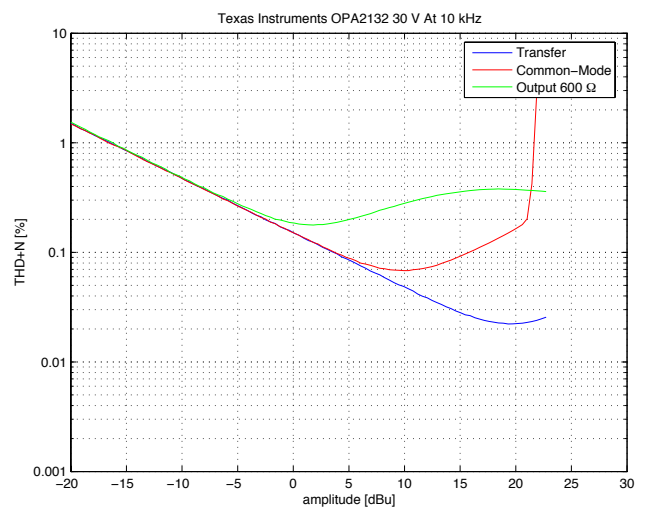
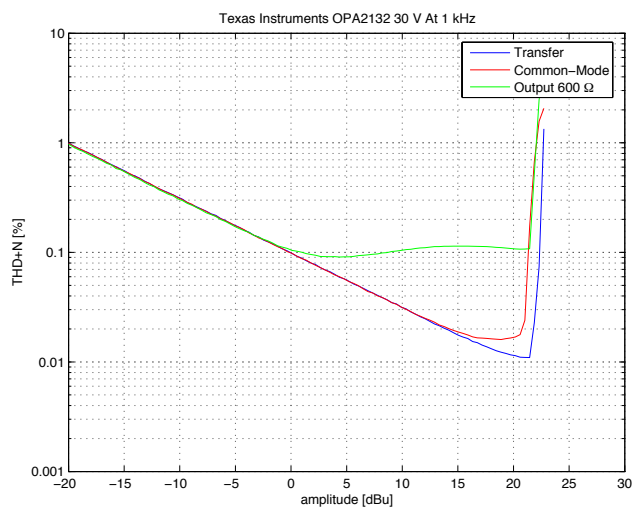
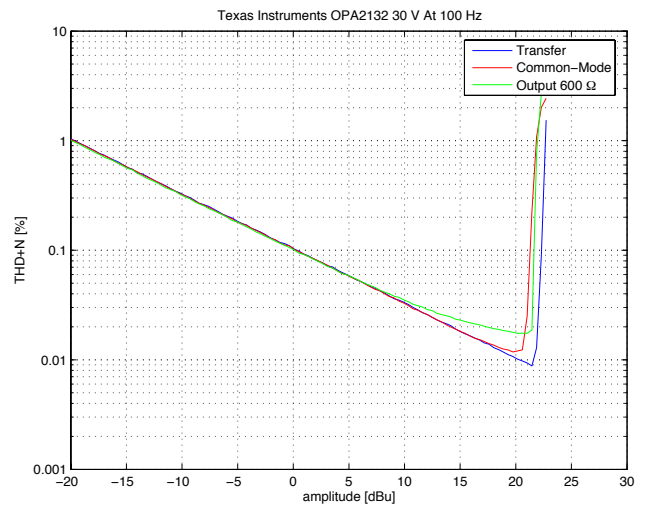
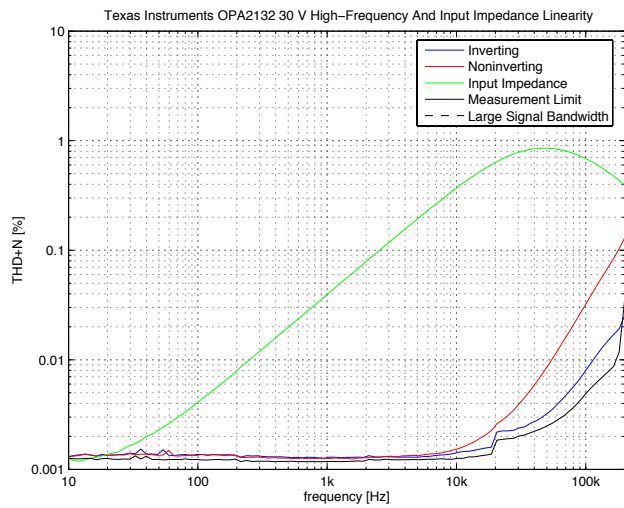
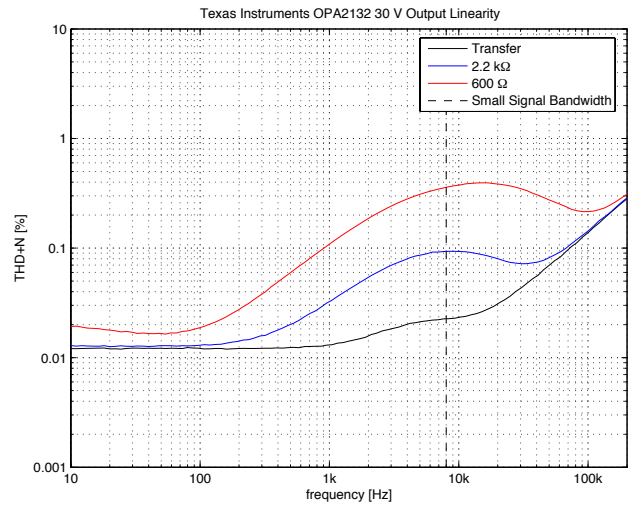
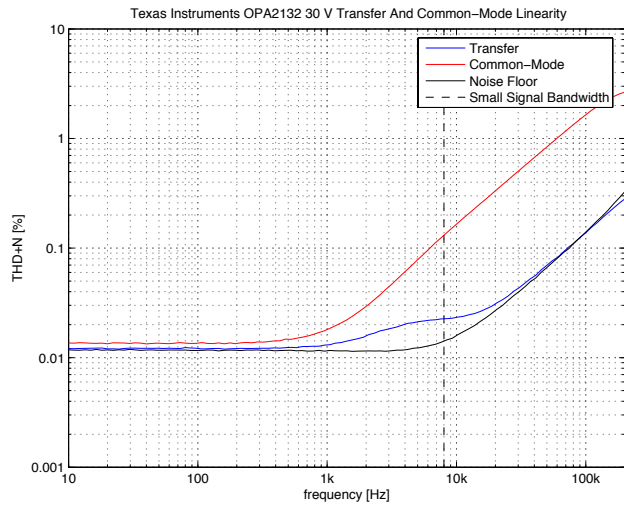
Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		0.5	2	mV
Input Bias Current		5	50	pA
Input Offset Current		2	50	pA
Gain Bandwidth Product		8		MHz
Slew-Rate		20		V/ $\mu$ S
Input Voltage Noise (f = 1 kHz)		8		nV/ $\sqrt{\text{Hz}}$
Input Current Noise (f = 1 kHz)		3		fA/ $\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 12.5$	$\pm 13$		V
Output Voltage Swing ( $R_L = 2 \text{ k}\Omega$ )	+13.5/-13.8	+13.8/-14.1		V
Output Voltage Swing ( $R_L = 600 \Omega$ )	+12.5/-12.8	+13/-13.1		V
Power Supply Voltage	$\pm 2.5$		$\pm 18$	V
Quiescent Current per Amplifier		4	4.8	mA

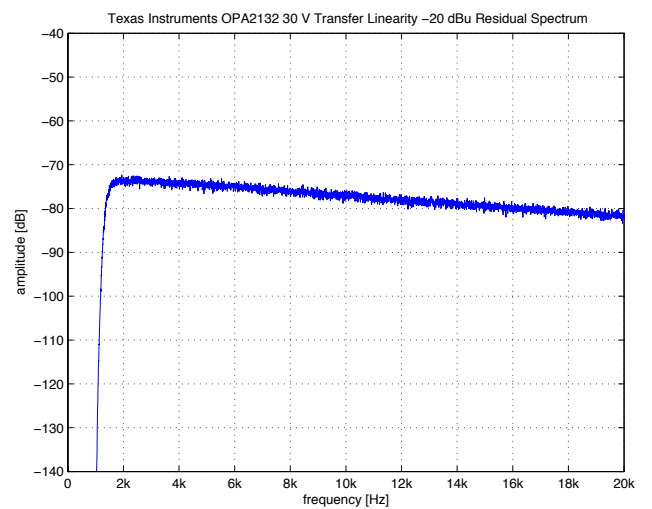
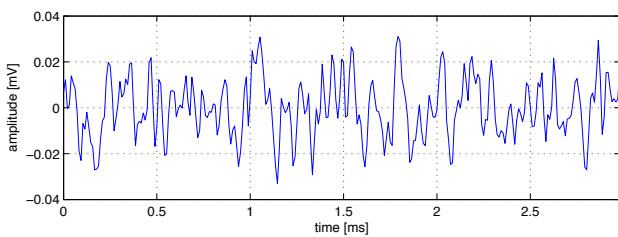
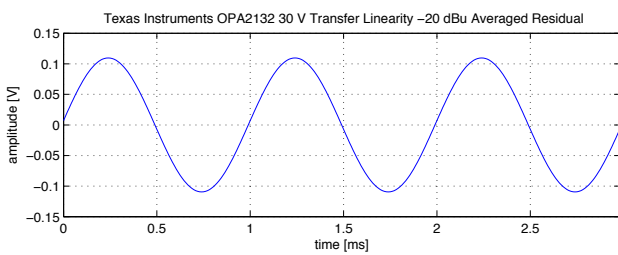
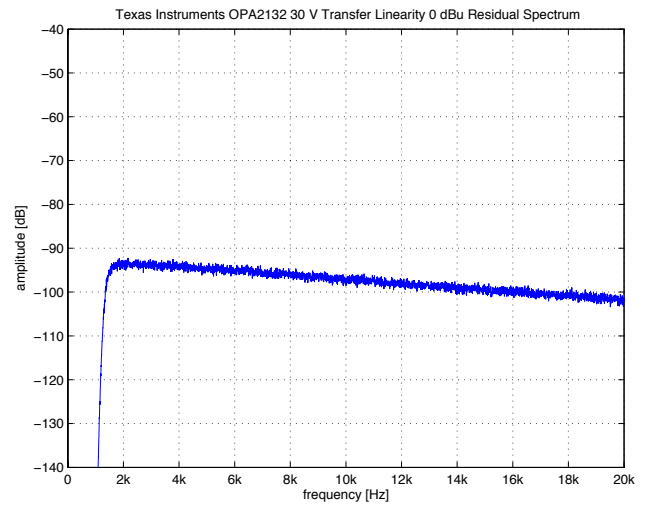
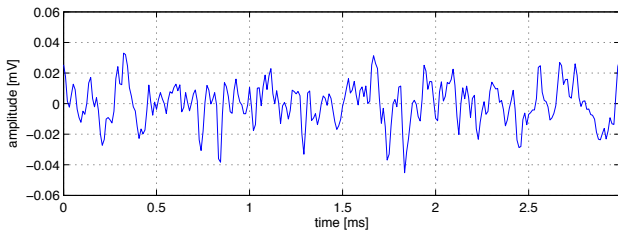
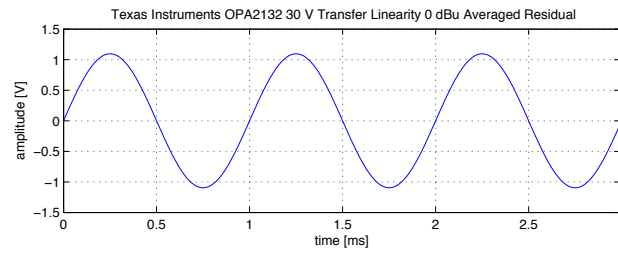
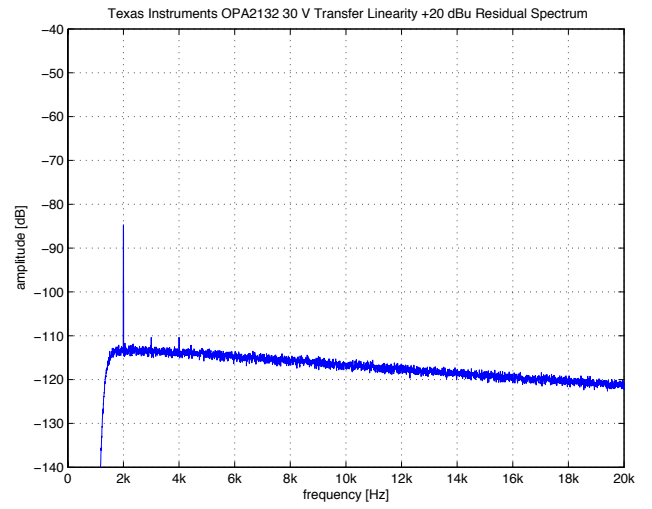
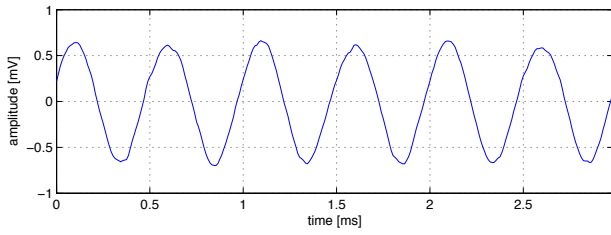
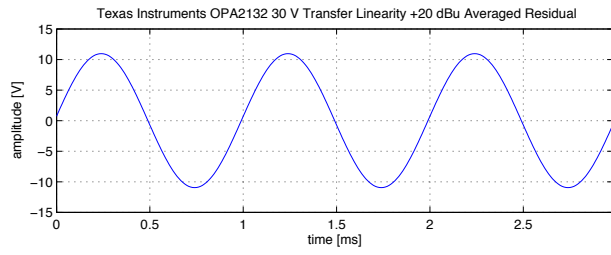
Table 3.24: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 15 \text{V}$ .

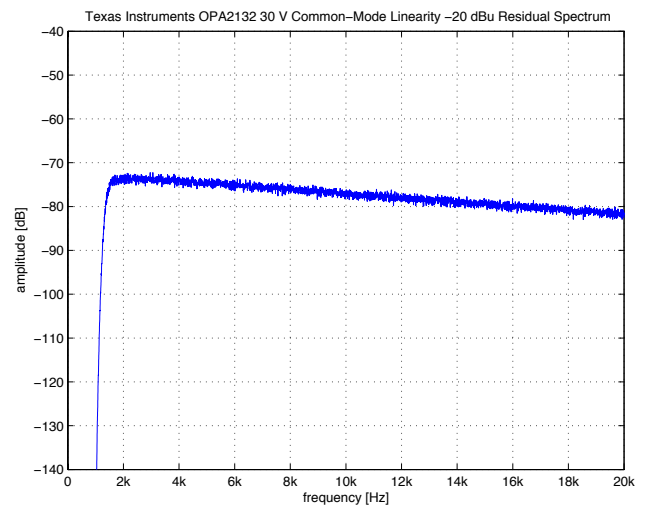
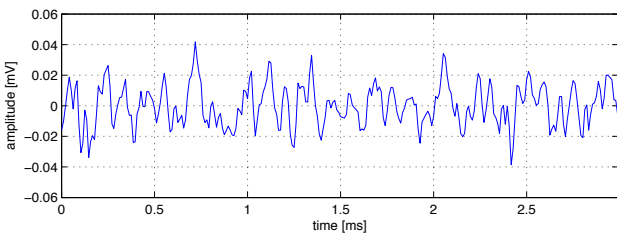
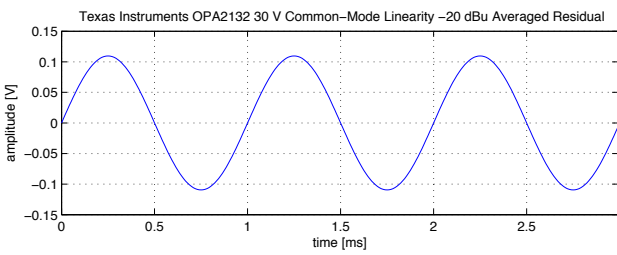
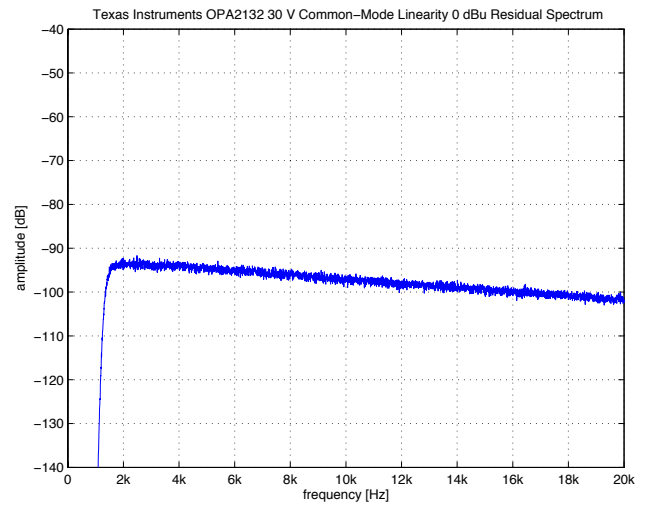
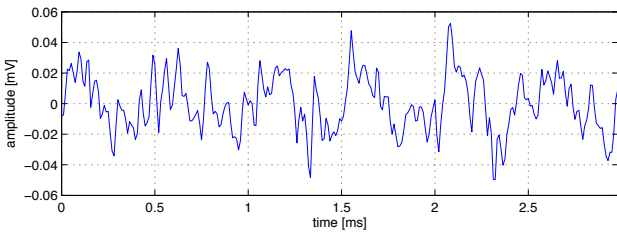
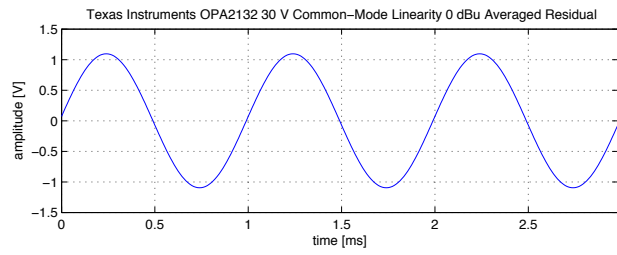
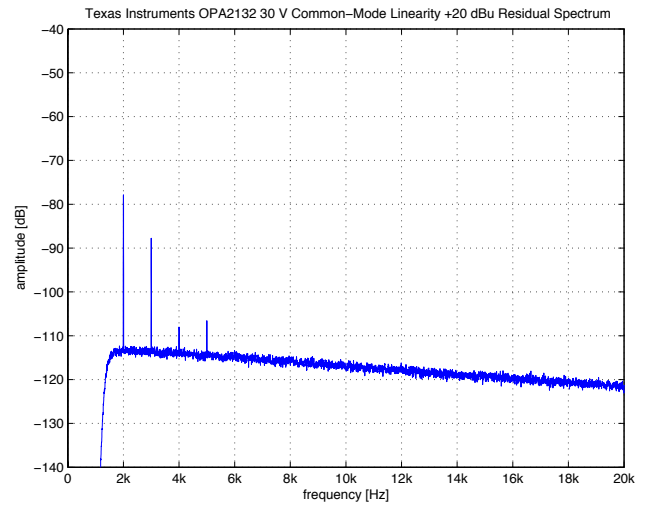
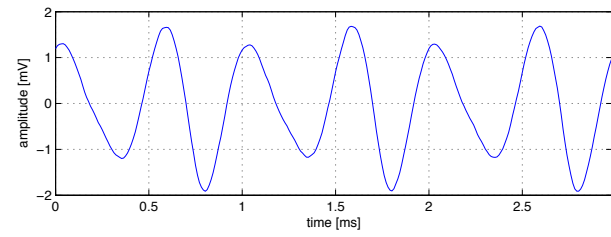
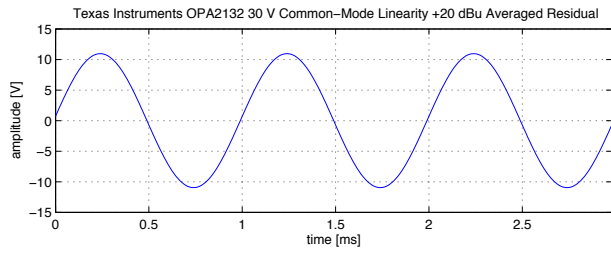
A dual amplifier with JFET inputs, topology is unknown. Voltage noise is modestly good only, input offset is rather good for a JFET amplifier though. Single and quad version are available (OPA132 and OPA4132); OPA134/OPA2134/OPA4134 appear to be versions with relaxed DC precision specification.

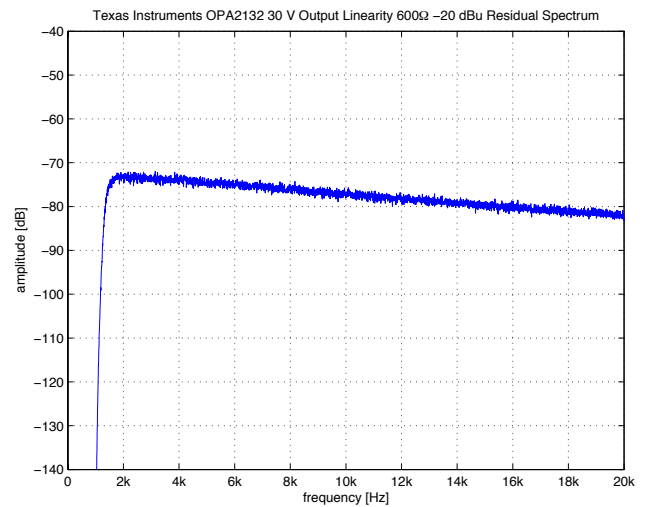
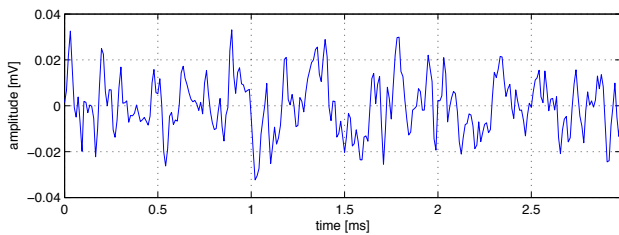
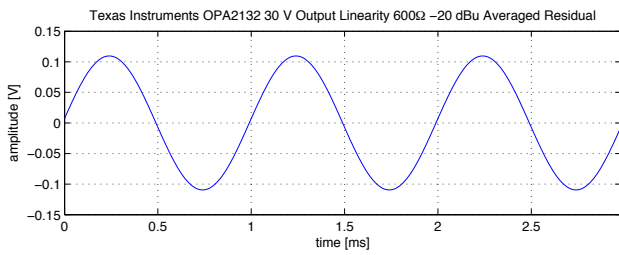
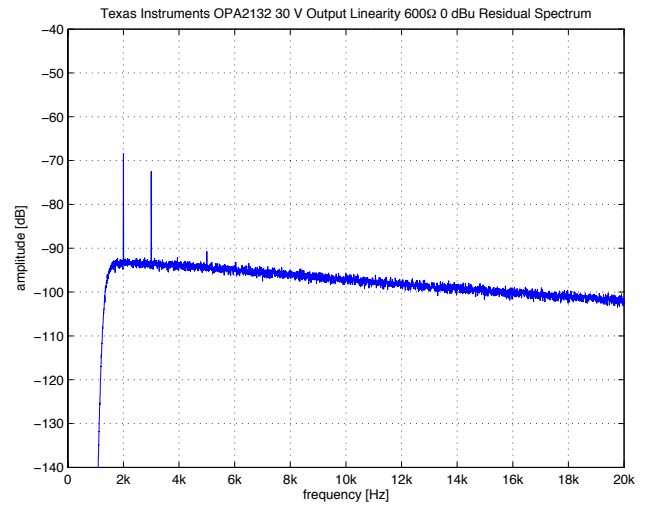
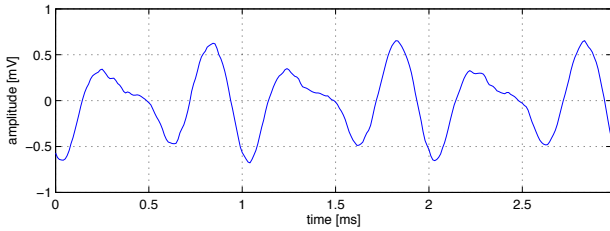
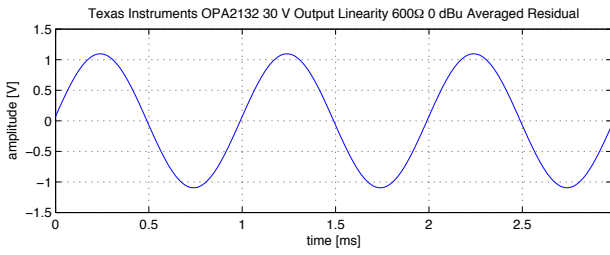
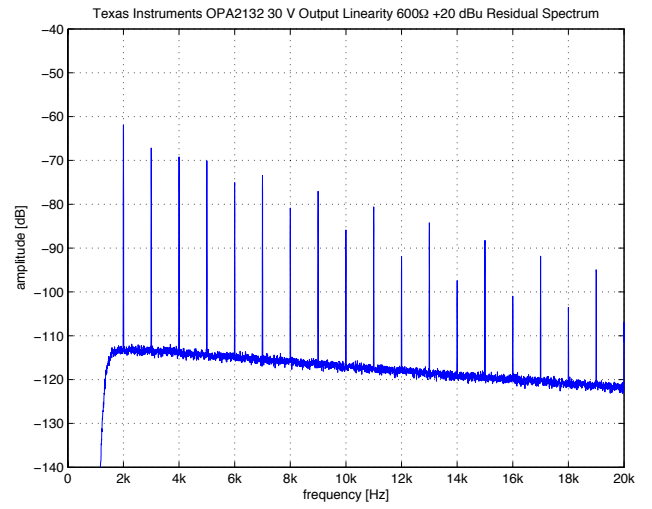
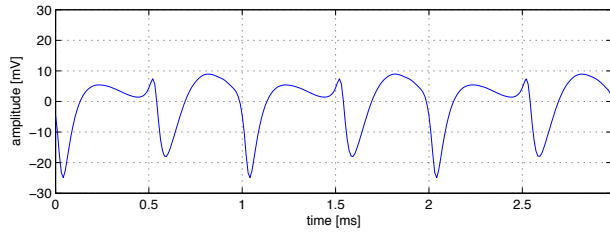
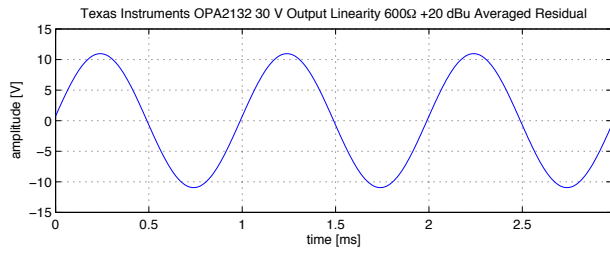
The basic transfer linearity is pretty good, although it degrades somewhat at higher frequencies. Common-mode effects are relatively well controlled for a JFET input devices, though resulting distortion is very significant at higher frequencies nonetheless. Heavy output loading causes serious distortion, with thermal effects and harmonics up to high frequencies visible.

Good overall cost-performance ratio for a JFET device. For lowest distortion attention to common-mode and especially output loading effects needed. Suitable upgrade for TL072 amplifiers where the higher quiescent current is no concern.









### 3.25 Texas Instruments OPA2604

<b>Number of Channels</b>	2
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	1.20 US\$ at 100 units (July 2008)

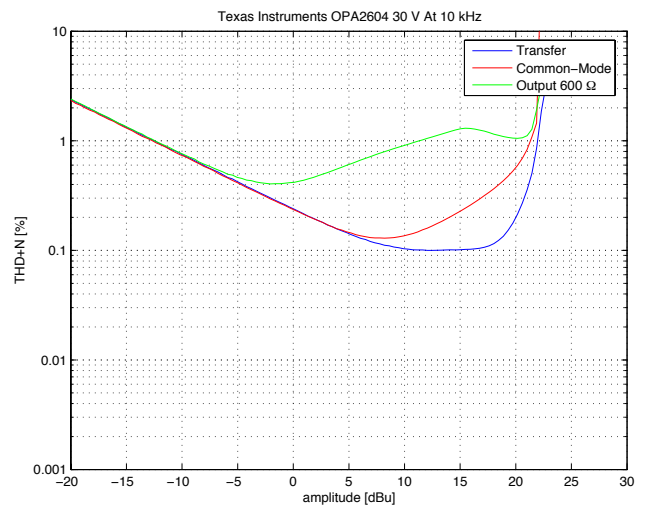
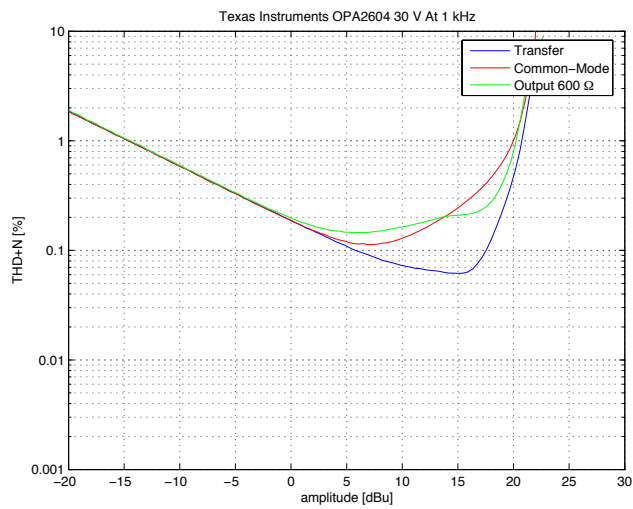
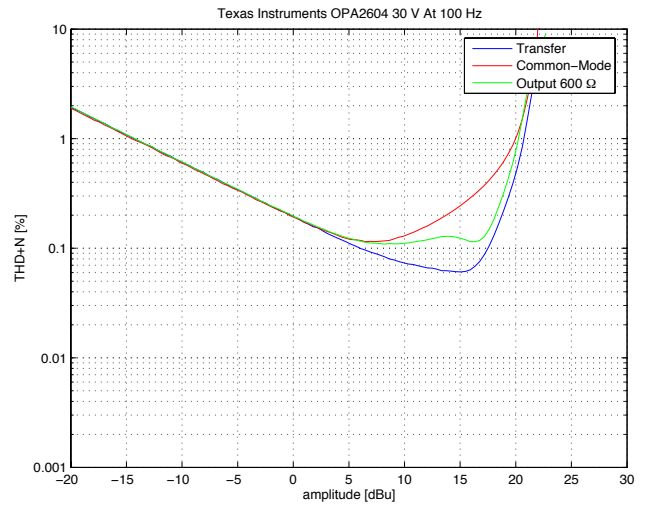
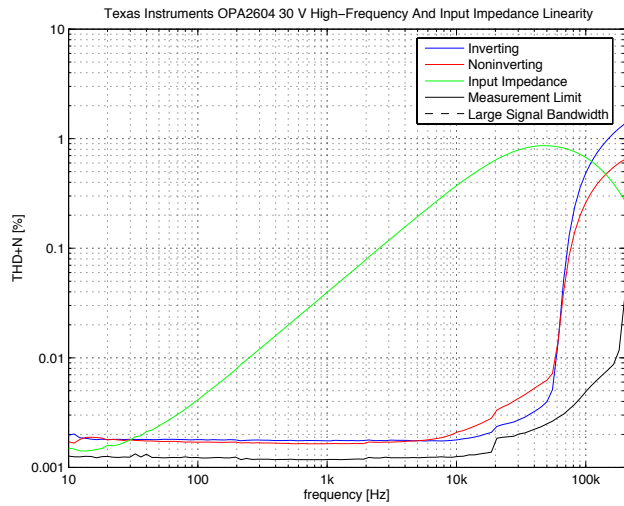
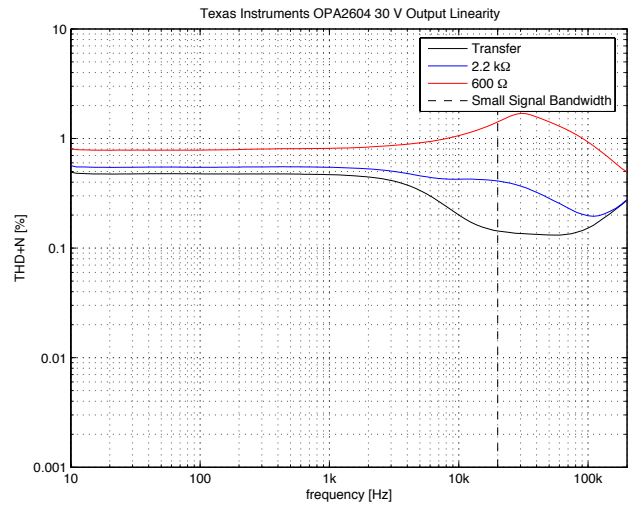
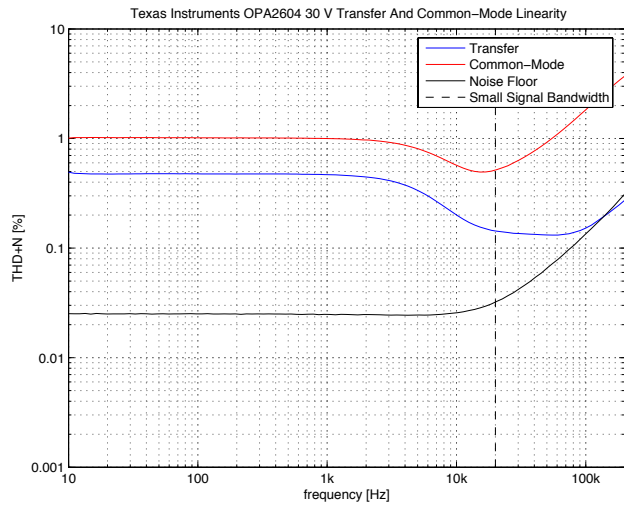
Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		1	5	mV
Input Bias Current		100		pA
Input Offset Current		4		pA
Gain Bandwidth Product		20		MHz
Slew-Rate	15	25		V/ $\mu$ S
Input Voltage Noise (f = 1 kHz)		11		nV/ $\sqrt{\text{Hz}}$
Input Current Noise (f = 1 kHz)		6		fA/ $\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 12$	$\pm 13$		V
Output Voltage Swing ( $R_L = 600 \Omega$ )	$\pm 11$	$\pm 12$		V
Output Current		$\pm 35$		mA
Power Supply Voltage	$\pm 4.5$		$\pm 25$	V
Quiescent Current per Amplifier		5.25	6	mA

Table 3.25: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 15 \text{V}$ .

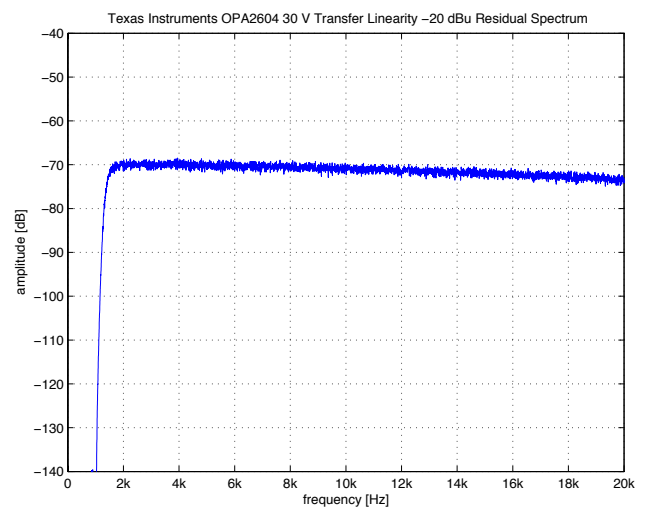
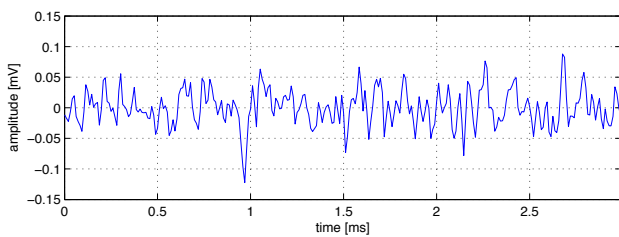
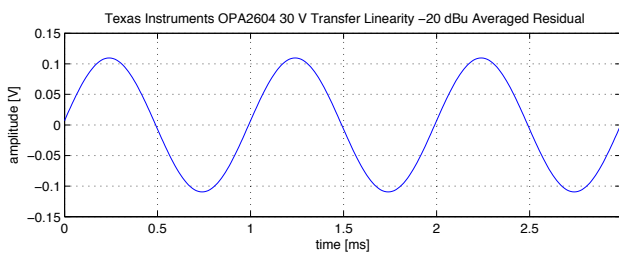
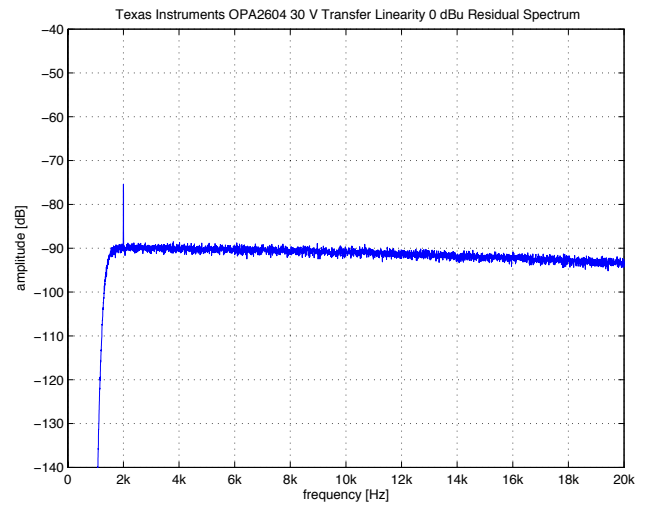
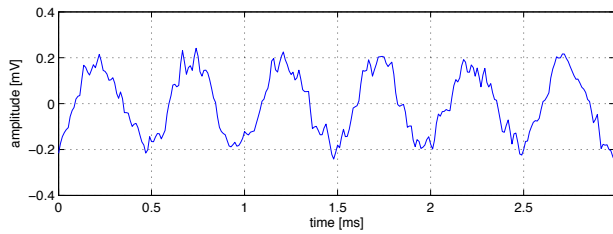
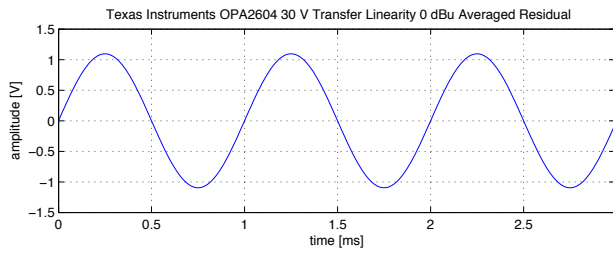
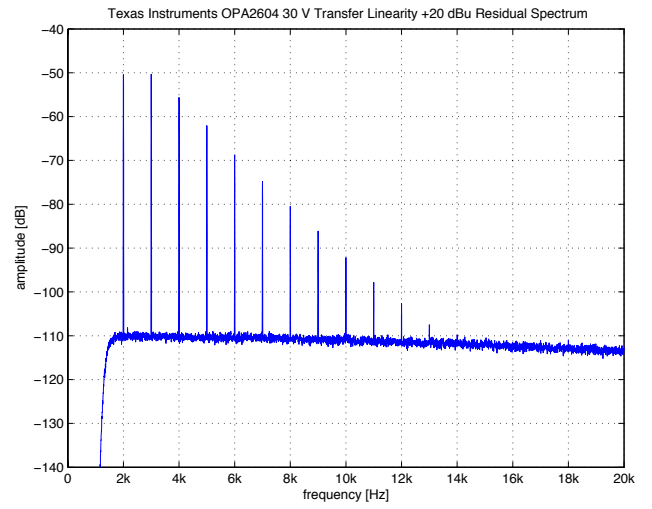
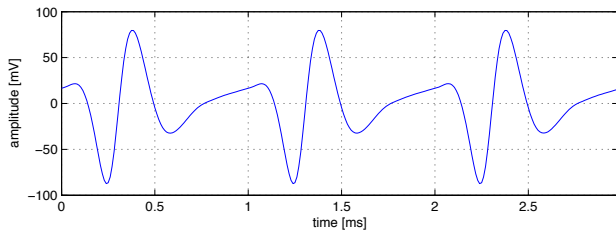
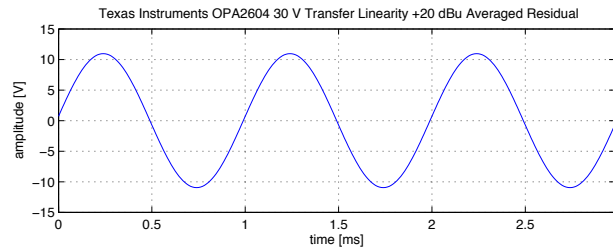
A JFET opamp specifically designed for audio applications, using a single-stage folded cascode architecture. Runs on a very wide power supply range, including unusually high voltages. Voltage noise is rather high.

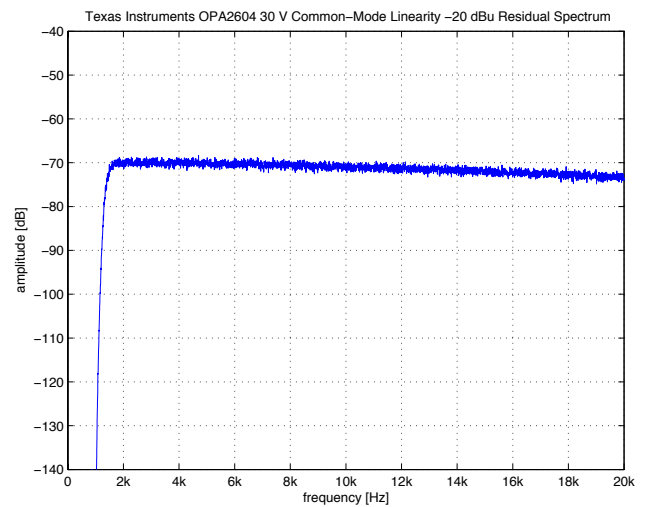
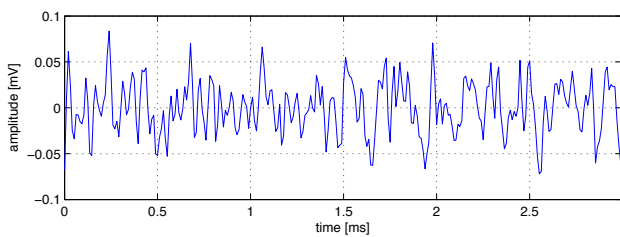
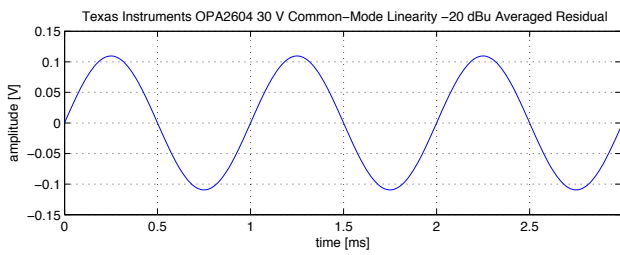
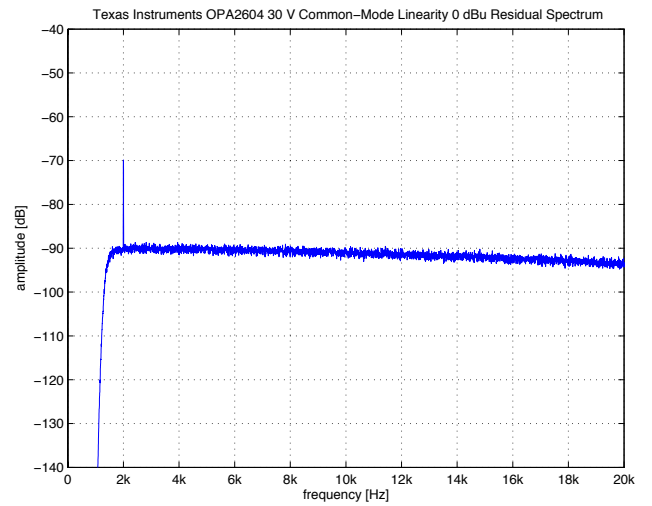
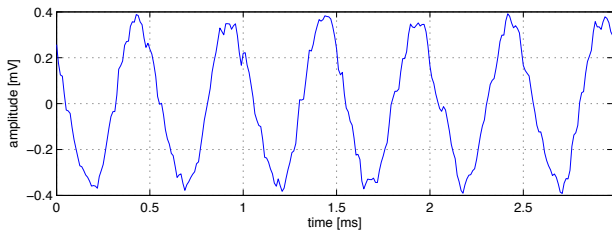
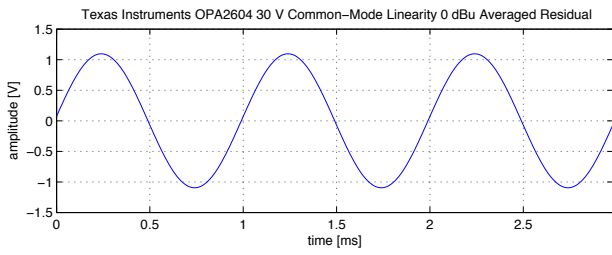
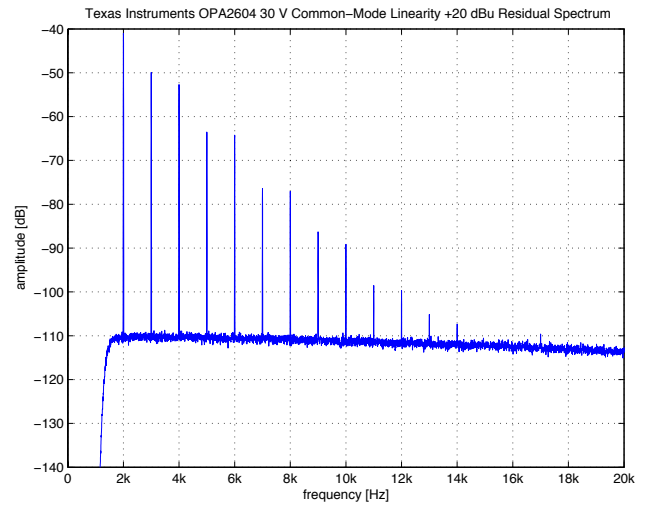
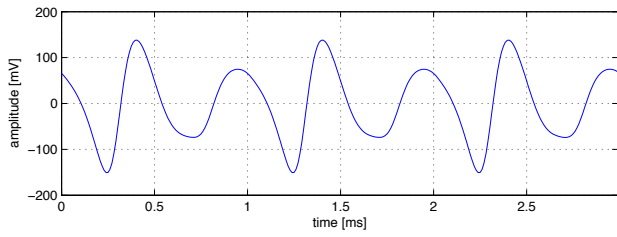
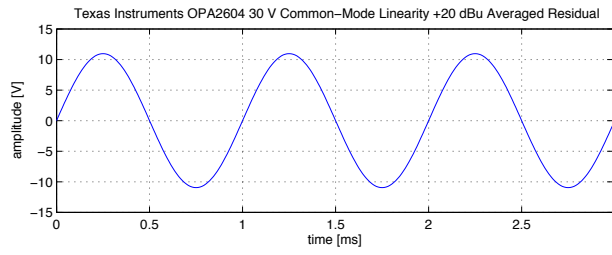
Why the manufacturer advertises this opamp as having particularly low distortion remains somewhat mysterious; all four distortion mechanism are heavily present, and the distortion at higher frequencies rapidly increases even further although the slew-rate of the amplifier is high. At least higher supply voltages help things considerably. Particularly noticeable is the excellent input impedance linearity with the 48 V power supply.

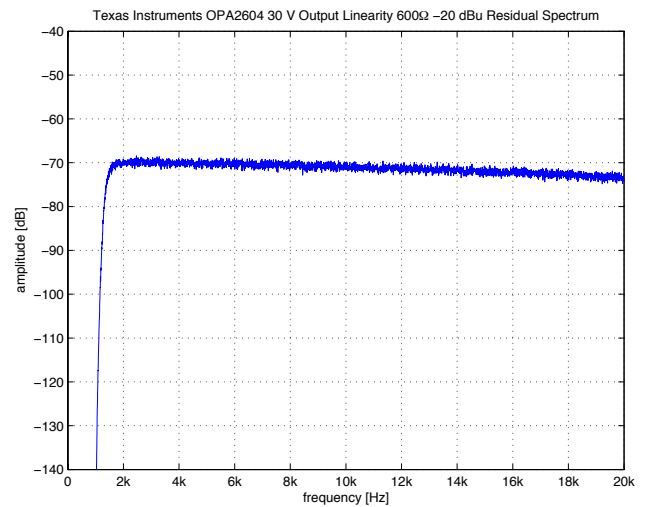
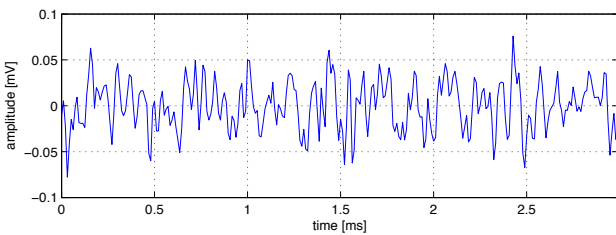
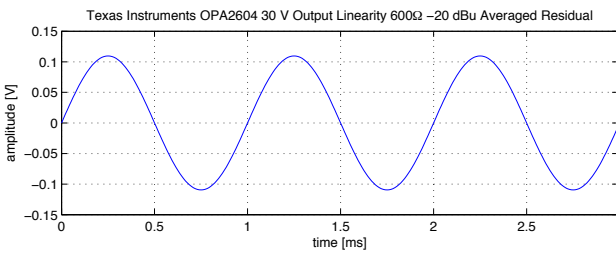
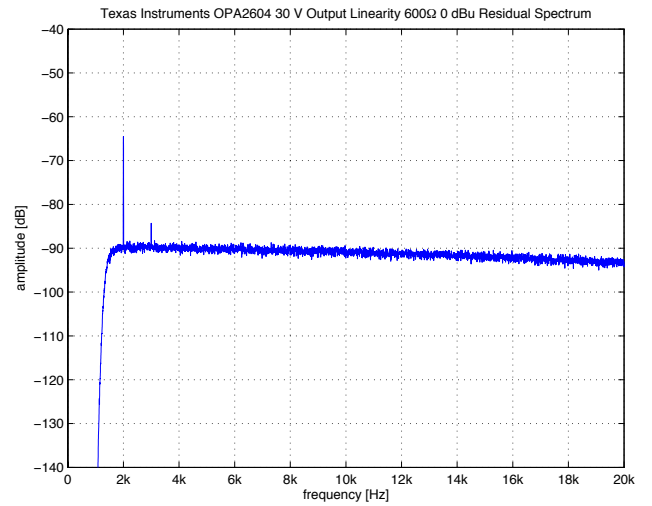
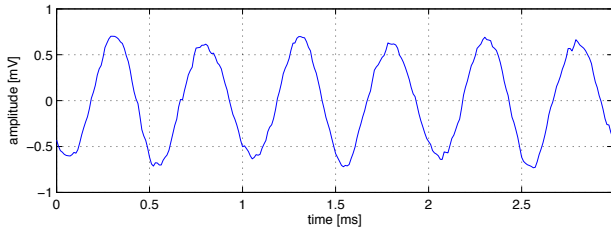
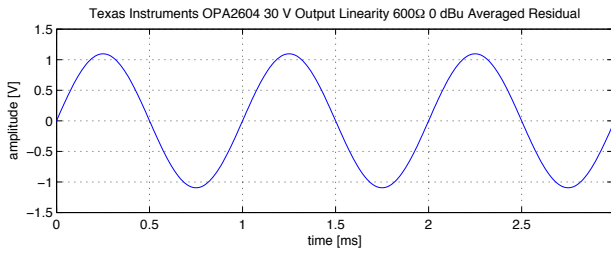
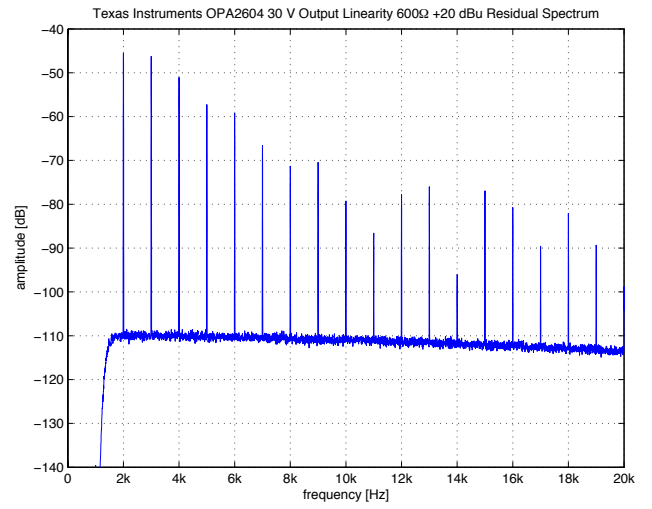
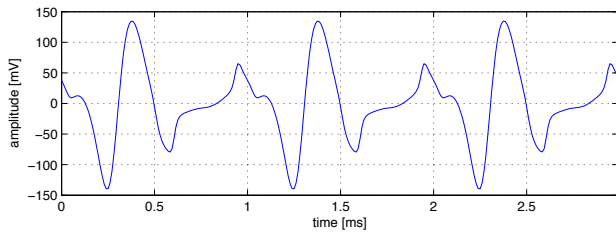
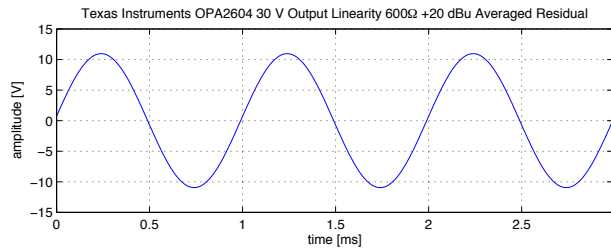
At standard supply voltages this amplifier seems not to be of much use for low distortion applications as there are considerably better devices available at the same (or even lower) cost. May be a simple solution where higher output voltages are needed though.

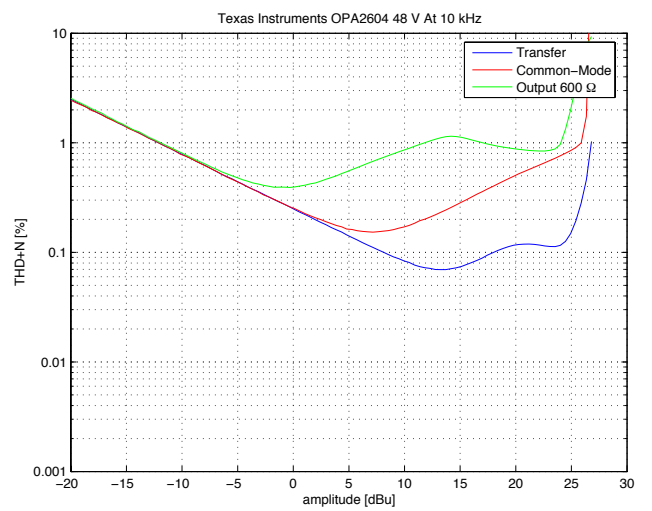
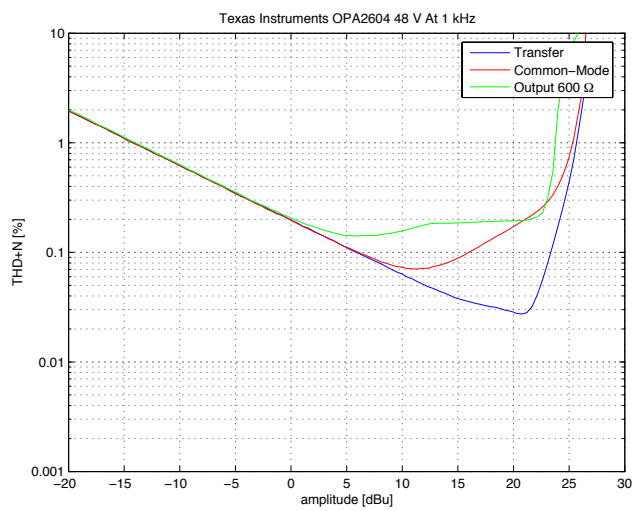
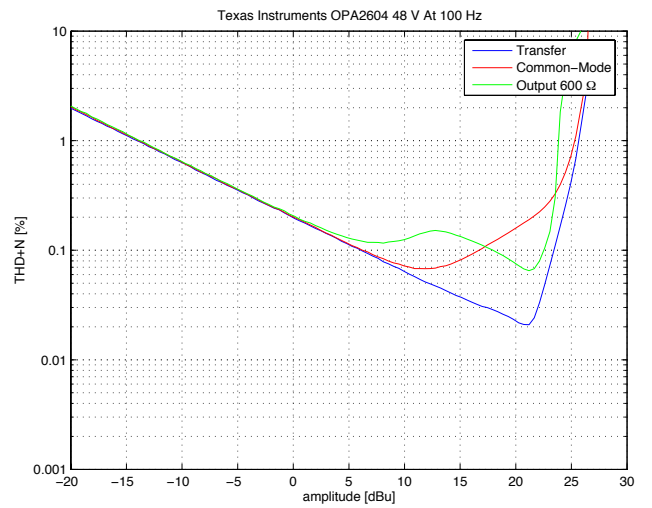
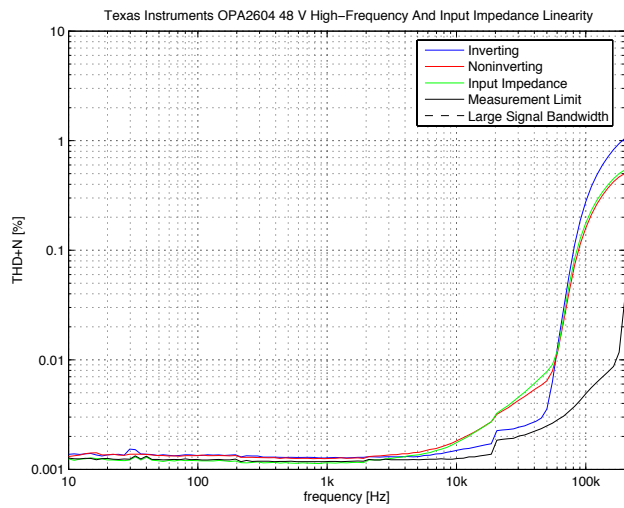
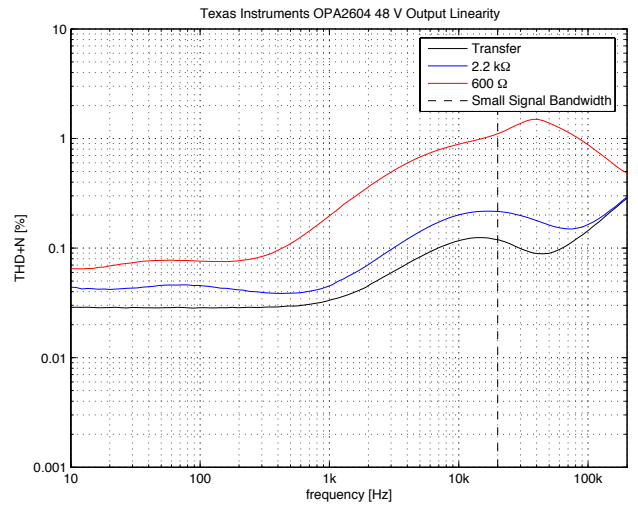
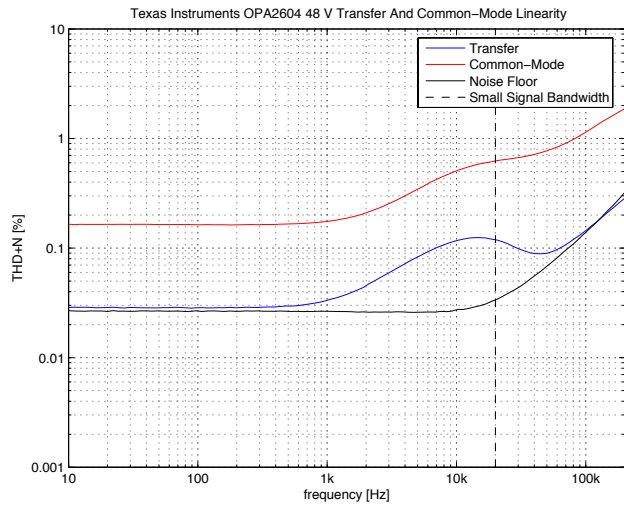


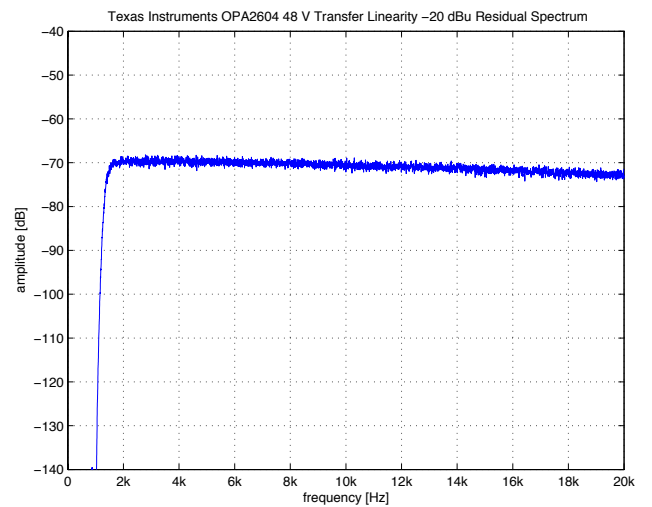
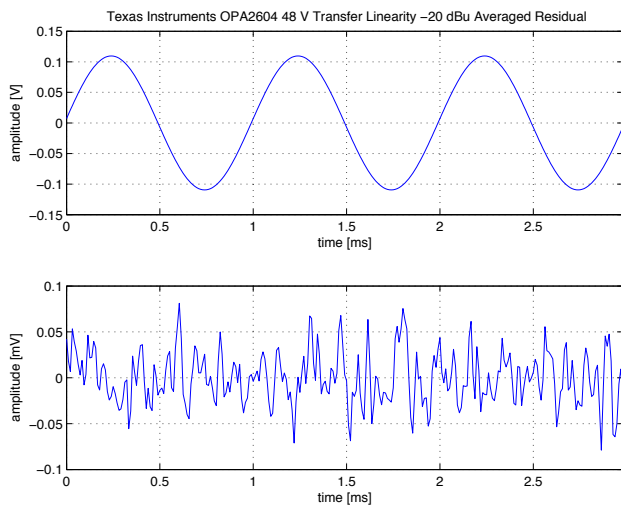
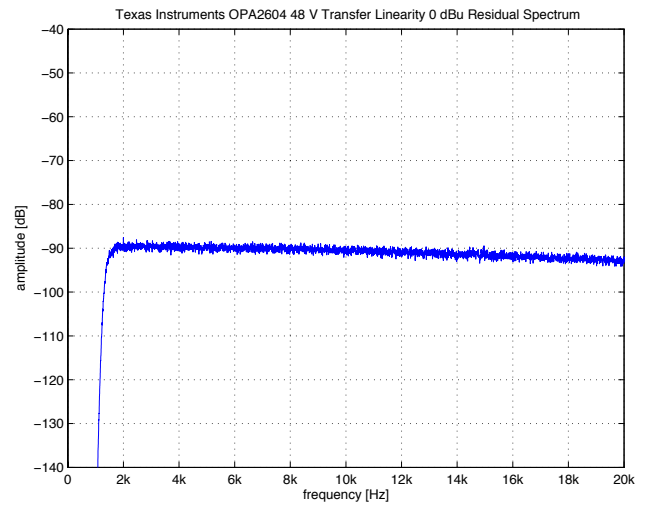
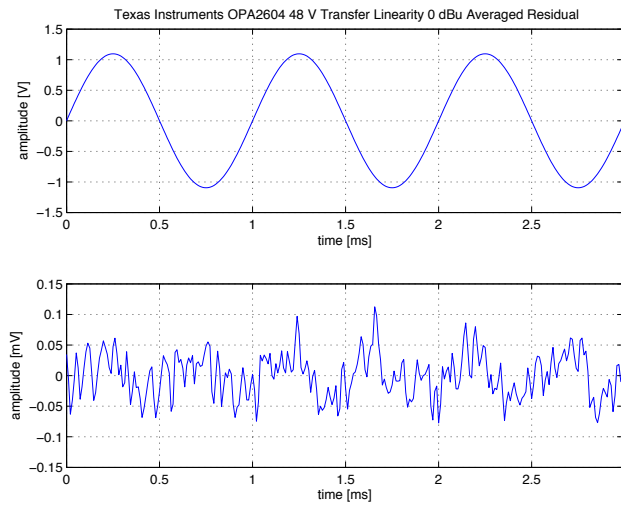
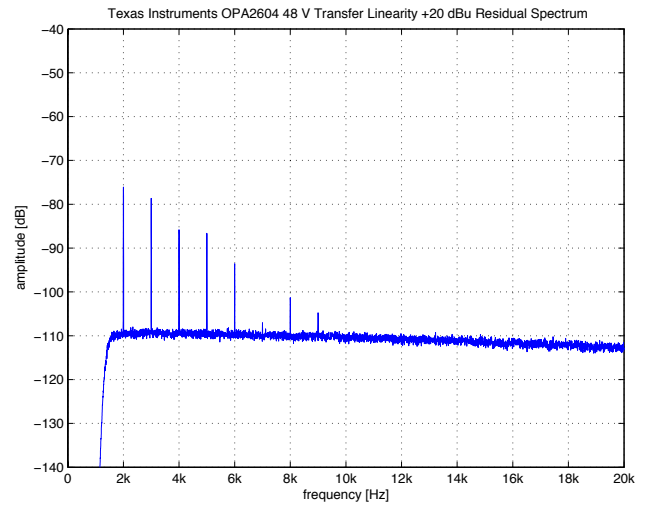
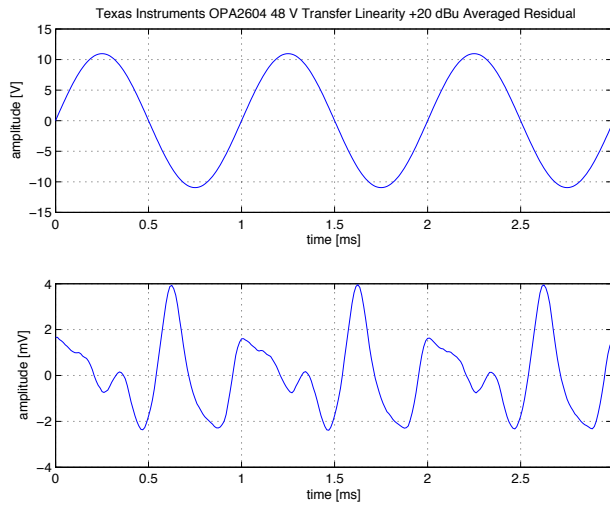


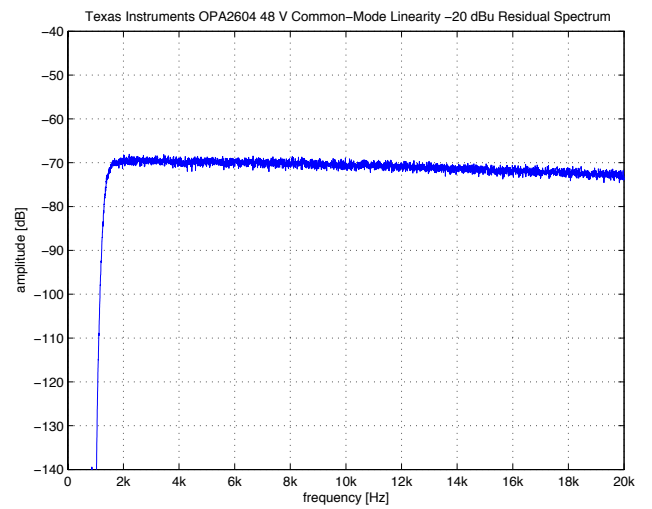
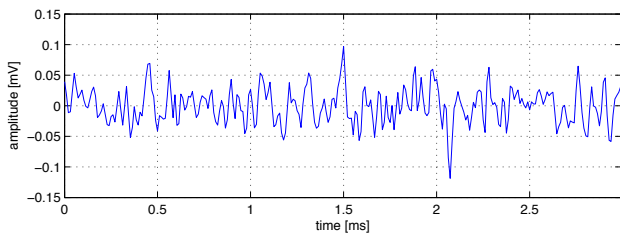
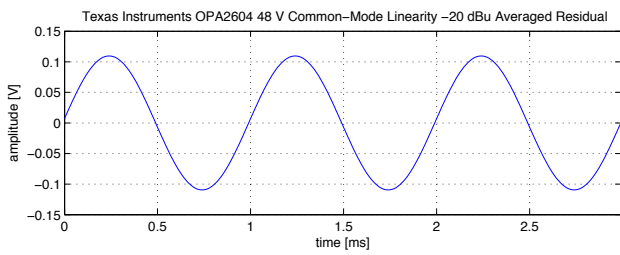
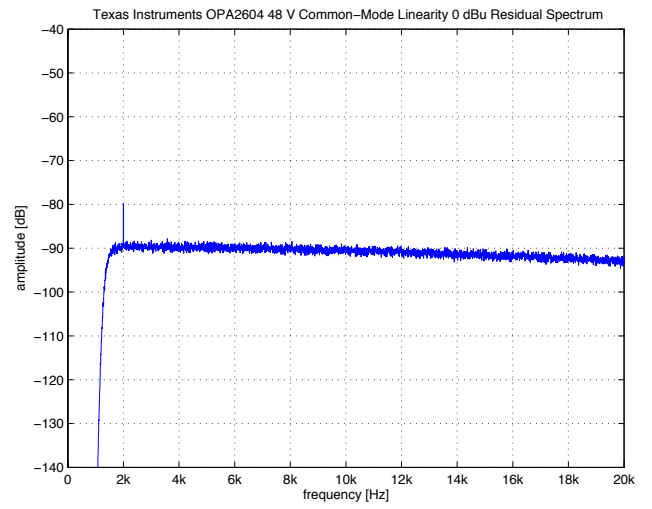
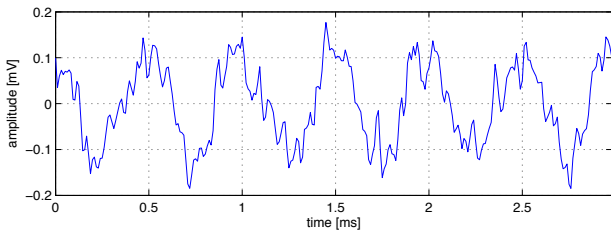
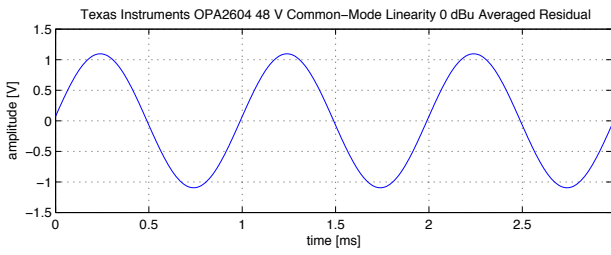
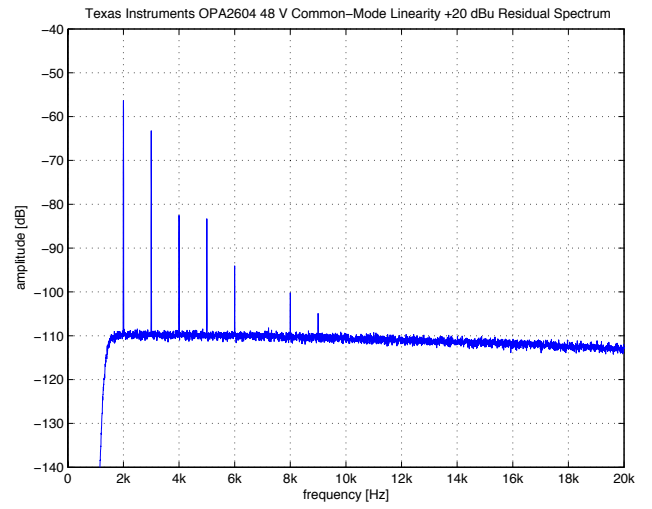
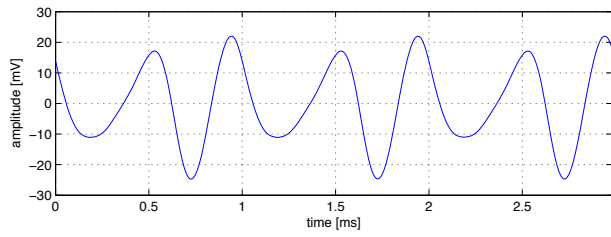
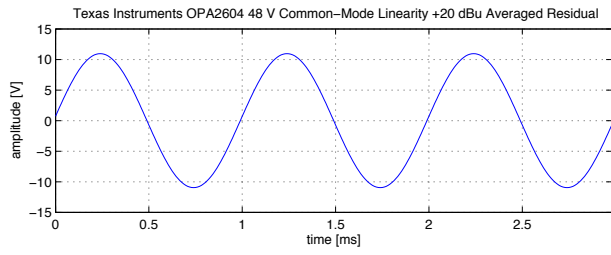


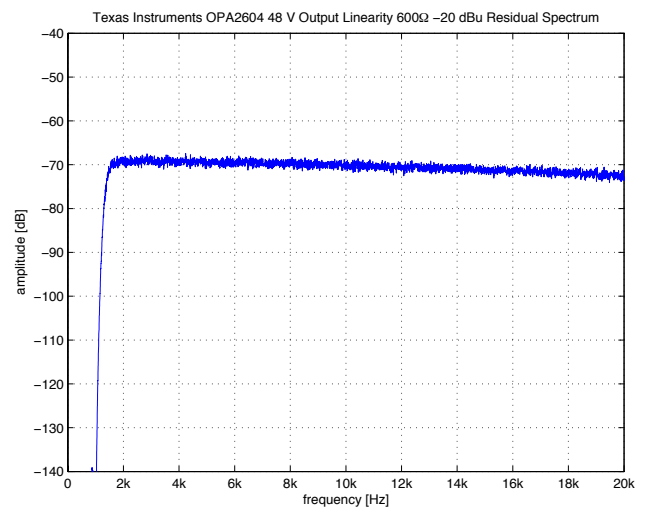
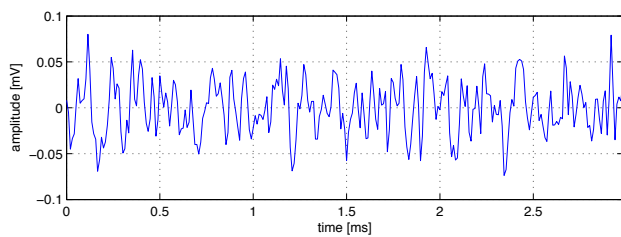
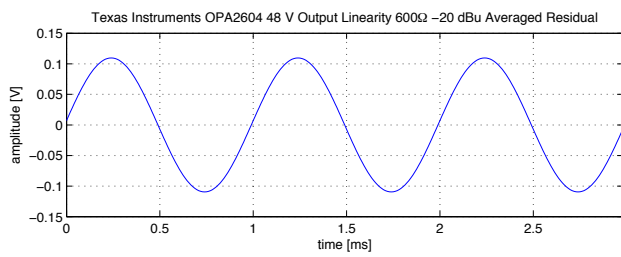
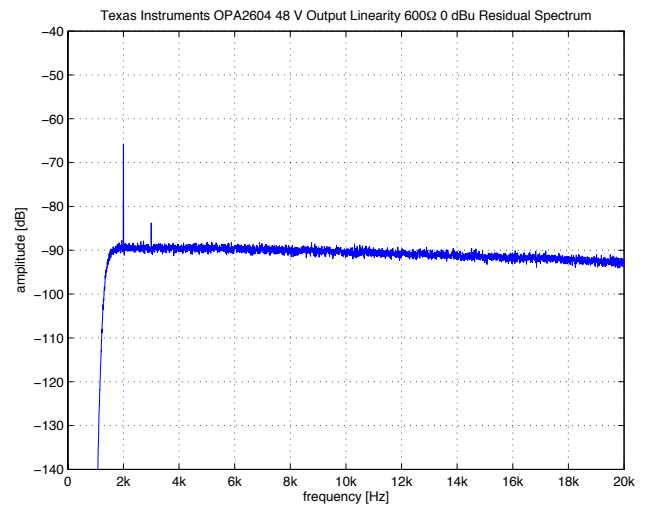
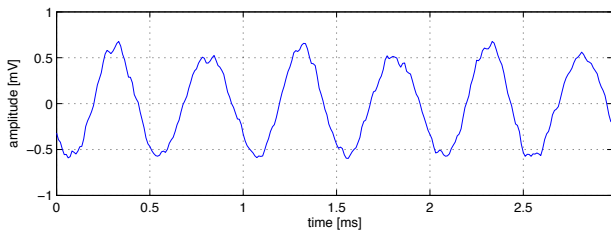
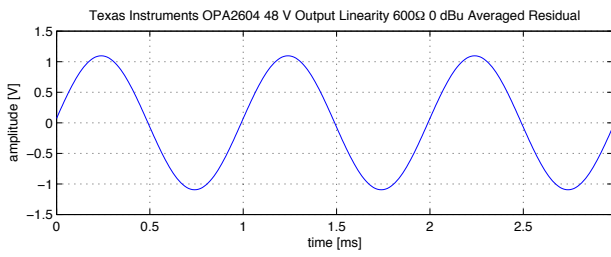
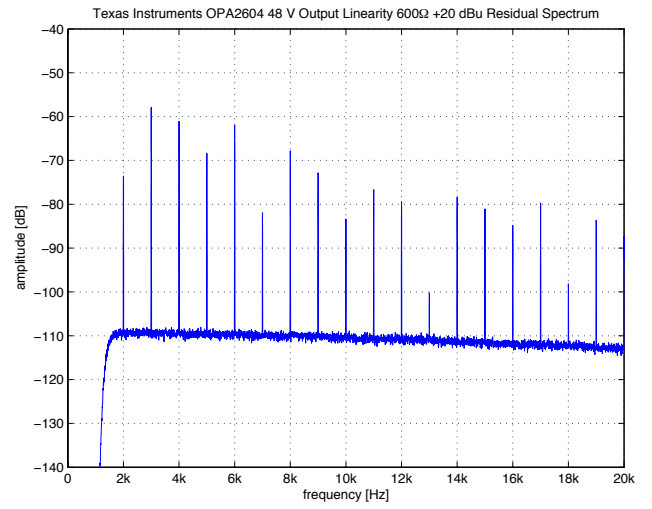
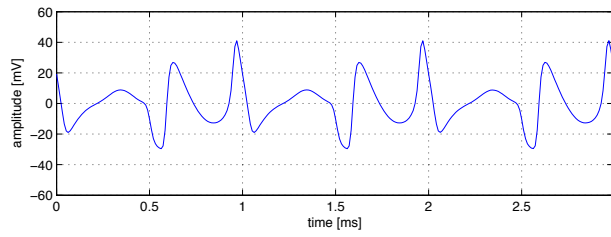
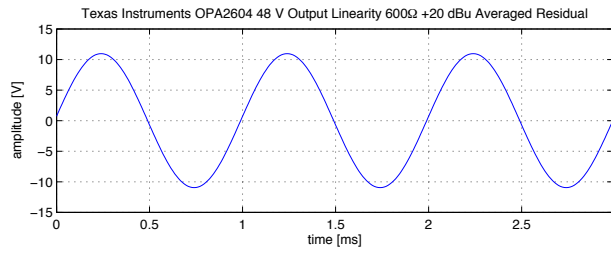












### 3.26 Texas Instruments RC4580

<b>Number of Channels</b>	2
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	0.21 US\$ at 1k units (August 2008)

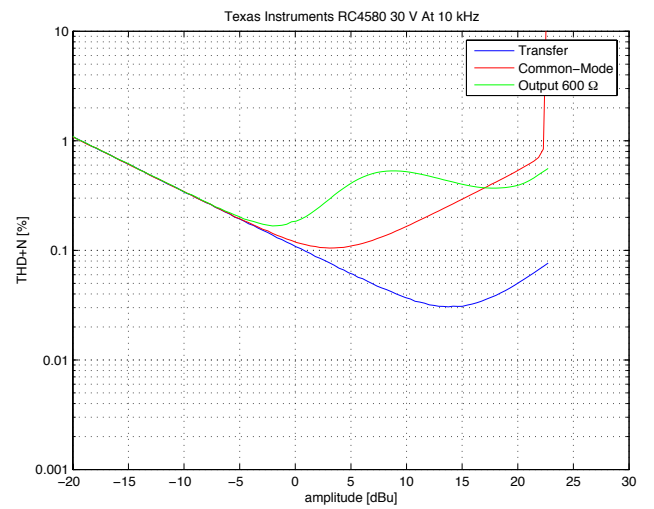
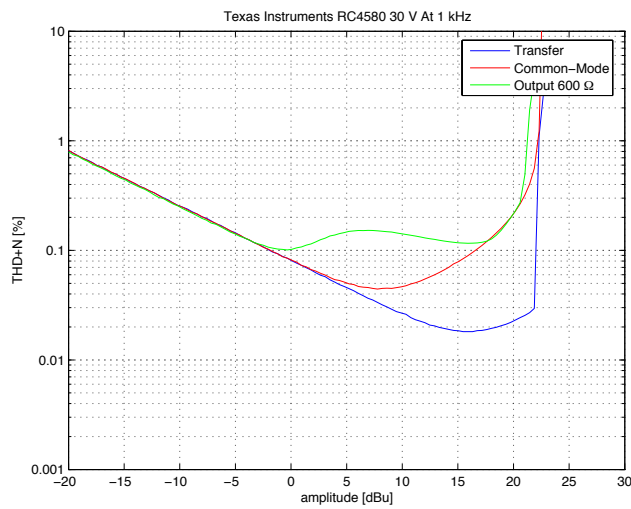
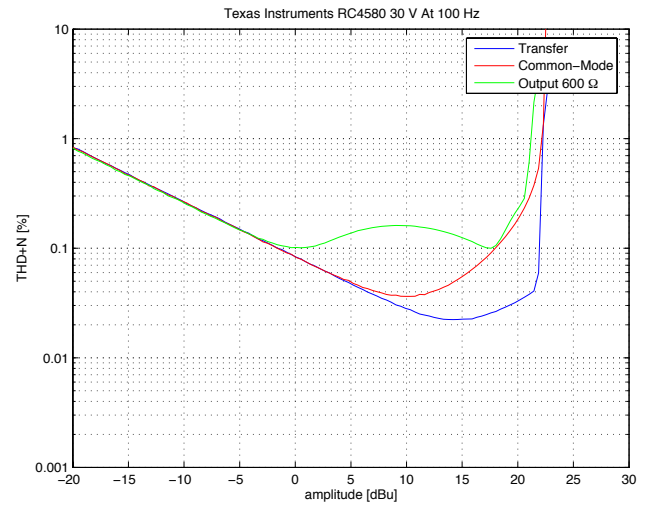
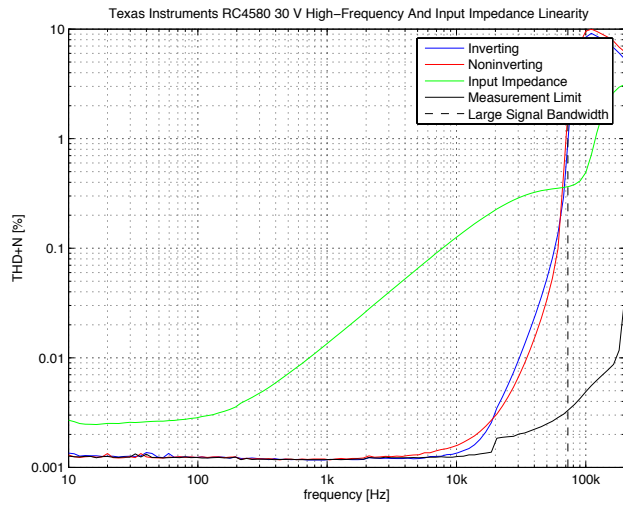
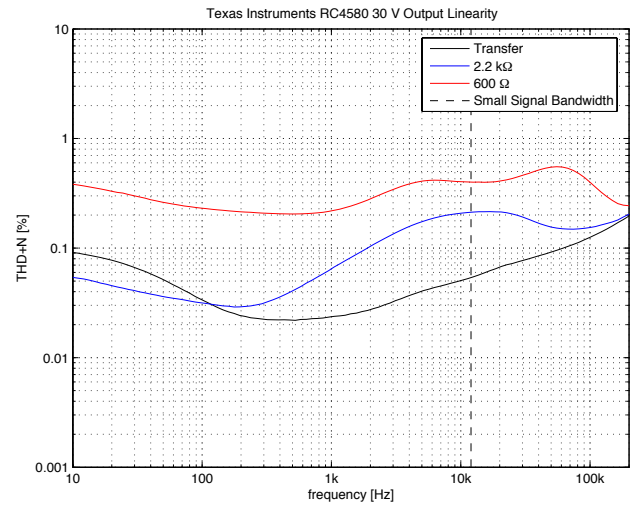
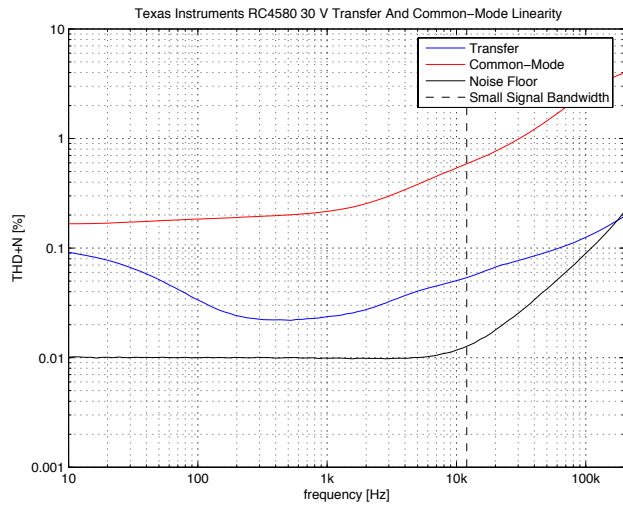
Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		0.5	3	mV
Input Bias Current		100	500	nA
Input Offset Current		5	200	nA
Gain Bandwidth Product		12		MHz
Slew-Rate		5		V/ $\mu$ S
Input Common-Mode Voltage Range	$\pm 12$	$\pm 13.5$		V
Output Voltage Swing ( $R_L = 2\text{ k}\Omega$ )	$\pm 12$	$\pm 13.5$		V
Power Supply Voltage	$\pm 2$		$\pm 18$	V
Quiescent Current per Amplifier		3	4.5	mA

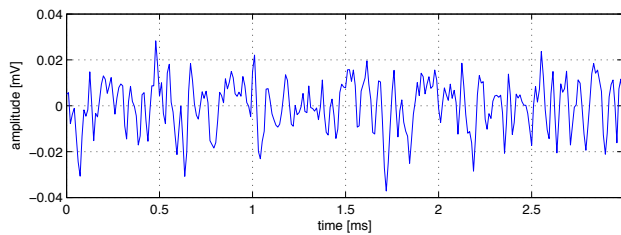
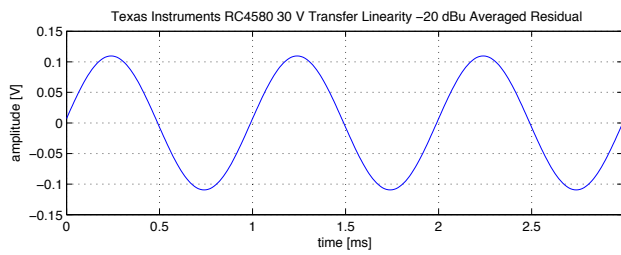
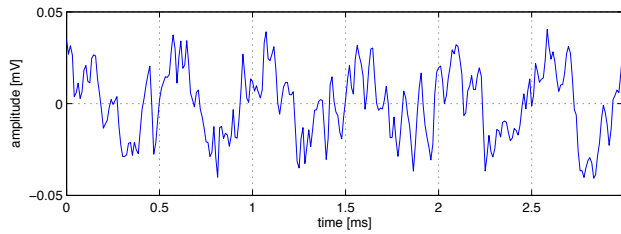
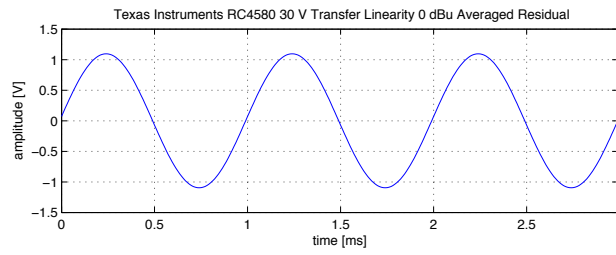
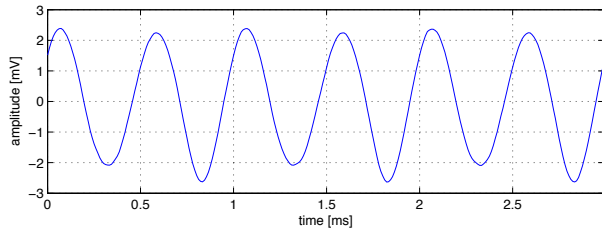
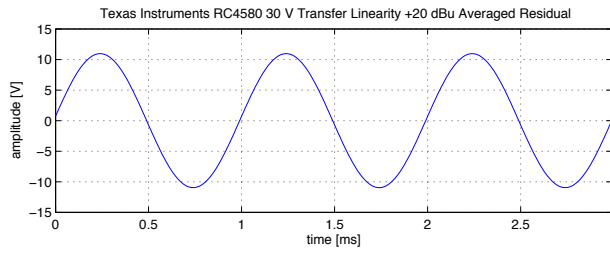
Table 3.26: Specifications for  $T_A = 25^\circ\text{C}$  and  $V_S = \pm 15\text{ V}$ .

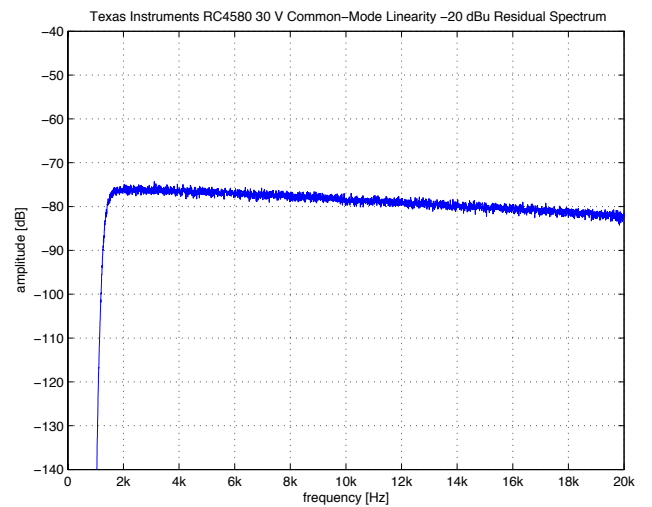
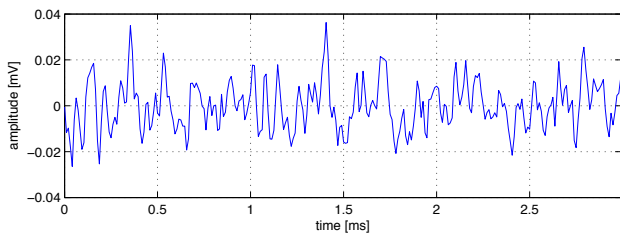
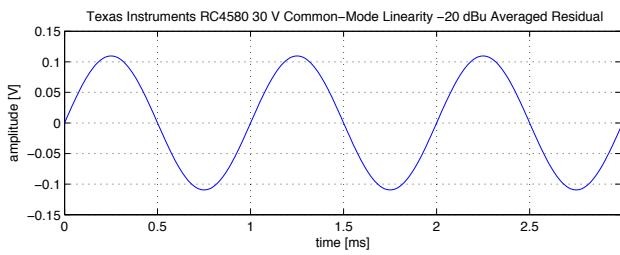
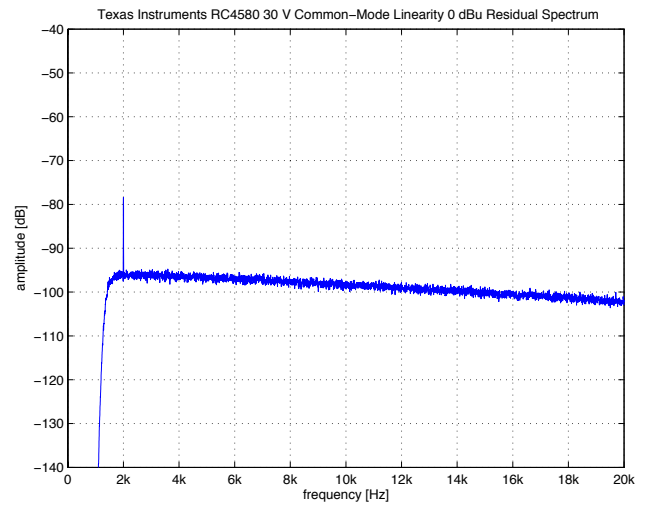
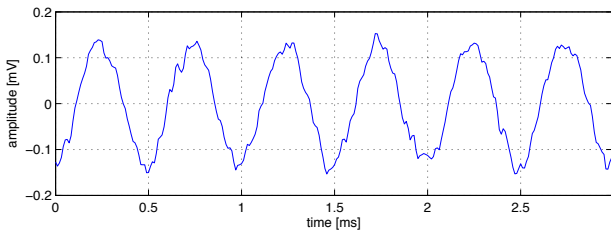
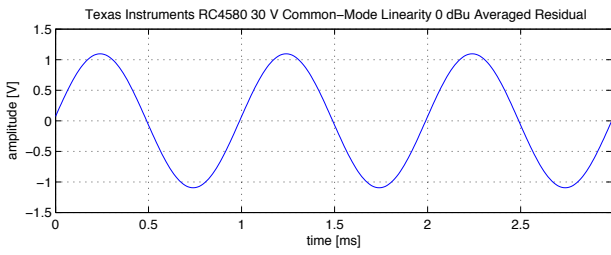
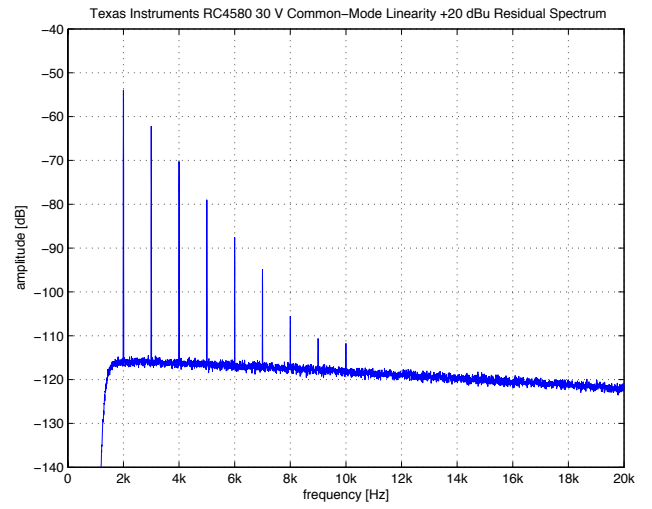
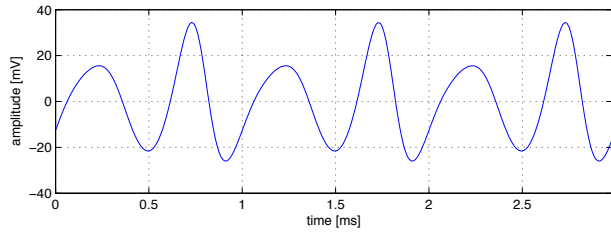
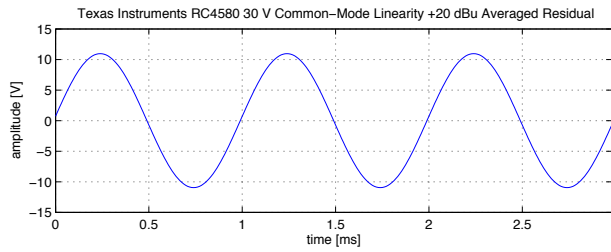
A bipolar amplifier using a two-stage architecture—according to the manufacturer’s datasheet specifically optimised for audio applications. Note the sparse specifications, even lacking a detailed noise specification.

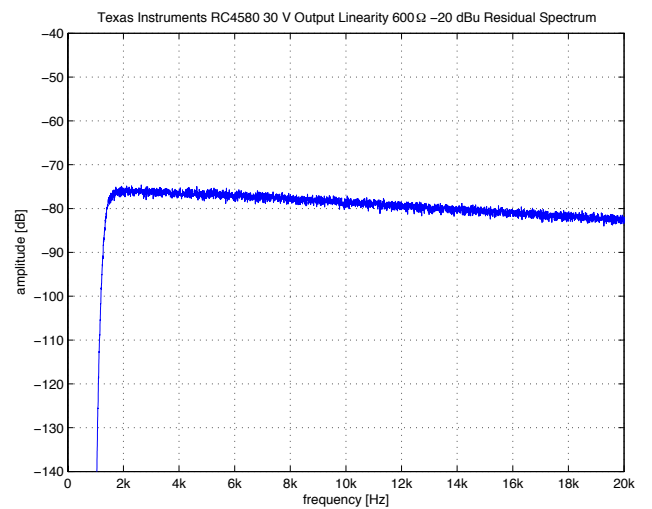
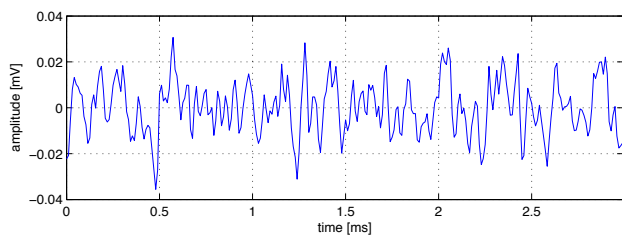
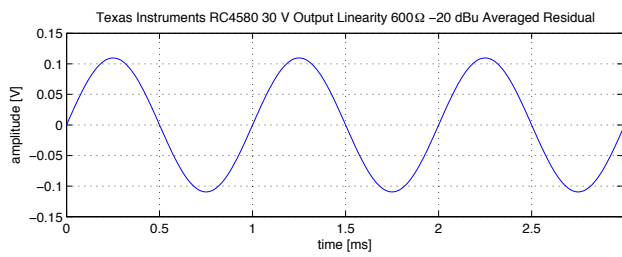
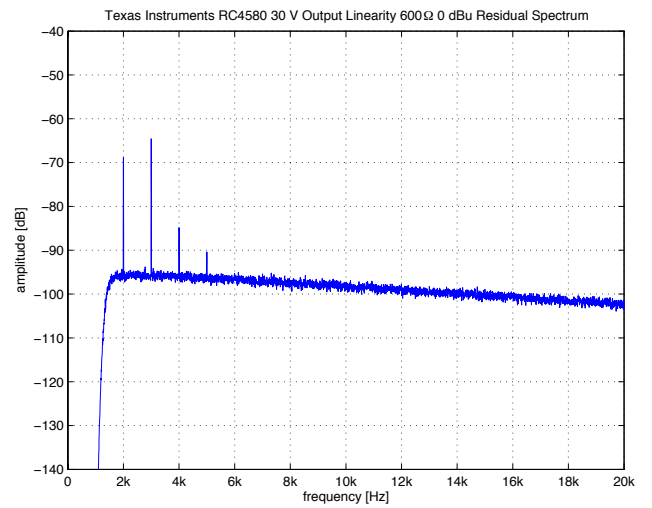
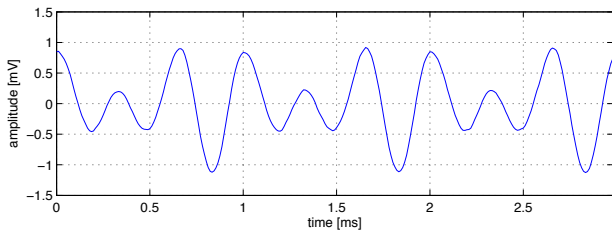
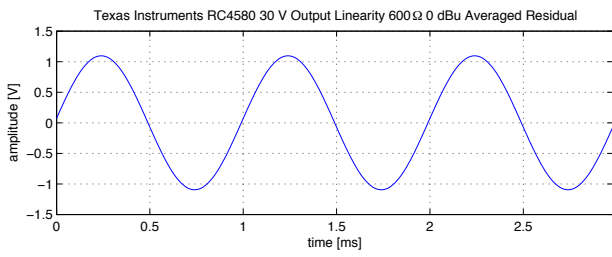
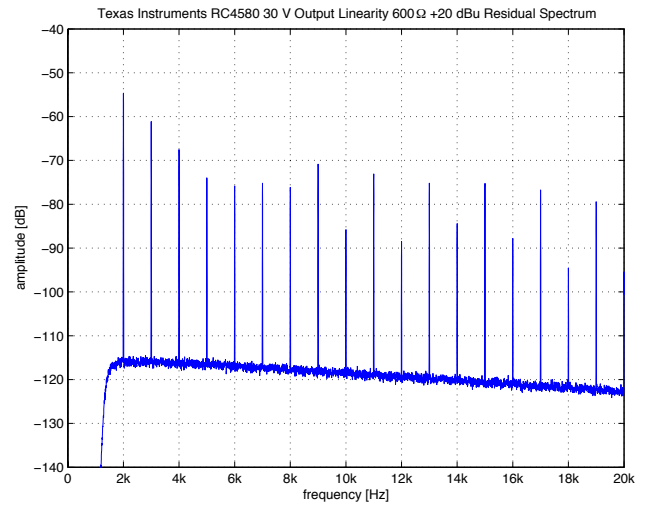
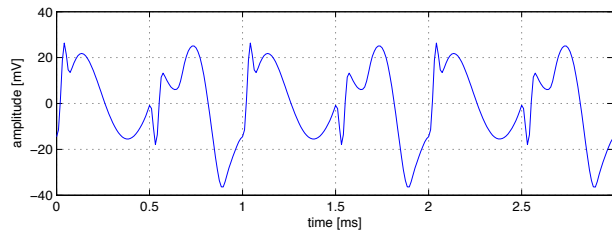
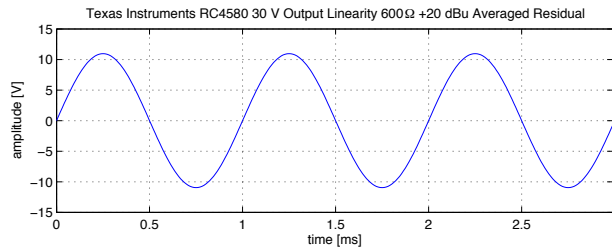
All tests indicate modest performance; there are better opamps available at the same or even lower cost.











## 3.27 Texas Instruments TL071

<b>Number of Channels</b>	1
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	0.22 US\$ at 1k units (August 2008)

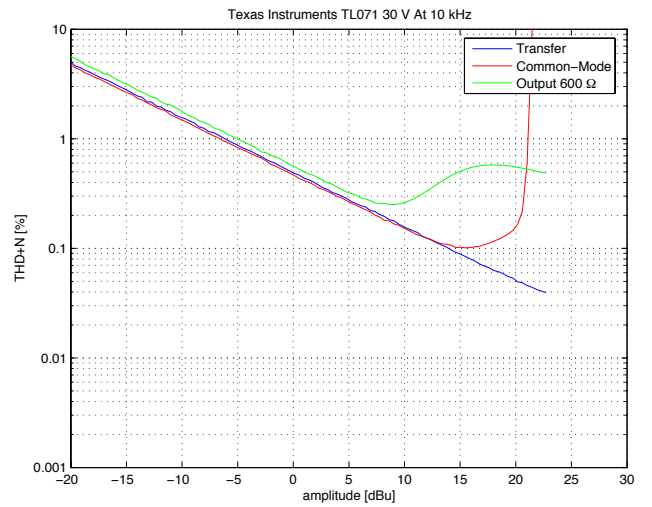
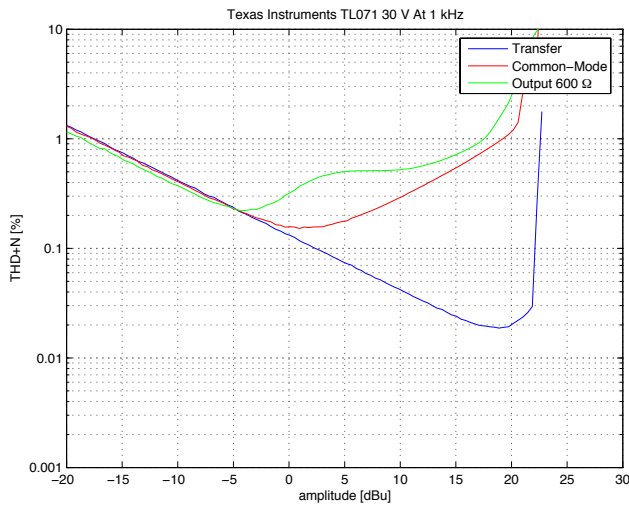
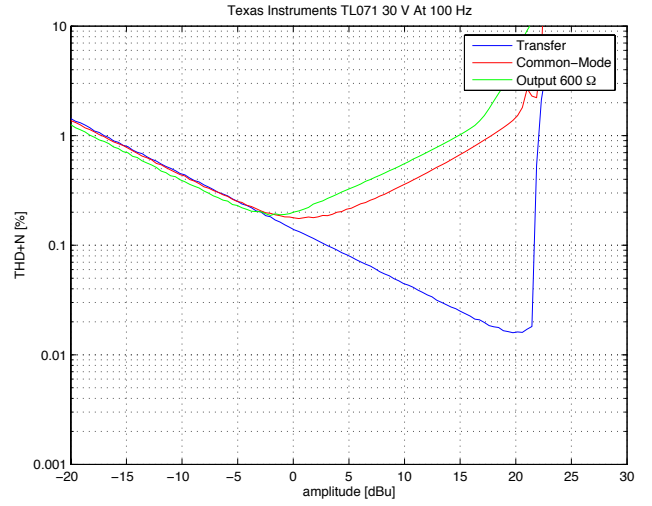
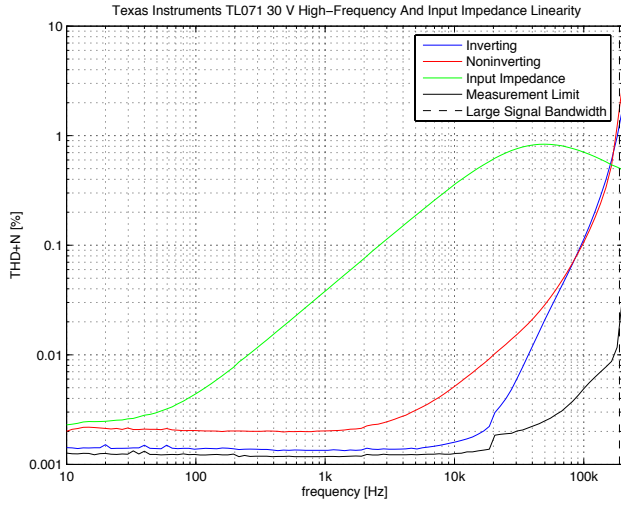
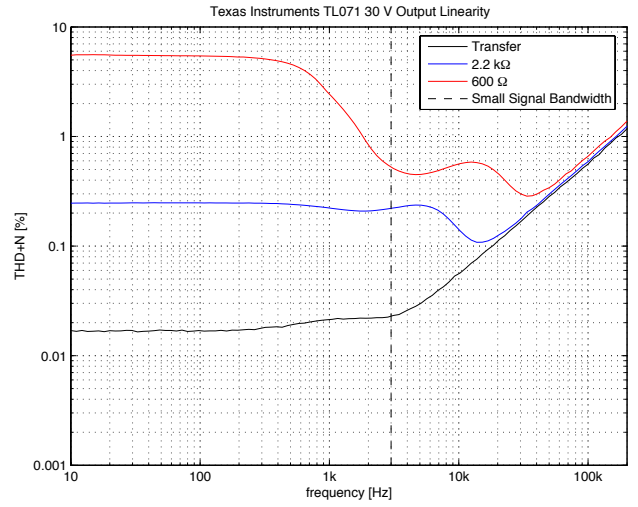
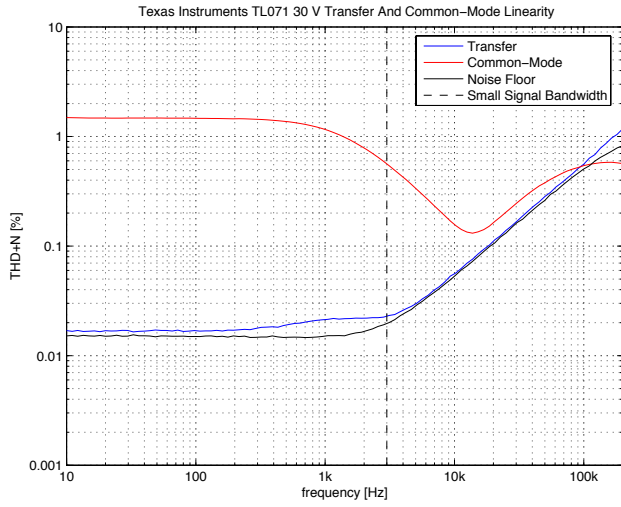
Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		3	10	mV
Input Bias Current		65	200	pA
Input Offset Current		5	100	pA
Gain Bandwidth Product		3		MHz
Slew-Rate	8	13		V/ $\mu$ S
Input Voltage Noise (f = 1 kHz)		18		nV/ $\sqrt{\text{Hz}}$
Input Current Noise (f = 1 kHz)		10		fA/ $\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 11$	+15/-12		V
Output Voltage Swing ( $R_L = 2 \text{ k}\Omega$ )	$\pm 10$			V
Power Supply Voltage			$\pm 18$	V
Quiescent Current per Amplifier		1.4	2.5	mA

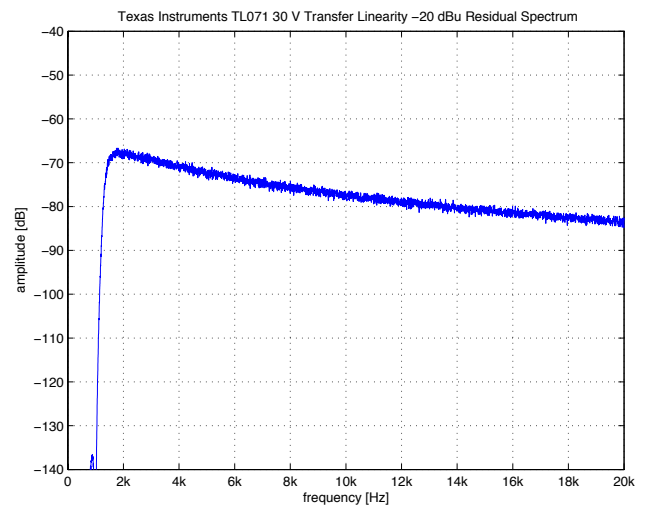
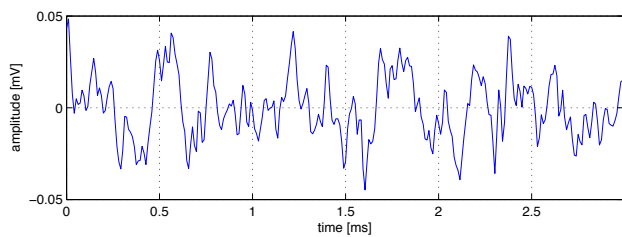
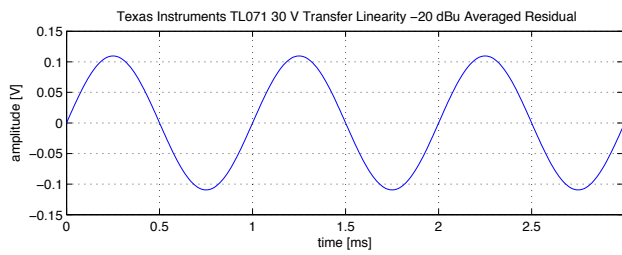
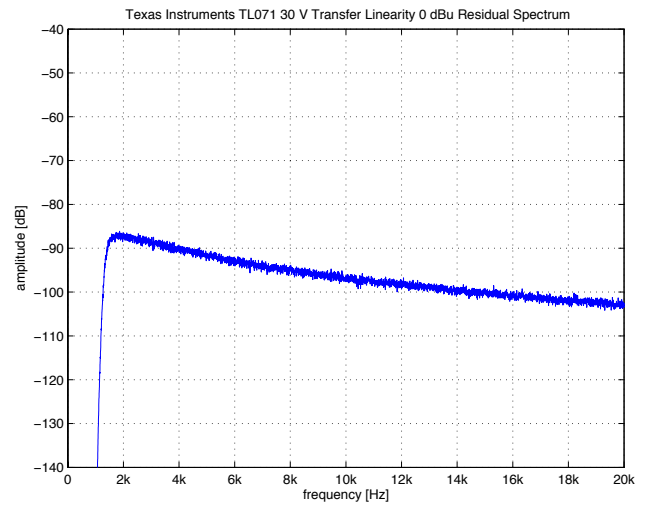
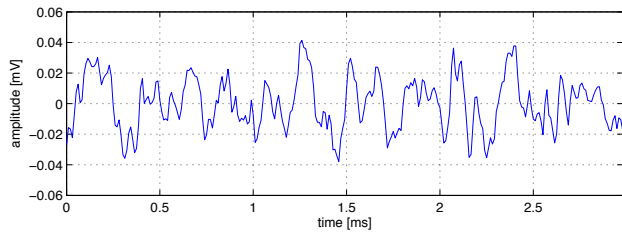
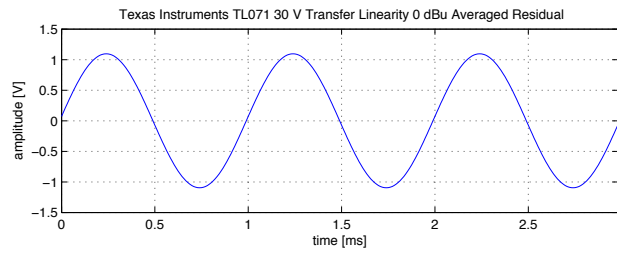
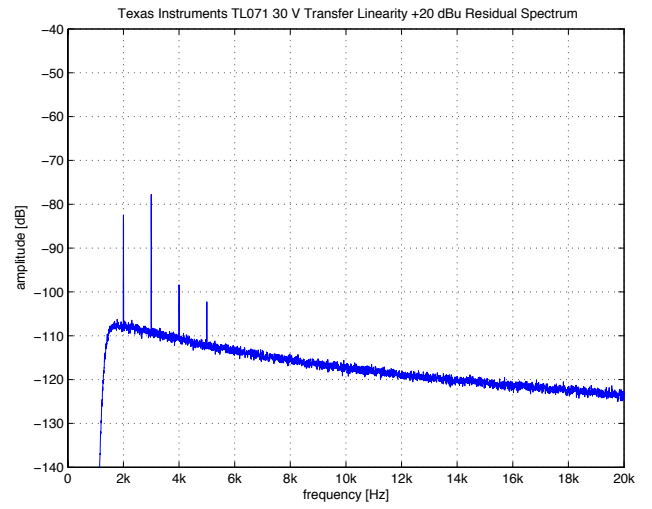
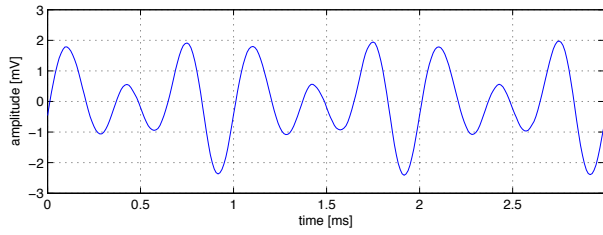
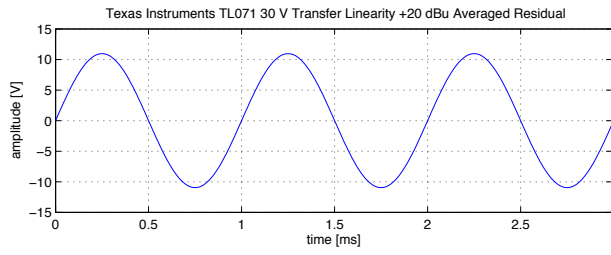
Table 3.27: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 15 \text{ V}$ .

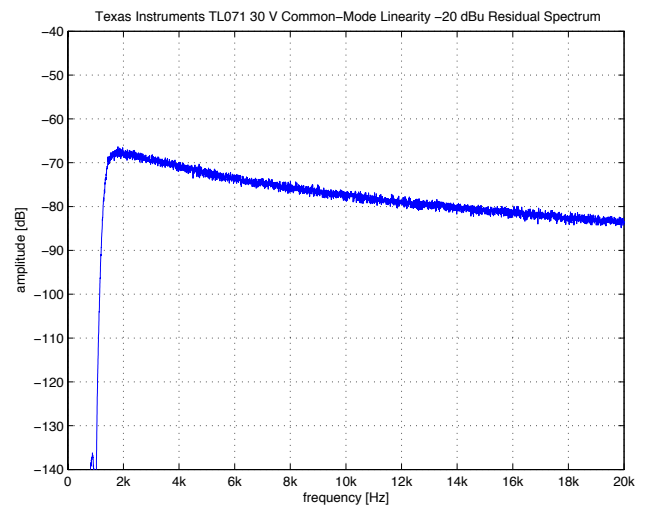
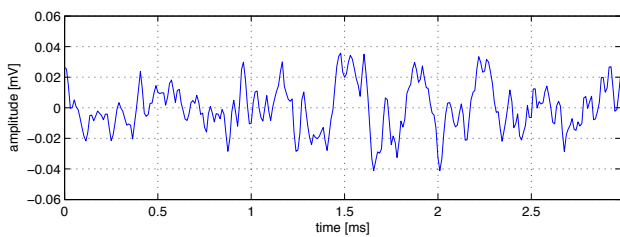
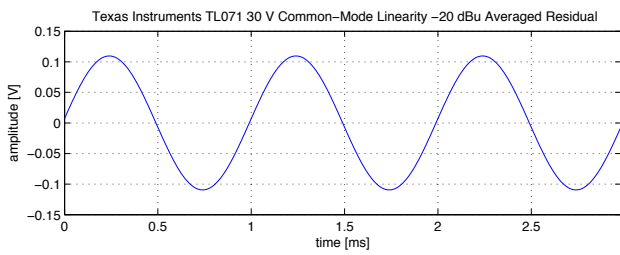
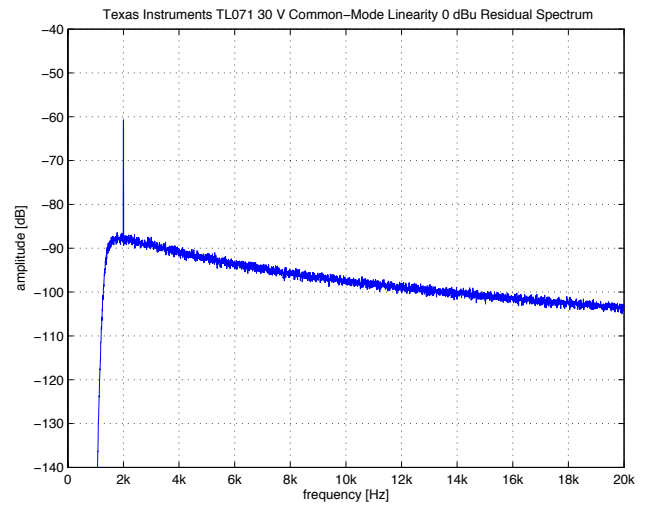
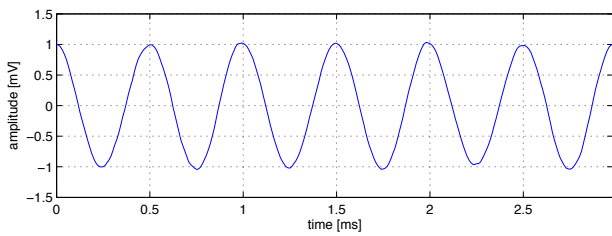
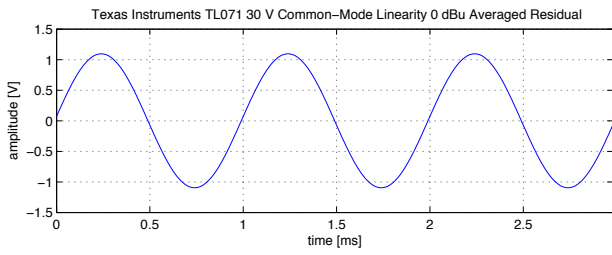
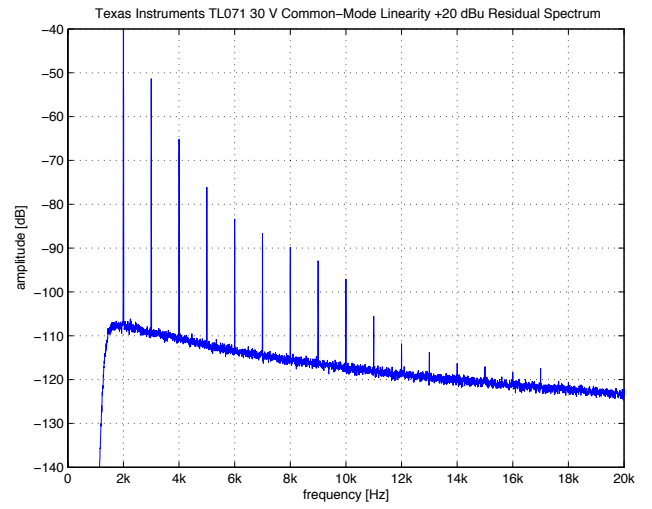
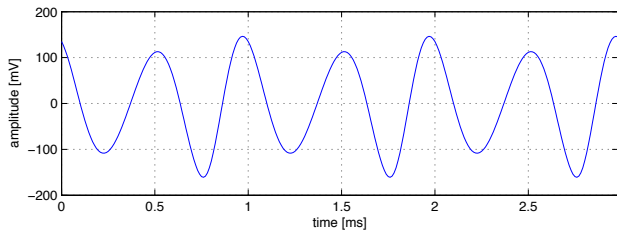
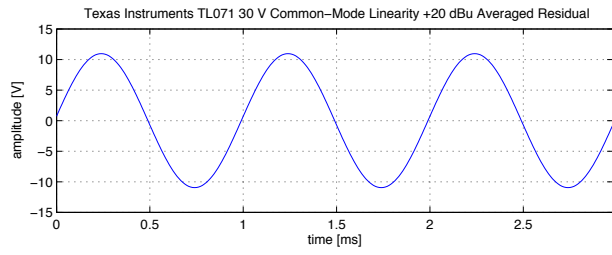
An early JFET amplifier using a two-stage topology. Trimming pins are available. Quiescent current is low, but the resulting voltage noise very high. Note the distinct asymmetric common-mode input voltage range. Dual and quad amplifiers (TL072 and TL074) are available.

The transfer linearity is relatively good within the audio band, at high-frequency the linearity decreased though although the slew-rate of the amplifier is comparatively high. Common-mode, input impedance and output loading linearity are all pretty poor. Due to the low gain bandwidth product the THD+N vs. amplitude plots at 10 kHz are of little significance as the small-signal bandwidth of the measurements setup is below that frequency.

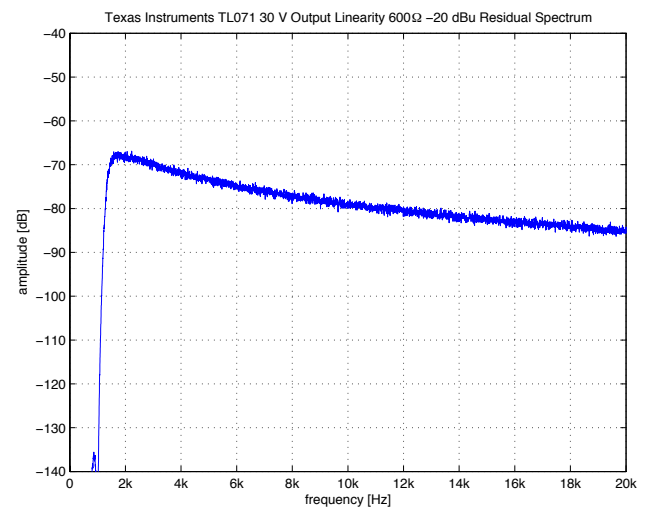
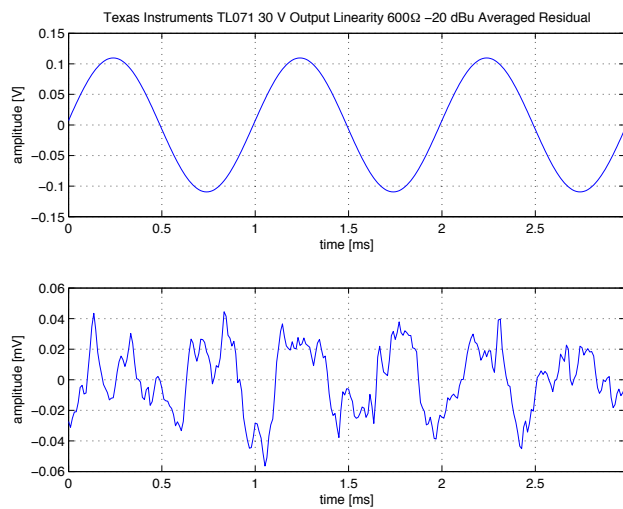
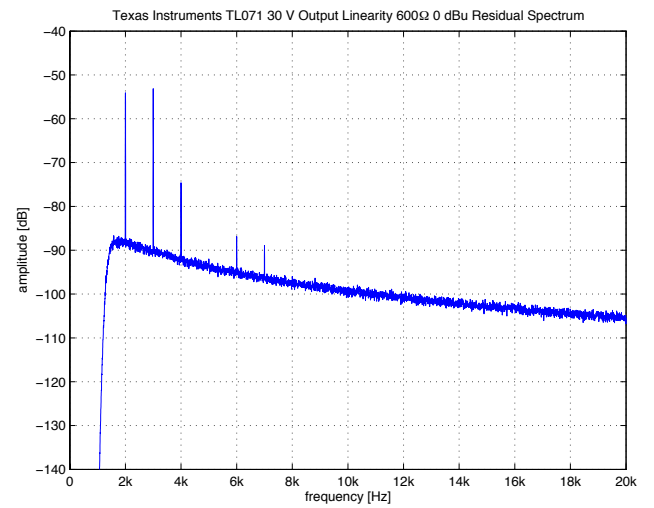
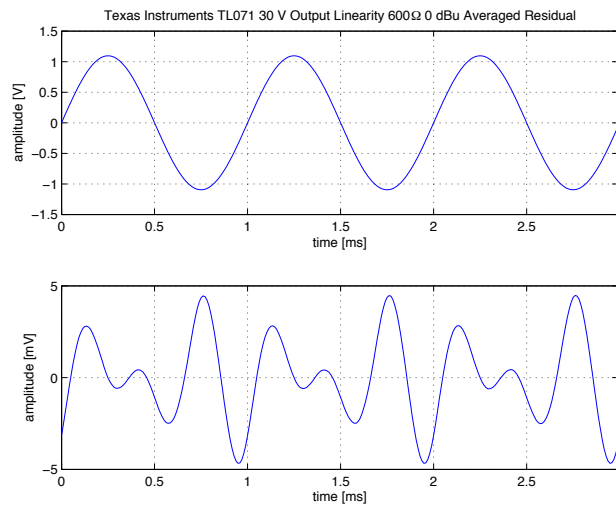
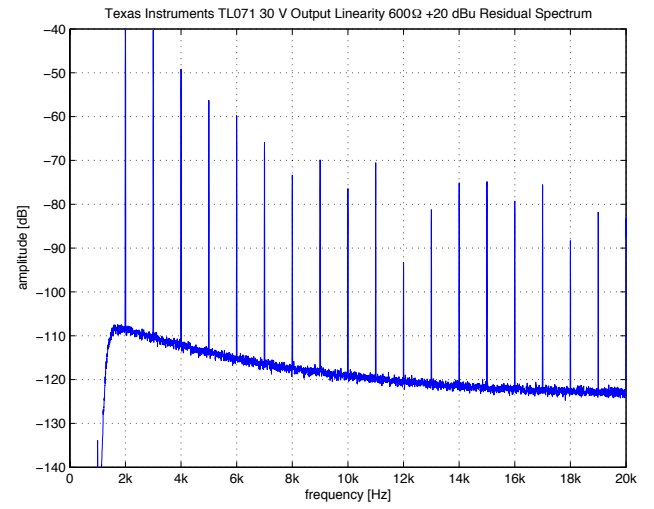
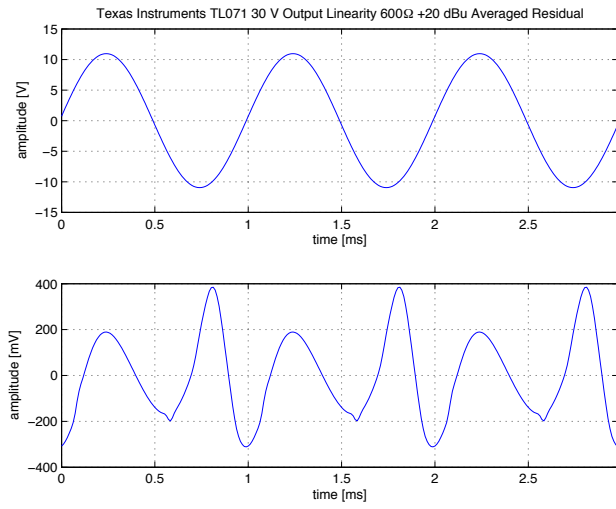
Perhaps usable where only the basic transfer linearity comes into play and where low quiescent current and cost are needed. Otherwise surpassed by recent amplifiers.











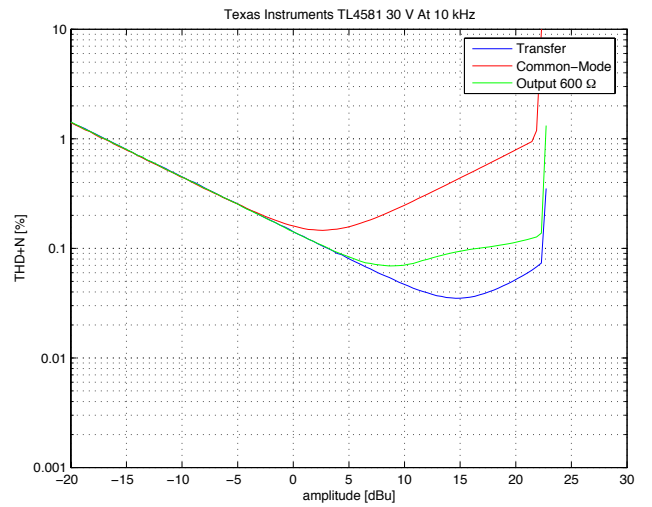
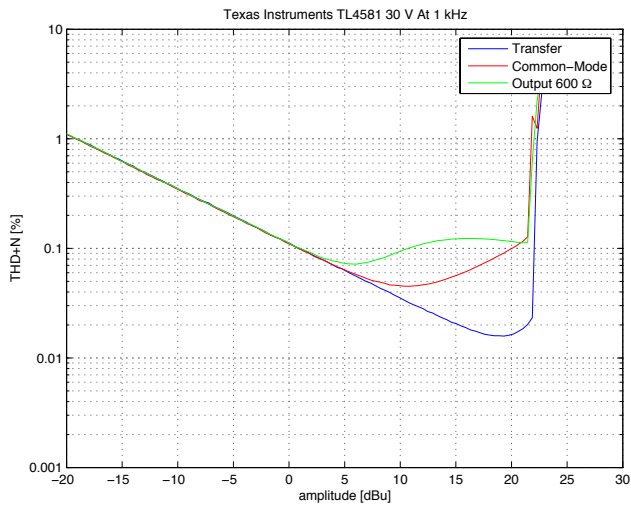
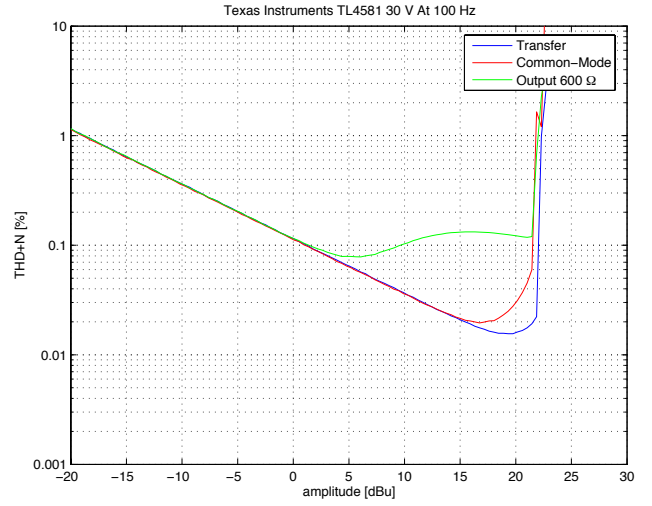
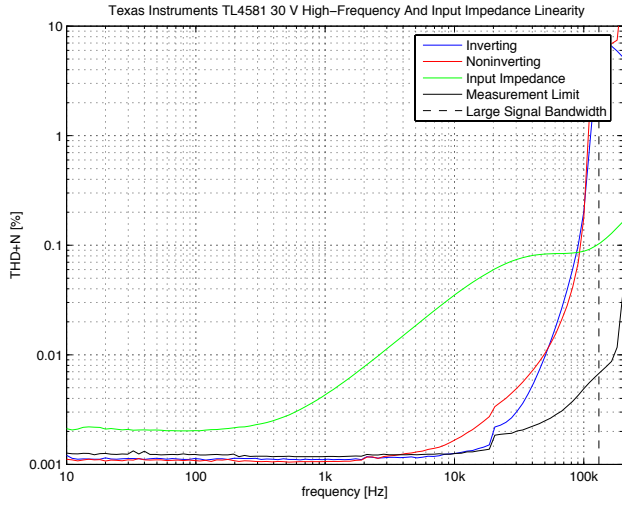
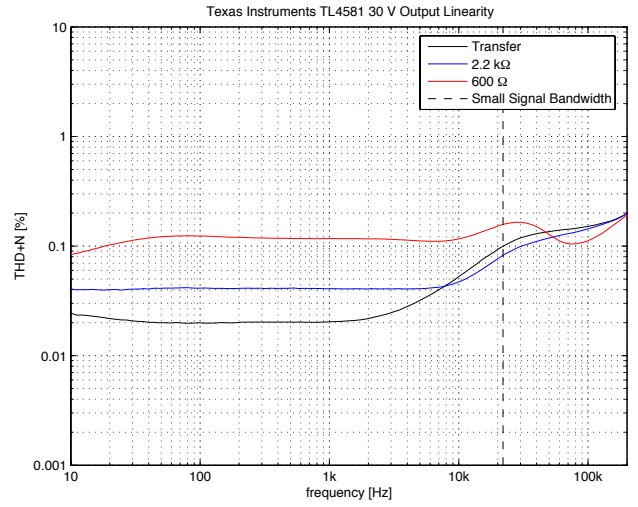
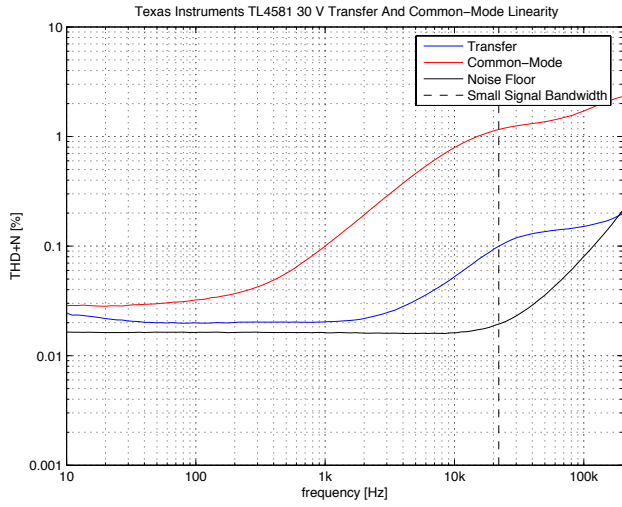
## 3.28 Texas Instruments TL4581

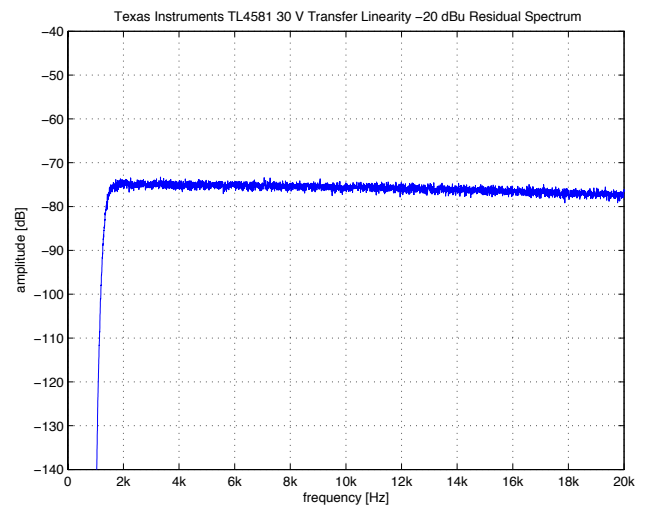
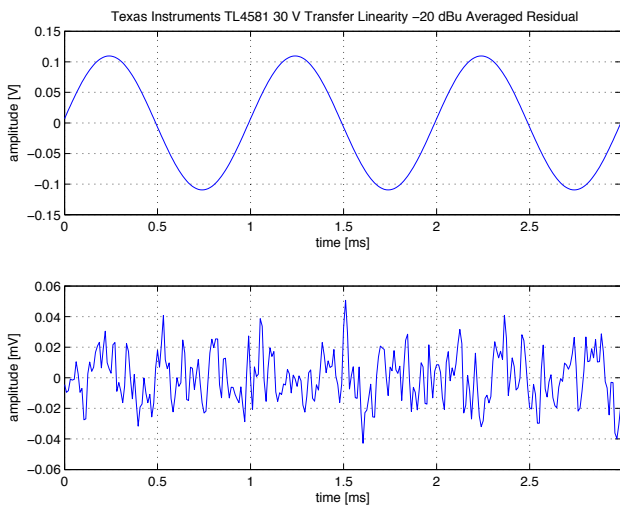
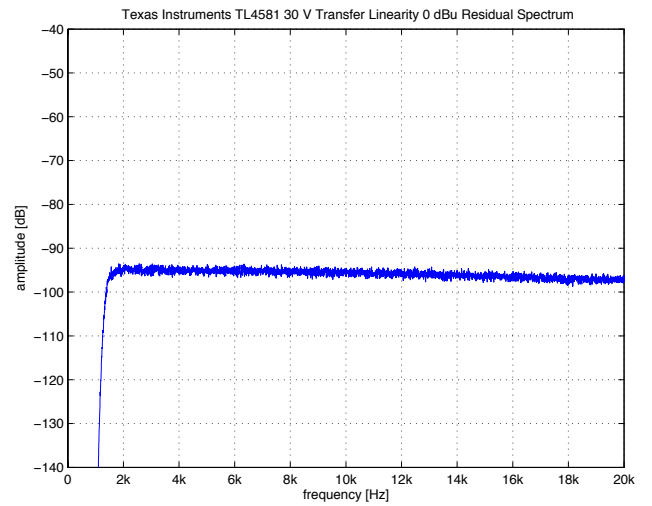
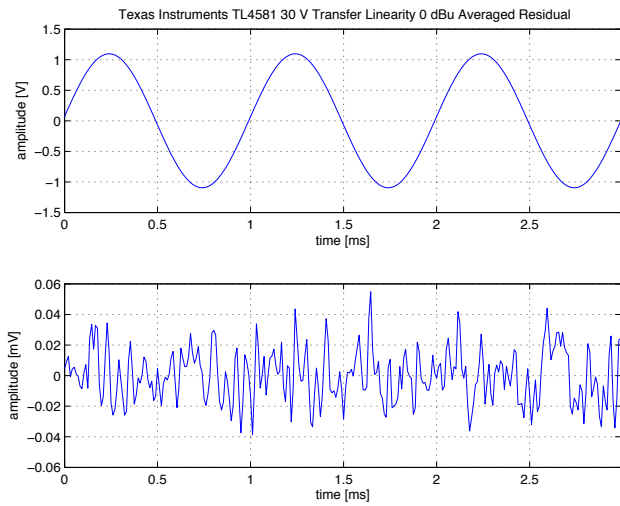
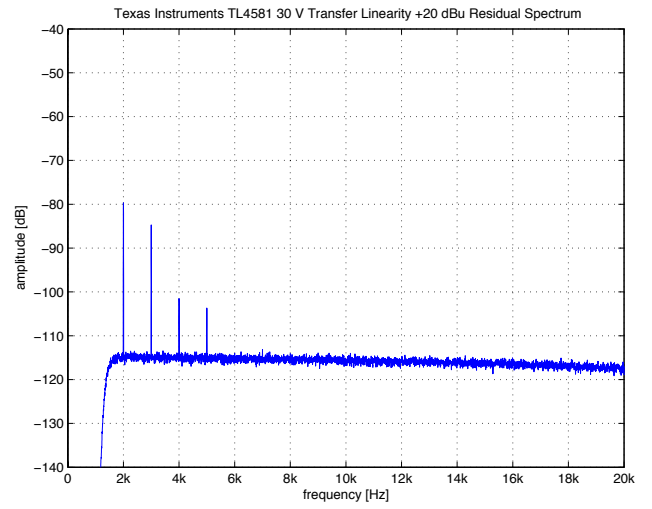
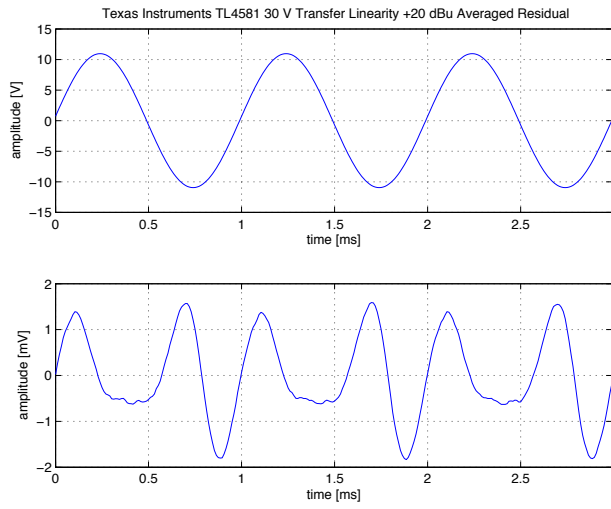
<b>Number of Channels</b>	2
<b>Packages</b>	DIP, SOIC
<b>Cost per Amplifier</b>	0.23 US\$ at 1k units (August 2008)

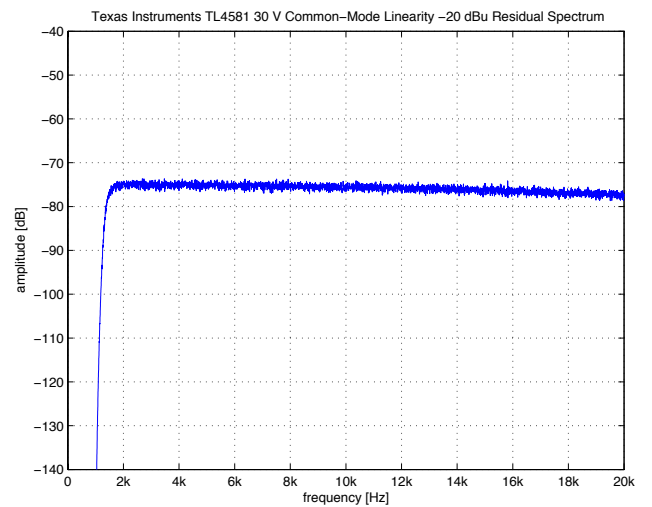
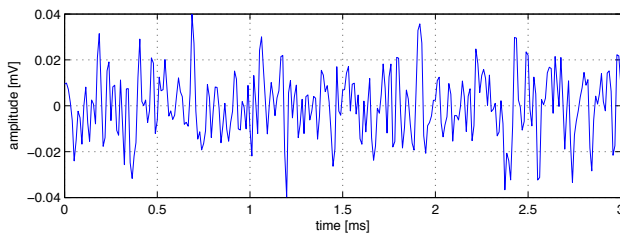
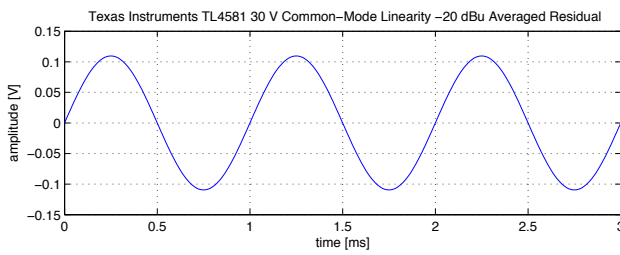
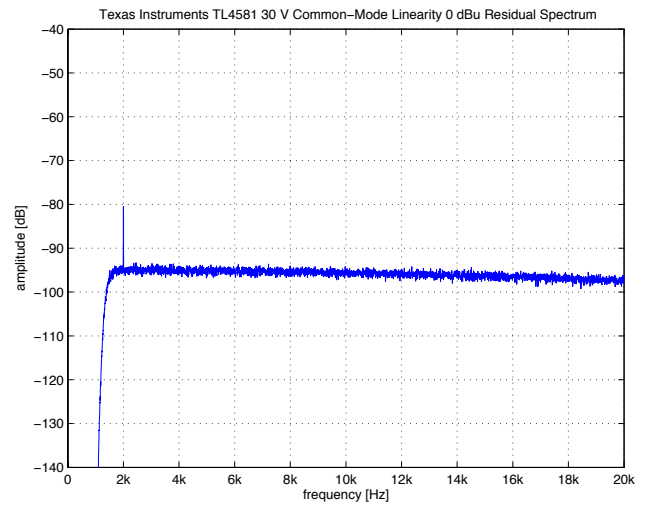
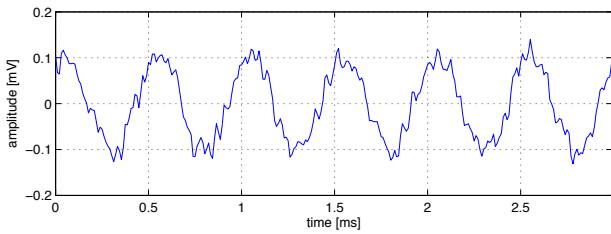
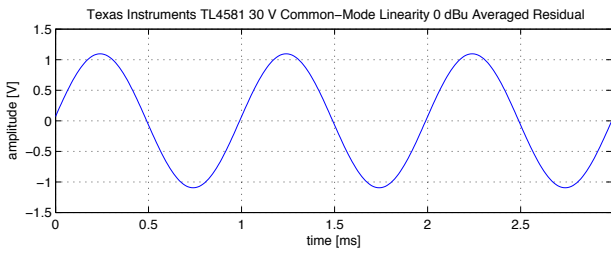
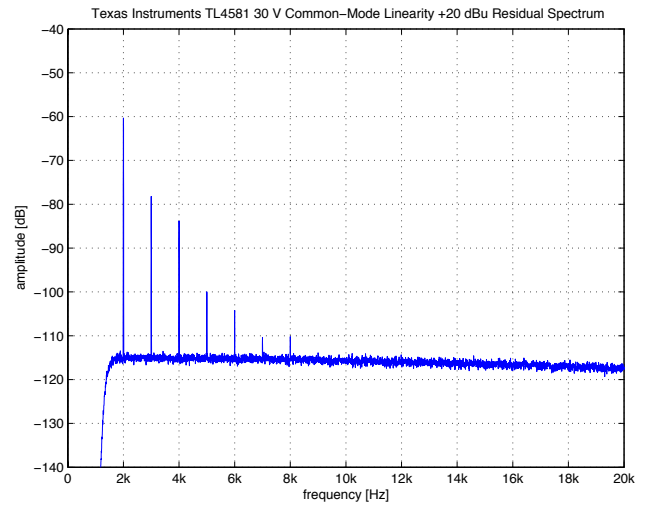
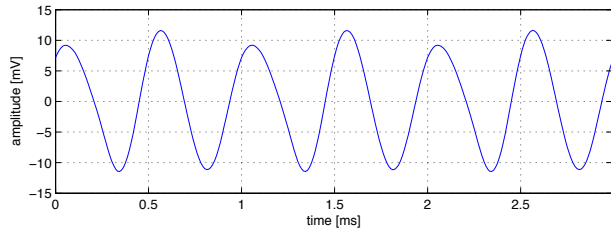
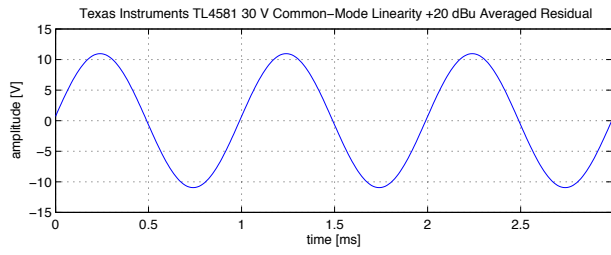
Parameter	Minimum	Typical	Maximum	Unit
Input Offset Voltage		0.5	4	mV
Input Bias Current		200	800	nA
Input Offset Current		10	150	nA
Gain Bandwidth Product		22		MHz
Slew-Rate		9		V/ $\mu$ S
Input Voltage Noise (f = 1 kHz)		5		nV/ $\sqrt{\text{Hz}}$
Input Current Noise (f = 1 kHz)		0.7		pA/ $\sqrt{\text{Hz}}$
Input Common-Mode Voltage Range	$\pm 12$	$\pm 13$		V
Output Voltage Swing ( $R_L = 600 \Omega$ )	$\pm 12$	$\pm 13$		V
Power Supply Voltage	$\pm 3$		$\pm 22$	V
Quiescent Current per Amplifier		4	8	mA

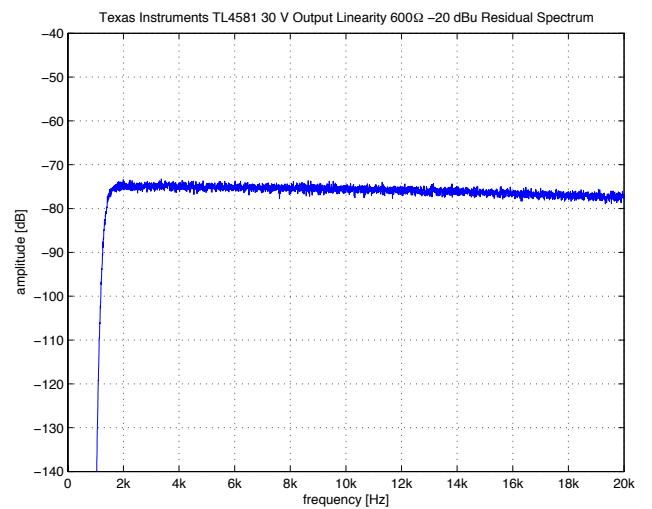
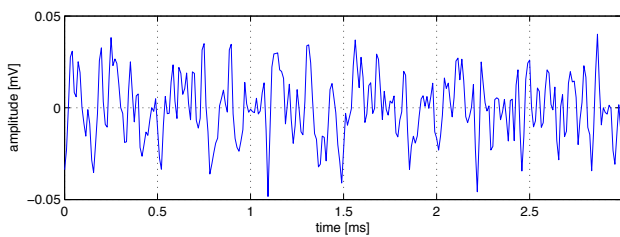
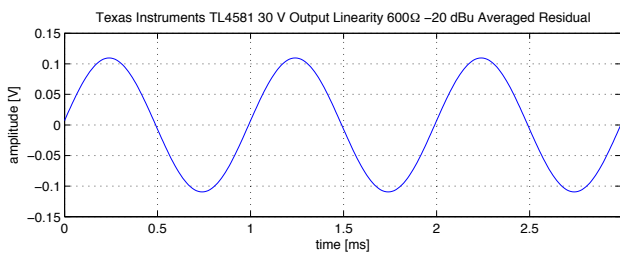
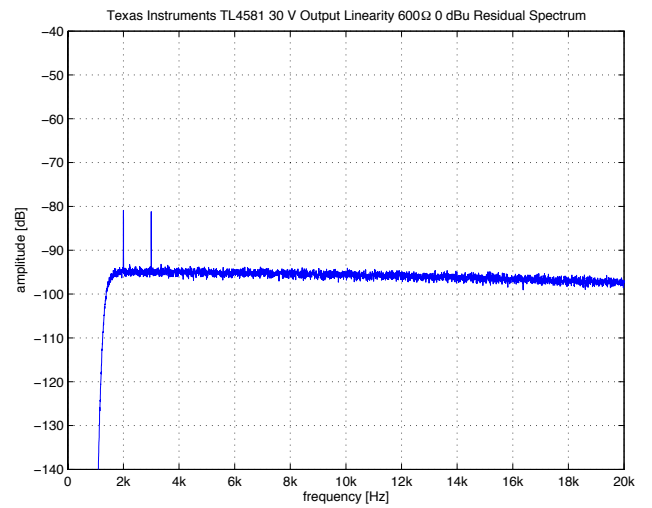
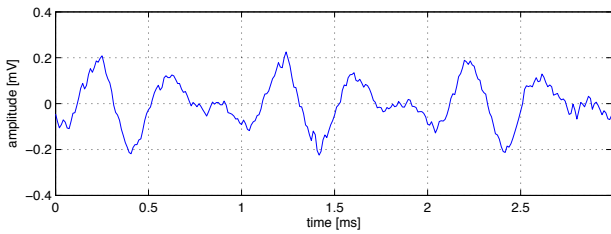
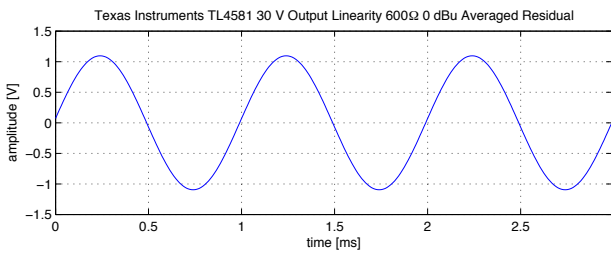
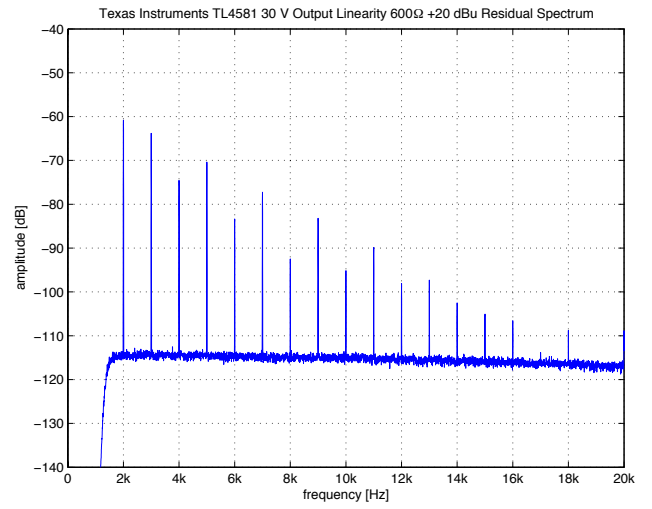
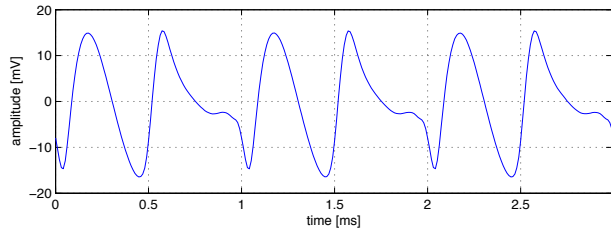
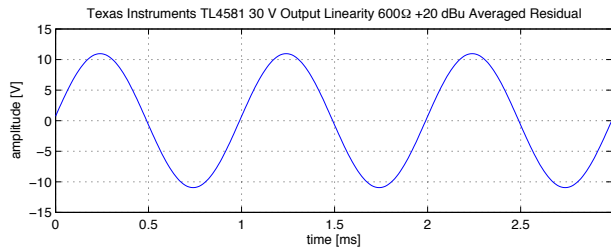
Table 3.28: Specifications for  $T_A = 25^\circ \text{C}$  and  $V_S = \pm 15 \text{V}$ .

The specifications of this amplifier are surprisingly similar to the NE5532 (see page 148) of the same manufacturer; the distortion measurements clearly indicate that this is indeed the same chip with another name. Fortunately the manufacturer makes the choice simple by charging more for the TL4581—measurements at higher supply voltage and further discussion of this amplifier is hence omitted.









## Appendix A

# Some Personal Conclusions

Besides providing the so far lacking systematic measurement data on opamp distortion and by this hopefully simplifying and speeding up the selection of a low distortion amplifier for a given application, the author intended to research the following questions with this measurement series:

- How does the distortion performance of typical IC amplifiers behave at low levels, especially with heavy output loading (i.e. the potential presence of significant crossover distortion)?
- How large is the influence of power supply voltage on distortion performance (i.e. do higher supply voltages provide better—or perhaps worse—distortion performance)?
- How does the distortion performance of discrete opamps compare with good IC amplifiers?

The first question can be answered as follows: For essentially all tested IC amplifiers the linearity measured at 1 kHz and a level of 0 dBu is considerably better than at +20 dBu, with or without output loading. Without output loading, the linearity at 0 dBu is in fact usually better than the measurement limit (given in this case by the noise level of the amplifier and the FFT resolution of the according spectral analysis), corresponding to a distortion level of at least 150–170 dB below the fundamental for a configuration with low noise gain. With 600  $\Omega$  output loading, this figure deteriorates typically by one or two orders of magnitude.

At a level of –20 dBu, both loaded and unloaded case give distortion readings below the measurement limit for most tested amplifiers (i.e. a distortion level of at least 130–150 dB below the fundamental for a configuration with low noise gain). It must be concluded that at medium levels around 0 dB output stage nonlinearity is for most amplifiers a dominant distortion mechanism, although the resulting performance is still mostly ex-

cellent. At lower levels this contribution vanishes, leaving distortion which is usually unmeasurable with the used setup.

For the second question—the dependence of distortion on power supply voltage—the following was found: Generally speaking distortion shows little dependence on power supply voltage, at least at levels sufficiently below clipping.<sup>1</sup> With respect to common-mode, input impedance and thermal distortion some exceptions are found though. The later typically shows an increase while the other two improve at higher supply voltages. The selection of a power supply voltage for lowest distortion may hence ask for a compromise in certain circumstances. However, the differences are usually rather small, making practical considerations (such as the availability of a certain supply voltage within a larger system) the overriding concern in probably the most cases.

The third question must remain unanswered for the time being as not enough discrete amplifiers have been tested yet.

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<sup>1</sup>It must be added though that the lowest supply voltage tested was  $\pm 15$  V; significantly lower voltages may lead to different results, but are not usually used for audio purposes.



## Appendix B

# Operational Amplifier Topologies

In this chapter we will quickly review the most important basic amplifier topologies. Opamp topologies are most often classified by the number of gain stages. For low-distortion amplifiers topologies with one to three stages are most suitable.<sup>1</sup> There exists a trade-off between speed (bandwidth and slew-rate) and DC precision (open-loop gain and drift) with respect to the number of stages; typically it is observed that for a given quiescent current adding a gain stage degrades speed by a factor of two [16]. As a rough rule of thumb it might be said that adding a gain stage improves DC precision by an order of magnitude though.

We can hence conclude that the optimum number of stages for low distortion depends on the frequency of interest. At higher frequencies (say 10 kHz and up) slew-rate is of great importance for low distortion, as has been pointed out before; topologies with few gain stages are hence at an advantage. At the lower end of the audio frequency range (below 1 kHz) the high open-loop gain of topologies with multiple gain stages pays off; in addition to this one might suspect that these amplifiers which are often optimised for low drift would show reduced thermal distortion as well—the measurement data however tells that this is not necessarily the case.

In the following we discuss the different topologies and highlight their basic advantages and disadvantages with respect to distortion performance. Note that these elaborations are of very general meaning only—as can be observed in the measurement data chapter, performance amongst different amplifiers with similar topologies can vary to a great extent; only actual measurement of the amplifier will reveal the attained performance. In addition to this it should be noted that the choice of overall topology has mainly

---

<sup>1</sup>Note that sometimes a unity gain output stage—which provides current gain but no voltage gain—is counted as stage as well, especially in the audio literature (e.g. [2]). The here discussed topologies would then have two to four stages with this nomenclature.

an influence on transfer linearity. The common-mode and input impedance linearity performance is heavily dependent on the exact implementation details of the input stage and largely independent of the rest of the amplifier; output distortion is partially related to overall topological choices but again closely dependent on the output stage design. Discussing input and output stage implementation in sufficient detail is beyond the scope of this paper though.

## B.1 One-Stage Topology

One-stage topologies are almost invariantly based on a folded cascode topology, as depicted in figure B.1. The folded cascode greatly increases the output impedance of the input stage, allowing reasonably high gain with a single stage. As the open-loop gain is directly proportional to the impedance at the cascode output (Q4 collector) great care will be needed in designing the current mirror collector load (Q5–Q7) and the output stage to avoid loading this node. The linearity of that topology will to a great extent depend on how well this is handled; the impedance needs not only to be high but also level independent up to high frequencies. Especially troublesome are junction and substrate capacity which effectively appear in parallel with the compensation capacitor C1. As their capacity is voltage dependent modulation of the gain bandwidth product results, leading to increased high-frequency distortion. The output stage will in any case need to be a double emitter follower to give sufficient load independence; for best performance even a triple follower must be used. The current mirror is either a Wilson type as shown in figure B.1 or a more complicated structure.

Various enhancements addressing the limited open-loop gain of the basic one-stage opamp have been developed, see e.g. [17][18][19]. The one probably most suitable for achieving low distortion is shown in figure B.2. The current mirror is not directly connected to the supply rail but kept floating by means of current source J5. Emitter follower Q7 bootstraps the collector of Q6 to the output voltage; this effectively increases its output impedance (including the contribution of junction capacity) by  $h_{FE}$  of Q7. As the collector/base of Q5 now tracks the output voltage as well a capacitor connected from this node to the amplifier output can be used to cancel output stage distortion by injecting an error current into the current mirror [13].

This topology has been advertised to combine the speed of single-stage topologies with the DC precision of three-stage architectures; the author suggest however that it would be more fair to say that they combine the speed of a single-stage architecture with the DC precision of two-stage topologies as offset drift is usually an order of magnitude worse than that of three-stage opamps. In any case these opamps are amongst the best ICs currently

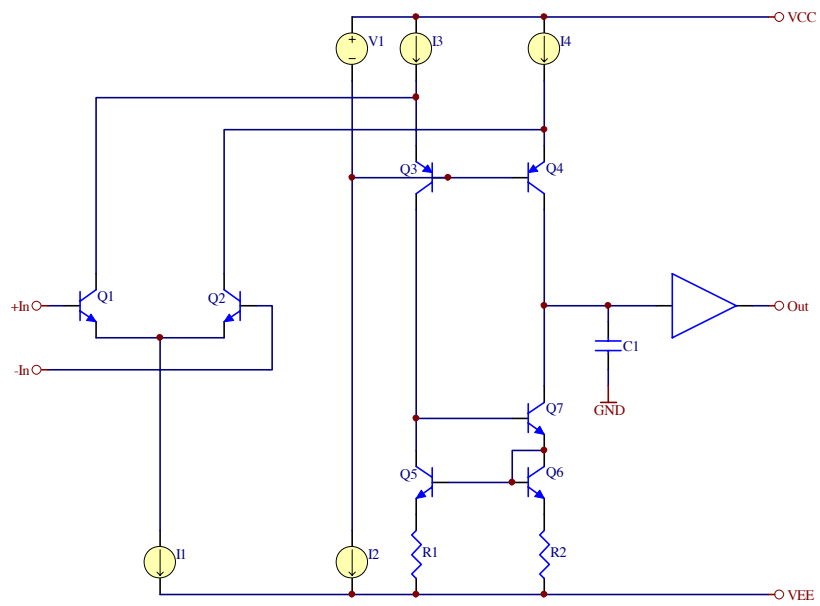


Figure B.1: One-stage folded cascode amplifier architecture.

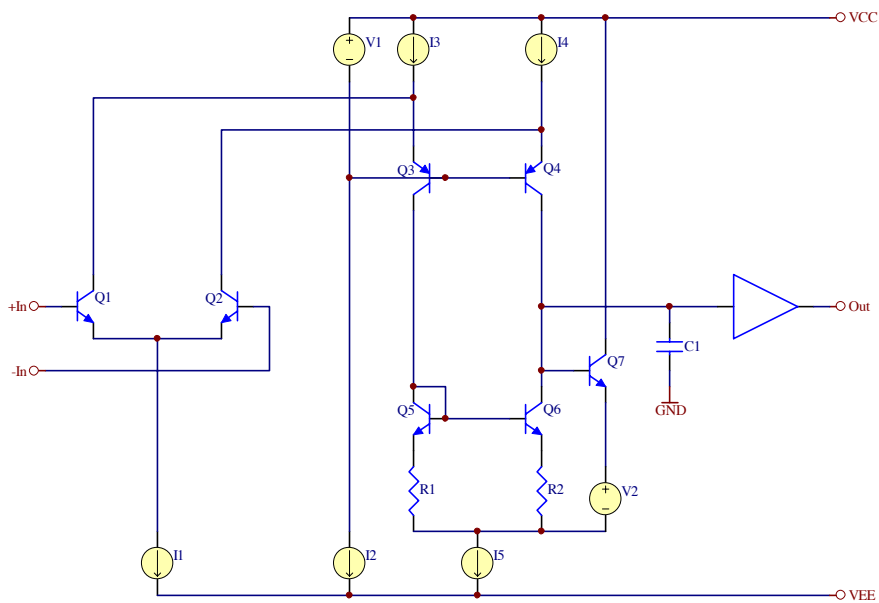


Figure B.2: Folded cascode opamp topology with bootstrapped current mirror collector load.

available with respect to distortion—see e.g. the AD797 and LT1469. As for best performance this topology needs to be implemented in a bipolar process these amplifiers tend to be rather costly though.

## B.2 Two-Stage Topology

Figure B.3 shows a typical implementation. The input pair Q1/Q2 is loaded with an active collector load (the current mirror formed by Q3, Q4, R1 and R2) which provides the balanced-to-single-ended conversion. Q5 and Q6 make up the second stage. As pointed out e.g. in [2] this topology has many advantages which makes it particularly suitable for a low distortion amplifier. In a nutshell these are:

- The voltage gain of the amplifier is almost entirely provided by the second stage. This makes up for easy compensation—particularly as the second stage is the dominant pole to start with—and results in a relatively low number of secondary poles.
- The compensation capacitor C1 provides so-called *pole splitting*, i.e. it moves the secondary poles of the input stage and output buffer upwards in frequency [3]. The unity gain frequency can hence be set higher than would be expected from a separate analysis of the gain stages.
- The compensation capacitor C1 provides local feedback to the second stage which increases with frequency at 6 dB/octave. As global feedback reduces with frequency at typically the same rate the total feedback applied to the second stages remains (as a first-order approximation) constant with frequency. This greatly reduces the distortion contribution of the second stage compared to the usual case where total feedback reduces with frequency.
- The local feedback applied to the second stage decreases the output impedance of this stage at high frequencies. This makes this gain stage less susceptible to (potentially voltage-dependent) loading from the output stage which would otherwise result in increased distortion.

Note that some of these points apply to the other discussed topologies as well, but that the two-stage architecture is unique in combining all of them. It is particularly suited for discrete implementation (e.g. power amplifiers), as the sum of its advantages makes up for low parts count—even lower than for the intuitively simpler one-stage topology—in a typical implementation.

If this topology is implemented on a standard (i.e. not complementary) bipolar IC process it is usually done with a PNP input, i.e. as the complementary amplifier to the one shown in figure B.3. Otherwise Q6 would

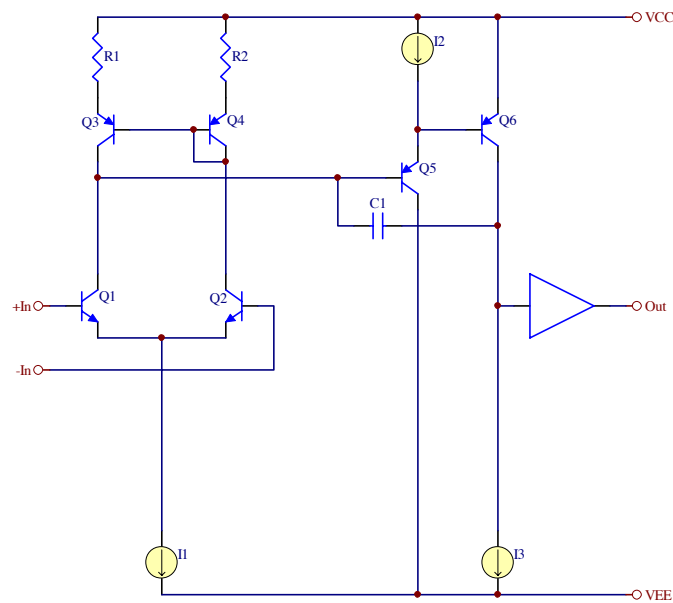


Figure B.3: Typical two-stage opamp topology.

become a slow lateral device which would severely restrict the achievable speed. The use of lateral devices for Q1/Q2 limits the speed of the amplifier as well but the restriction is less serious. Alternatively they can be cheaply implemented as P-channel JFETs, e.g. as in the TL071/TL072/TL074 and the various descendants which all offer modest distortion performance as they are typically optimised with respect to low quiescent current and cost. If implemented in a modern fully complementary process very low distortion amplifiers can result though (see e.g. the LT1213).

### B.3 Three-Stage Topology

Figure B.4 shows a typical three-stage topology. Q1 and Q2 are the first stage input transistors; while the use of a resistive collector load for the input pair and a balanced second stage (Q3–Q8) lead to potentially very good drift performance, the resulting first stage gain is lower than with an active collector load (as used e.g. in the two-stage topology of figure B.3). This necessitates the use of a third stage (Q9 and Q10) in order to provide overall high open-loop gain. As the collector impedance of Q10 is not particularly sensitive the output stage can be a single emitter follower, although for lowest gain sensitivity a dual emitter follower is used.

Compensation of this topology is not easy and requires at least three large capacitors: C1 makes the drive to the second stage single-ended at high frequencies while C2 sets overall compensation. Feed-forward capacitor C3

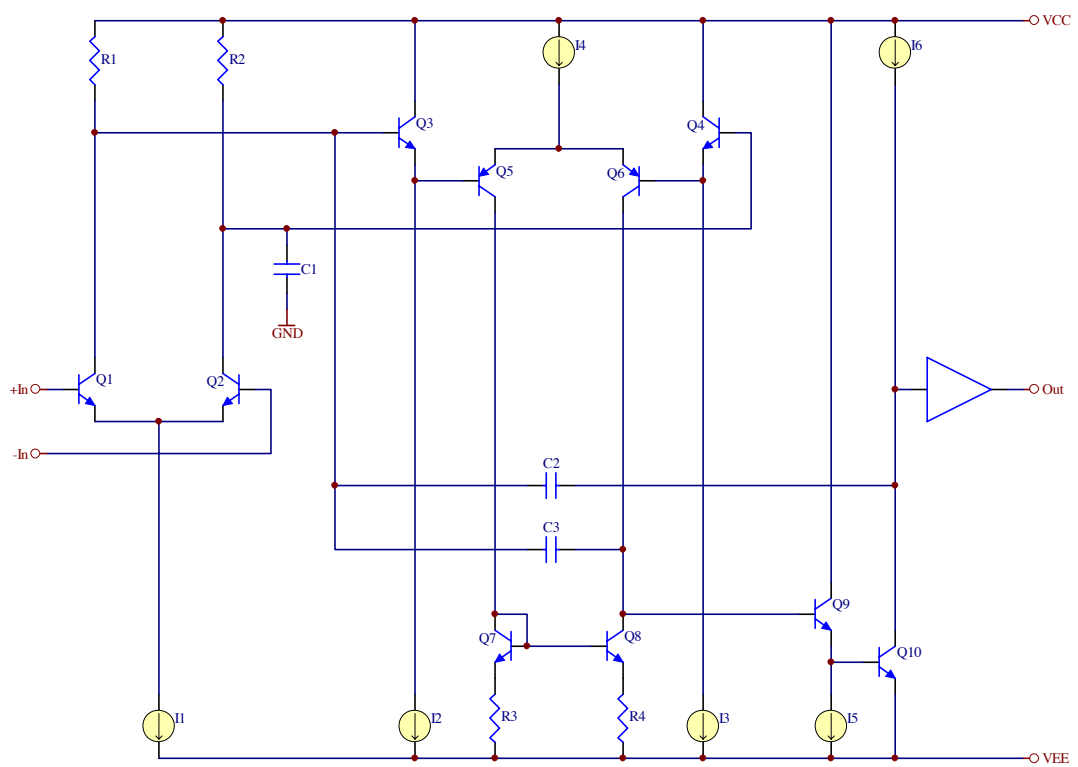


Figure B.4: Typical three-stage opamp.

bypasses the PNP level shifter transistors Q5 and Q6 at high frequencies; this allows easy implementation in a standard non-complementary IC process as with the feed-forward capacitor the slow lateral PNP devices do not limit the amplifier gain bandwidth product. Compared with a two-stage topology (which needs to be implemented as PNP input on a standard bipolar process as noted above) the input transistors Q1 and Q2 are of NPN polarity. These have higher  $h_{FE}$ , which in turn reduces input bias and offset currents. These advantages probably explain—in addition to the mentioned drift advantage of the resistive input transistor collector load—the predominance of the three-stage topology over the two-stage architecture in IC amplifiers.

Even with the feed-forward capacitor the resulting bandwidth and slew-rate is usually lower (and with respect to slew-rate also more asymmetric) than for the other discussed topologies though. If high speed is to be realised with such a topology the quiescent currents need to be high; the LT1115 is such an example.

## Appendix C

# Change Log

The following list records the additions and changes applied to this document.

### September 1, 2008

- First release.



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